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Low Leakage Charge Recycling Power Gating Structure for CMOS VLSI Circuits

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Abstract: Power dissipation has become an important factor in integrated circuits fabrication due to the rapid increase of battery powered hand held devices. In particular static dissipation increases considerably as technology scales down. To extend the battery lifetime of portable devices and ensure proper operation of digital circuits, static dissipation reduction needs to be addressed. In this paper, a low leakage charge recycling technique is proposed for this concern. The simulation results reveal that this technique exhibits 74 % leakage reduction, 37 % ground bounce reduction, 58 % Power Delay Product (PDP) reduction and nearly 10-33 % improvement in noise margin compared to conventional technique.

Keywords: charge recycling; data retention; drowsy mode; leakage power; power gating; sleep mode

Vezja CMOS VLSI z nizkim uhajalnim tokom vrat

Izvleček: S porastom števila baterijsko napajalnih naprav je poraba energije postala ključen problem pri izdelavi integriranih vezij. Natančneje, z manjšanjem velikosti vezij se poraba povečuje. Za podaljšanje baterijskega delovanja in zagotavljanje zanesljivega delovanja prenosnih naprav je porabo energije potrebno posebej obravnavati. V članku je predlagana tehnika nizkega uhajalnega toka in obnovljivega naboja. Rezultati nakazujejo 74 % znižanje uhajalnega toka, 27 % znižanje vpliva ozemljila, 58 % znižanje PDP in 10 - 33 % izboljšanje meje šuma glede na klasične tehnike.

Ključne besede: obnavljanje naboja; zadržanje podatkov; uhajalni tok; stanje pripravljenosti

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1 Introduction

Power dissipation in CMOS circuits mainly has two important components namely dynamic power dissipation and static power dissipation. Total power dissipation is dominated by dynamic power or switching power component. However in deep submicron technologies, static power is increasing and it is nearing the dynamic power [1]. Hence the concept of minimizing static power gains importance, if the devices remain idle for long time as its battery power will be drained off due to leakage. Static Power in CMOS circuits results due to the leakage currents flowing through the transistor when there are no input transitions. The main sources of leakage currents in a MOS transistor [2] are shown in figure 1.

Sub-threshold Leakage: The current which flows from the drain to the source of a transistor operating in the weak inversion region.

Gate leakage: The current which flows directly from the gate through the oxide to the substrate due to gate oxide tunnelling and hot carrier injection.

Gate Induced Drain Leakage: The current which flows from the drain to the substrate induced by a high field effect in the MOSFET drain caused by a high V_{DG}.

Reverse Bias Junction Leakage: It is caused by minority carrier drift and generation of electron/hole pairs in the depletion region.

Sub threshold leakage is the most predominant component compared to other leakage sources and minimizing this will lead to substantial decrease in static power [2]. Throughout this paper leakage refers to sub threshold leakage. Several techniques have emerged to reduce leakage power. Mutoh [3] proposed a power gating technique (sleep approach) which cuts off power to the circuit blocks when they remain idle. In sleep

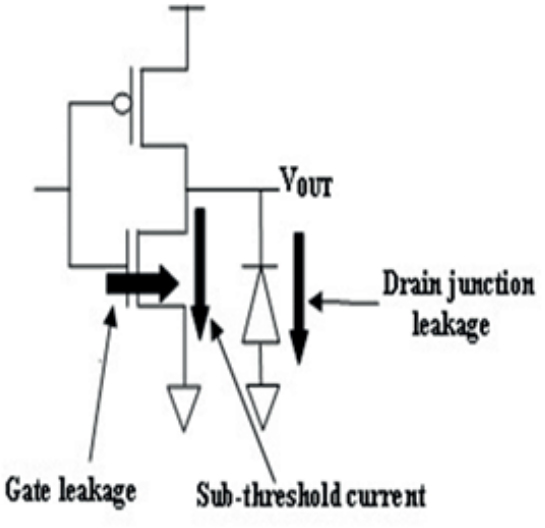

Figure 1: Leakage Currents

approach, the circuit blocks operate in active and sleep modes. High leakage reduction is obtained in sleep mode but the data in the circuit blocks are lost. Also when the circuit makes a transition between active and sleep mode, a large rush through current flows through the sleep transistor. When the circuit is in active mode, charge is stored at the gate of the sleep transistor and it is dumped to ground as the circuit moves to other state. No attempt is made to use the charge at the gate of the sleep transistor.

In this paper, we introduce low leakage charge recycling power gating structure which reuses the charge stored at the gate of sleep transistor to reduce rush through current and to provide data retention. The remainder of the paper is organized as follows: Section 2 describes about the literature survey of the leakage reduction techniques. The proposed technique and its functionality are elaborated in section 3 and the experimental results are discussed in section 4. Section 5 concludes the work.

2 Previous work

In CMOS circuits, data in the circuit blocks are lost if the circuit block is in standby mode. This becomes undesirable if the standby duration is short. To retain the data, an intermediate data preserving mode called drowsy mode is introduced by raising the virtual ground node voltage, thereby maintaining a significant voltage difference across the circuit blocks. The virtual ground voltage is raised by utilizing clamping devices like diodes, MOS transistors etc.

In [4], the authors proposed a sleep buffer approach which provides data retention without using any clamp devices. In sleep buffer technique, virtual ground voltage is raised, by recycling the charge at the gate of sleep transistor through sleep buffer and it works well when the circuit switches between active and drowsy modes frequently but the sleep mode is lost. This approach provides power gating to internal circuits and sleep buffer, but is not suitable for long idle periods due to high leakage. In [5], authors proposed a tri modal switch (TMS) which provides low leakage sleep mode and uses charge recycling for data retention. In sleep mode, leakage reduction is offered but a sneak path exists from V_{DD} to ground through sleep and drowsy transistors. TMS technique is not efficient in terms of area and leakage reduction. In paper [6], the authors propose a charge recycling technique as shown in figure 2, which reuses the charge at the gate of the sleep transistor to clamp the virtual ground level, thereby attaining data retention in intermediate mode. In this technique, a pass transistor (PT) is connected between the virtual ground rail and gate of sleep transistor for recycling the charge during mode transitions but the leakage power is soaring. In this paper, we provide an efficient power gating technique which mitigates leakage power in sleep mode and provide low energy, low ground bounce based on charge recycling concept.

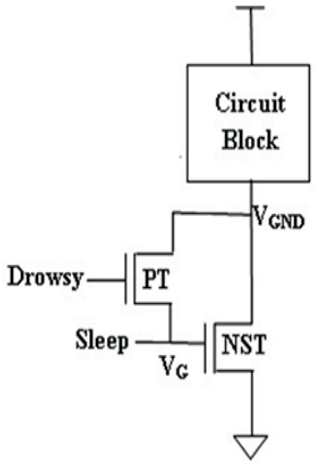

Figure 2: Charge Recycling Technique

3 Proposed technique

In this section, we present the circuit configuration and functionality of the proposed low leakage charge recycling (LLCR) technique. Figure 3 shows the circuit configuration of LLCR technique and its functionality is provided in Table 1. A PMOS transistor (PST) at the supply rail and NMOS transistor (NST) at the ground rail are used for power gating. A pass transistor (PT) is connected between V_G and V_{GND} for charge recycling and for boosting the V_{GND} level. LLCR technique enables three different circuit operation modes: active, sleep

and drowsy depending on the values of the control signals as shown in table 1.

Table 1: LLCR Technique Functionality

Sleep	Sleep bar	Drowsy	Circuit Mode
1	0	0	Active
0	1	0	Sleep
0	0	1	Drowsy

3.1 Active Mode

In active mode sleep bar, drowsy signals are low and sleep signal is high making the transistors PST and NST *on* and transistor PT *off*. As the sleep transistor is *on* the virtual ground (V_{GND}) node voltage is approximately at zero level. The voltage across the CMOS circuit block is $\approx V_{DD}$ and the circuit block resumes its normal operation. As the sleep signal is raised high, the voltage at the gate of the sleep transistor (V_G) is raised and the electric charge gets stored at V_G.

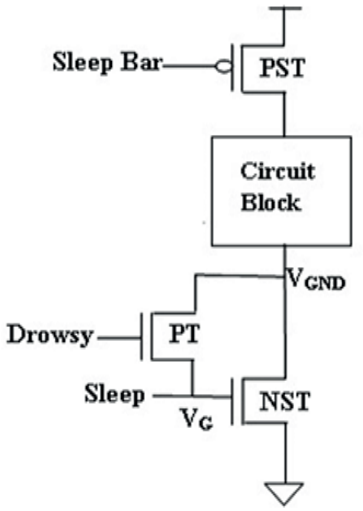

Figure 3: Low Leakage Charge Recycling Technique

3.2 Drowsy Mode

In drowsy (intermediate power saving) mode, drowsy signal is set to high while the sleep signal is set to low. The drowsy transistor is *on* and the charge stored at the gate of sleep transistor during active mode, increases the virtual ground voltage through the *on* drowsy transistor.

At the beginning of mode transition from active to drowsy, the drain current of the sleep transistor is given by

$$I_D = \mu_n C_{ox} \frac{W}{L}\left[(V_{gs} - V_{th})V_{ds} - \frac{V_{ds}^2}{2}\right] \quad (1)$$

The transistor PT conducts when the drowsy signal is high and the charge stored at V_G flows into V_{GND} through PT. This process continues until the charge at V_{GND} and V_G are equalized. Thus the drain and gate nodes of sleep transistor are connected through the pass transistor and its *Vgs* and *Vds* becomes equal. Now the current I_D through sleep transistor is as in equation (2).

$$I_D = \mu_n C_{ox} \frac{W}{L}\left[\frac{V_{ds}^2}{2} - V_{th}V_{ds}\right] \quad (2)$$

The current I_D in equation (2) flows from virtual ground to ground and the V_{GND} voltage reaches equilibrium (*Vcr*) at the balance point of the leak current of the circuit block and the current through the sleep transistor. Thus the voltage level of V_{GND} node is increased to *Vcr* and the voltage across the circuit block is (V_{DD}-/*Vtp*/-*Vcr*), which is sufficient to retain the data in the block.

3.3 Sleep Mode

When the sleep, drowsy signals are low and sleep bar signal is high, transistors PST, NST and PT are *off*. The voltage across circuit block is zero and it enters into deep sleep mode. According to Table 2, gate leakage of PMOS is high, if it is in (011) state, that is when the PMOS is in direct contact with V_{DD} due to tunnelling of more electrons. In figure 2 all the PMOS transistor in the pull up network are connected to V_{DD}, which means that there are higher possibilities of electrons tunnelling from gate to source if the gate voltage of PMOS transistors are zero. In LLCR technique, only the sleep transistor (PST) is in direct contact with V_{DD} and all other PMOS transistors in the pull up network are connected through PST. In sleep mode, since PST is not in (011) state, no PMOS transistors in the circuit block are in (011) state even if their gate voltages are zero and thus the gate leakage is drastically reduced.

Table 2: Gate Leakage Currents; G=Gate, D=Drain, S=Source

Device	Bias	90nm	65nm	45nm
	{GDS}	(nA)	(nA)	(nA)
PMOS	110	7.739	212.2	1240.5
PMOS	101	7.739	212.2	1240.5
PMOS	100	15.478	424.5	2480.7
PMOS	011	12.594	347.2	1991.5

Gate Leakage Current of PMOS at four significant states: [7]

Sub threshold leakage current of a MOS transistor is given by

$$I_{ds} = I_{dso}\, e^{\frac{Vgs - Vto + \eta Vds - K\gamma Vsb}{nv_T}} \left(1 - e^{\frac{-Vds}{v_T}}\right) \quad (3)$$

Where I_{dso} is the current at threshold, *n* is a process-dependent term affected by the depletion region characteristics, η is the DIBL coefficient, *Vto* is the threshold voltage when the source is at the body potential, V_T = k*T*/q = 26 mV, S is sub threshold slope and *k*γ is the body effect coefficient. Sub threshold leakage current increases with *Vds* due to DIBL effect. In the proposed technique *Vds* of the PMOS transistors in the pull up network is very less as they are not in direct contact with V_{DD}. Hence as per equation (3) the sub threshold leakage reduction is high in LLCR technique. Therefore it is observed that the overall leakage reduction in LLCR is significantly better than charge recycling technique as the proposed LLCR technique suppresses the major constituents of leakage.

4 Experimental results

We estimated leakage power, noise margin, ground bounce, delay and power delay product for conventional charge recycling and low leakage charge recycling techniques. We used Synopsys HSPICE for simulation of a two input NAND gate using 32nm PTM models [8]. Section 4 is organized as follows: Estimation of static power is characterized in section 4.1, ground bounce analysis is done in section 4.2, power delay product is discussed in 4.3. Section 4.4 deals with static noise margin analysis.

4.1 Static Power Estimation

In CMOS circuits, leakage of pull up network is determined by the parallel PMOS transistors that are in direct contact with V_{DD}. Considering figure 2, all the PMOS transistors in the pull up network are in direct contact with V_{DD} and as the circuit blocks size increases, number of PMOS parallel paths in contact with V_{DD} also increases and the leakage increases. Considering the proposed scheme, sub threshold leakage is determined by only one PMOS transistor (PST) irrespective of the circuit block size. This illustrates that the leakage in proposed LLCR technique is less compared to the leakage in the structure of figure 2. The leakage current and static power comparisons in sleep mode are shown in figure 4 and figure 5 respectively.

4.2 Ground Bounce analysis

In CMOS circuits the parasitic components of the power and ground distribution networks produce power/ground bounce. As shown in figure 6, the instantaneous discharge current through the sleep transistor gives rise to current surges during mode transitions and the bouncing noise in one power gating domain is transferred to the surrounding active circuits blocks through the shared power and ground distribution networks. The active circuit blocks thereby may errornously latch a wrong value or switch at a wrong time, if the voltage due to the ground bounce is more than the noise margin of the circuit. The ground bouncing noise has become an important reliability issue in nanometer regime with shrinking noise margins.

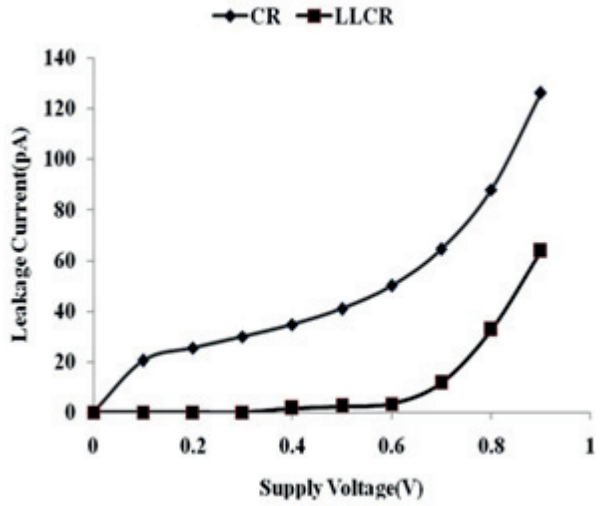

Figure 4: Leakage Current Comparison

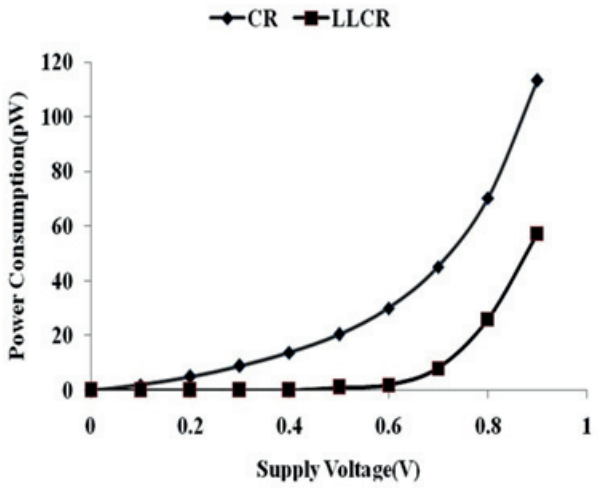

Figure 5: Static Power Comparison

The parasitic resistance, inductance and capacitance used for ground bounce calculation are 217 mΩ, 8.18 nH and 5.32 pF [10]. Figure 7 shows the ground bounce due to transitions from sleep to drowsy mode. Conventional charge recycling technique switches from 16.6 mV to 36.8 mV and the proposed LLCR technique switches from 14 mV to 30.9 mV. Hence it is clear that the proposed technique perform better as compared to the

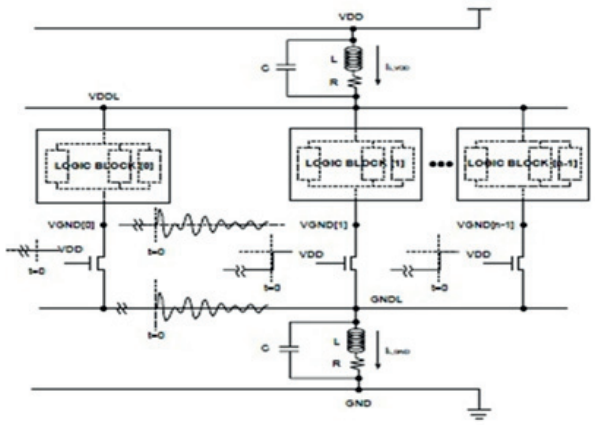

Figure 6: Ground bounce in a System-on-a-Chip employing multiple power gating structures to control leakage power [9].

conventional charge recycling technique. The average virtual ground voltage of CR and LLCR technique during mode transition is 180 mV and 114 mV respectively and it is given in table 4 which implies that the ground bounce surges are less in the proposed technique.

4.3 Power Delay Product Estimation

Power delay product (PDP) is another important factor for analysing the digital circuits, which is a product between propagation delay and power consumption. Static power delay product comparison is shown in figure 8. The delay of LLCR technique is 8.556E-12 seconds while the delay of conventional technique is 5.32E-12 seconds. Delay of LLCR technique is more due to the parasitic capacitance of the additional PMOS sleep transistor (PST). However the proposed method has a superior performance in terms of power delay product compared to the conventional charge recycling technique as the leakage power dissipation of LLCR technique is much less.

4.4 Static noise margin

In drowsy mode data stability should be high as this mode is meant for preserving the data. Noise margin defines the data stability of the circuits in data retention mode by determining the allowable noise voltage on the input so that the output will not be corrupted. Higher the noise margin better is the stability. The specification most commonly used to describe noise margin are the low noise margin NM_L, and the high noise margin NM_H. These parameters are estimated from the DC transfer characteristics of the circuits by calculating V_{IL}, V_{OL}, V_{IH} and V_{OH} values. The DC characteristics and its slope of the proposed technique for noise margin calculation are shown in figure 9.

Noise margin values depend on the effective supply voltage experienced by the circuit block. As the average virtual ground voltage value of LLCR technique is less during mode transitions, the supply voltage experienced by the circuit block is more leading to good data retention and stability as compared to conventional technique. Table 3 lists the noise margin values and it is clear that the data stability is high in LLCR

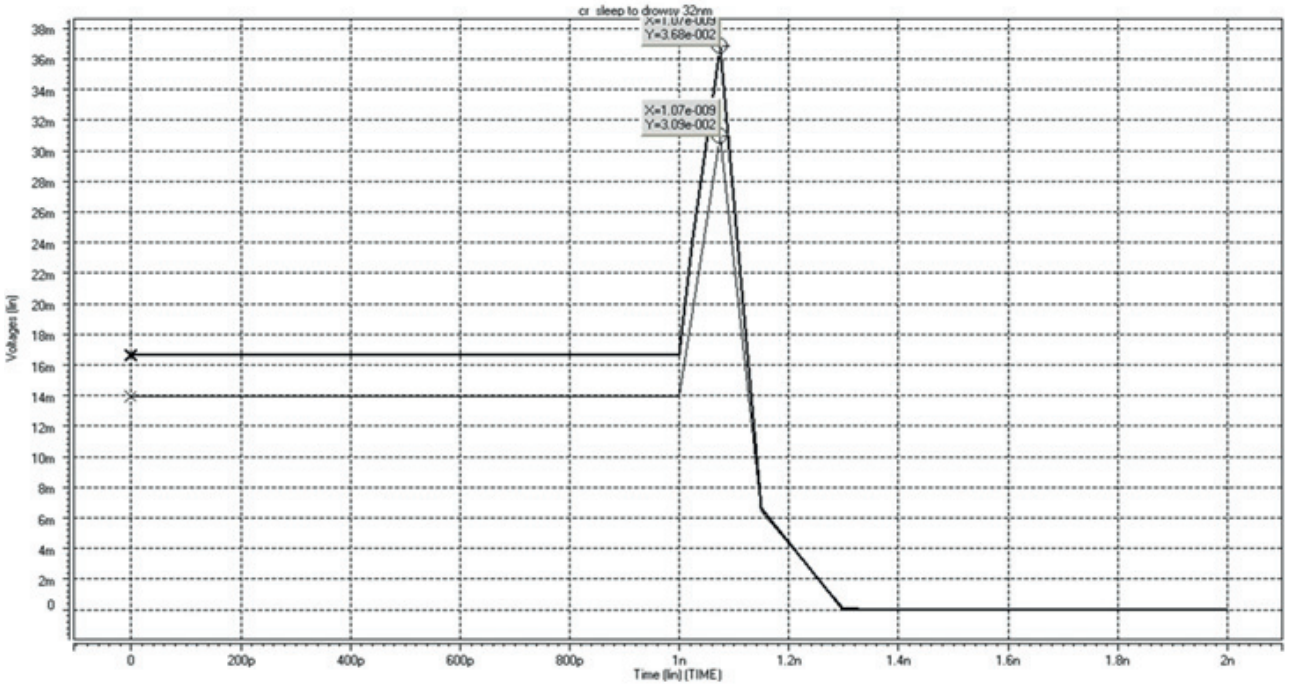

Figure 7: Ground Bounce Comparison

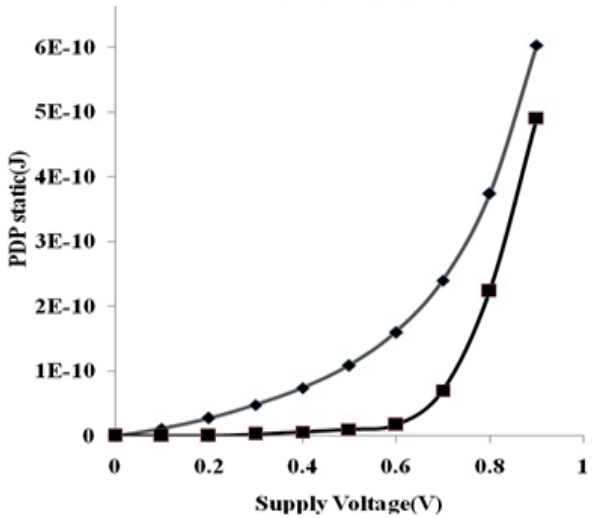

Figure 8: PDPstatic Comparison

technique by a maximum of about 32.5 % over conventional technique.

Table 3: Static Noise Margins (mV)

Technique	NML	NMH
LLCR	266	293
CR	243	221

The performance characteristics comparison shown in table 4 proves that the low leakage charge recycling technique performance is better than conventional charge recycling technique. In conventional power gating structures always there is a trade off between the leakage power and ground bounce but the proposed technique offers both leakage power and ground bounce reduction.

Table 4: Performance Characteristics

	CR	LLCR
Static Power(xE-10W)	2.2947	0.5980
Average Vgnd Voltage(xE-1V)	1.8090	1.1450
Delay(xE-12S)	5.32	8.55
PDP(xE-21J)	1.2214	0.5081

5 Conclusion

In this paper performance characteristics such as leakage power in sleep mode, data stability, ground bounce and power delay product of conventional charge recycling technique and proposed LLCR technique are scrutinized in detail. From the analysis it is apparent that the LLCR technique consumes low power in sleep mode compared to conventional charge recycling technique. Ground bounce, noise margin and power delay product estimation makes clear that this scheme is an efficient power gating technique. The proposed LLCR technique can be used in hand held devices such

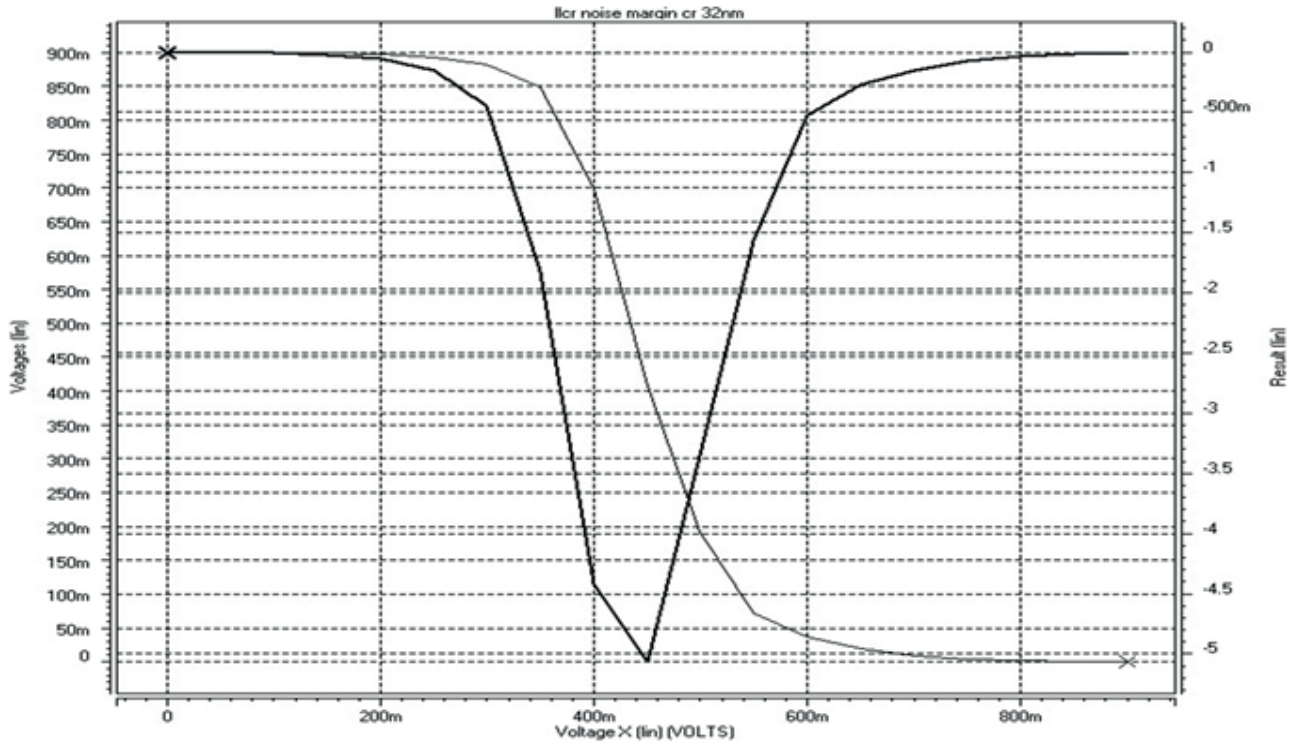

Figure 9: DC transfer Characteristics of LLCR Technique

as mobile phones and laptops for leakage reduction and data retention if the devices are idle for short duration as well as for long duration.

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