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Variable Gain Amplifier for mobile WiMAX receiver

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Abstract: In this paper a Variable Gain Amplifier (VGA) applied to mobile WiMAX standard is presented. The VGA plays an indispensable role in radio frequency receiver. It keeps the signal power falling to the ADC constant while the input one varies substantially. The proposed VGA cell is composed of two transimpedance amplifiers and a transconductance amplifier. Flexibility was ensured to VGA control using a novel method based on active resistor implemented with current conveyer structure. The VGA circuit is optimized for high gain, low noise and low power consumption. In order to attempt mobile WiMAX standard specifications, three VGA cells are cascaded. The studied circuit is designed in CMOS 0.35 µm AMS process technology. It can provide a maximum gain of 74 dB and a minimum gain of 20 dB. The simulated structure provides less than 21 dB of noise figure, a CMRR of 82 dB and a margin phase of 97 °. It achieves an ICP1 of -15.5 dBm. The power consumption is approximately equal to 15 mW under ±0,75 V supply voltage.

Keywords: Variable Gain Amplifier; mobile WiMAX; high gain; low noise

Ojačevalnik s spremenljivim ojačenjem za mobilni WiMAX sprejemnik

Izvleček: Predstavljamo za mobilni WiMAX prilagojen ojačevalnik s spremenljivim ojačenjem (VGA). VGA igra neizogibno vlogo v sprejemniku radijske frekvence. Drži signalno moč na ADC konstanti, pri spremenljivem vhodnem signalu. Predlagana VGA celica je sestavljena iz dveh transimpedančnih in enega transkonduktančnega ojačevalnika. Fleksibilnost kontroliranja VGA je zagotovljena z aktivnim uporom, ki je realiziran s tokovno prenosno strukturo. VGA vezje je optimizirano za visoka ojačenja, nizki šum in nizko porabo energije. Za zagotavljanje standardov mobilnega WiMAX je uporabljena kaskada treh VGA celic. Vezje je izdelano v CMOS 0.35 µm AMS tehnologiji. Največje ojačenje je 74 dB, najmanjše 20 dB. Šum simulirane strukture je pod 21 dB. CMRR je 82 dB in robna faza 97 °. Dosega ICP1 -15.5 dBm. Pri napajalni napetosti ±0.75 V je poraba okoli 15 mW.

Ključne besede: Ojačevalnik s spremenljivim ojačenjem; mobilni WiMAX; visoko ojačenje; nizek šum

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1 Introduction

The IEEE 802.16 task group has been founded in 1999 to develop wireless broadband standards. This family of standards is authored by the Institute of Electrical and Electronics Engineers (IEEE). It belongs to the Wireless Metropolitan Area Networks (WMAN). It has been commercialized under the label WiMAX (Worldwide Interoperability for Microwave Access) by the WiMAX forum industry [1]. The forum is an organization that certifies and promotes the interoperability and compatibility of broadband wireless products based upon IEEE 802.16 standards. Different projects were proposed by the working group. The mainly approved standards areWiMAX for fixed and mobile applications [2]. IEEE 802.16a is addressed to fixed application. The frequency band is between 10-66 GHz for LOS (Line Of Sight) environments and 2-11GHz for NLOS (Non LOS) environments. IEEE 802.16e adds mobility and allows communication from base station to mobile phone and laptop. Mobile WiMAX operates in the frequency band of 2-6 GHz. It promotes a data rate up to 70 Mbit/s and a distance up to 50 km theoretically [3].

This work will be restricted to the mobile WiMAX standard. Mobile WiMAX specifications are given in [2] in the physical layer section. Only OFDMA (Orthogonal Frequency Division Multiple Access) modulation scheme is used. A mobile WiMAX receiver shall be able of detecting and decoding a maximum input signal of -30 dBm and a minimum input signal of -91 dBm. NF (Noise Figure) shall be less than 8 dB in addition to a maximum of 5 dB from implementation losses [2]. In our research we are inter-

ested in the profile operating in the 3.4-3.6 GHz frequency band. Thus the channel bandwidth is set to 10 MHz and the receiver uses TDD (Time Division Duplexing) for duplexing mode and 1024 for the FFT size [4].

In mobile WiMAX standard, it is required to design the receiver frontend with low cost and low power consumption to ensure integrability and mobility.VGA (Variable Gain Amplifier) constitutes one of the key components of the receiver. It has to maintain the signal power falling to the ADC (Analog to Digital Converter) constant while the input one varies substantially [5-9]. These variations are more important for mobile WiMAX since the receiver moves. A lot of trade-offs have to be considered when designing the VGA. Firstly, VGA has to meet high linearity since it constitutes the last component of the receiver. In the other hand, a high gain range is required in order to adjust low input signal. It is also important that VGA ensures low noise and low power consumption [10]. These constraints and requirements make VGA design task delicate and a real challenge for designers especially when it is applied for mobile WiMAX standard.

This paper is structured as follows. In section 1, VGA specifications for mobile WiMAX standard and VGA topology are detailed. VGA optimization approach is proposed in section 2. Simulation results are reported in section 3. Section 4 presents concluding notes.

2 VGA Circuit

2.1 VGA specifications

The distribution of WiMAX specifications through the different components of the receiver was completed. System level simulations were applied to a homodyne receiver. Each block characteristics, such as gain, ICP1 (Input-1 dB-Compression Point), NF (Noise Figure) and IIP3 (Third Order Intercept Point measured at the Input) are obtained. Table I lists the VGA specifications for the mobile WiMAX receiver. When the input signal is strong with large power, it doesn't require an important amplification.In this case, VGA provides low gain (21 dB).

Table 1: VGA specifications

Parameters	specifications	
	weak signal	Strong signal
Gain (dB)	72	21
NF (dB)	20	17
ICP1 (dBm)	8	5
IIP3 (dBm)	18	15

If the input signal is weak with low power, VGA should provide high amplification to reach ADC full scale.

2.2 VGA electrical design and voltage gain formulation

In this work, the adopted VGA circuit is proposed in [10]. It is composed by three cascaded blocks: two transimpedance amplifiers and a transconductance amplifier. The transconductance amplifier is based on differential pair with source degeneration topology. The chosen VGA architecture is shown in figure 1.

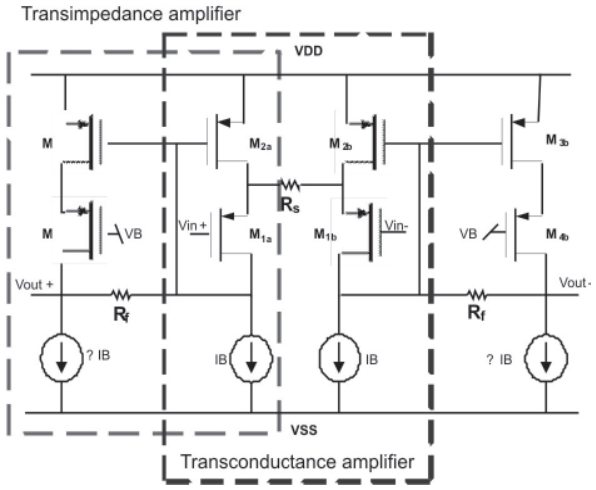

Figure 1: VGA architecture

VGA operation can be explained briefly as follows: a differential input voltage is applied to the transconductance amplifier ($M_{1a,1b}$ PMOS transistor). It is reproduced across the source degeneration resistor R_s, causing the appearance of current signal into $M_{2a,2b}$. Current amplification is then ensured by mean of the two transimpedance amplifiers. Amplified current is converted to an output voltage signal via the feedback resistor R_f. Gain range is ensured through R_s and R_f resistors variation.

Expression (1) describes the voltage gain of the VGA circuit [10] where G_m is the transcondcutance gain and R_m is the transresistance gain which is detailed in (2).

$$A_v = G_m R_m \quad (1)$$

$$R_m = - \frac{(R_f A_i - R_{in})}{(1 + A_i)} \quad (2)$$

Where R_{in} is the input resistance and A_i is the current gain of the current amplifier.

Formula (3) describes the DC differential transconductance gain. It can be approximated to $1/R_s$ if $R_s >> g_{01}/g_{m1}g_{m2}$.

$$G_{md} \approx \frac{1}{\left(\frac{g_{01}}{g_{m1}g_{m2}} + R_s\right)} \quad (3)$$

Expression (4) gives the DC transimpedance gain. If we consider that $R_f >> 1/g_{m3}$, formula (4) can be approximated to expression (5).

$$R_m = \frac{v_{out}}{i_{in}} = \frac{\frac{1}{g_{m3}} - R_f}{1 + 1/\alpha} \quad (4)$$

$$R_m \approx -\frac{R_f}{1 + 1/\alpha} \quad (5)$$

Small signal analysis is performed to the half VGA circuit. The differential voltage gain is described by expression (6) assuming that $g_m >> g_0$, $C_{gs} >> C_{gd}$ and $C_{gs2}+C_{gs3}=C_{gs2}(1+a)$. The DC voltage gain is given by expression (7) where r_{0c} is the output resistance of the current mirror (expression (8)).Considering that $R_f >> 1/g_{m3}$, $R_s > r_{o2}$ and $a >> 1$, the DC voltage gain will be reduced toR_f/R_s. The differential voltage gain formula is a transfer function presenting one zero and three poles (expressions 9-12).

$$A_v \approx A_{V0} \frac{1 - \frac{s}{\omega_z}}{(1 + \frac{s}{\omega_{p1}})(1 + \frac{s}{\omega_{p2}})(1 + \frac{s}{\omega_{p3}})} \quad (6)$$

$$A_{V0} = \frac{-(\frac{1}{g_{m3}} + R_f)(\frac{\alpha}{\alpha+1})}{(R_s // r_{02})(1 + \frac{R_f}{(1+\alpha)r_{0c}})} \approx \frac{R_f}{R_s(\frac{\alpha}{\alpha+1})} \quad (7)$$

$$r_{0c} = g_{m4} r_{04} r_{03} \quad (8)$$

$$\omega_Z \approx +\frac{g_{m1}}{C_{gs1}}(\frac{r_{01}}{r_{02} // R_s}) \quad (9)$$

$$\omega_{p1} \approx -\frac{g_{m1} r_{01} g_{m3} r_{0C}}{C_{gs1}(r_{01} g_{m3} r_{0C} + R_f)}(1 + \frac{1}{\alpha} + \frac{R_f}{\alpha r_{0C}}) \approx -\frac{g_{m1}}{C_{gs1}}(1 + \frac{1}{\alpha}) \quad (10)$$

$$\omega_{p2} \approx -\frac{g_{m3}}{C_{gs2} + C_{gs3}} \frac{r_{0C}}{(r_{0C} + R_f)}(1 + \frac{1}{\alpha} + \frac{R_f}{\alpha r_{0C}}) \approx -$$
$$\approx -\frac{g_{m3}}{C_{gs3}(1+\alpha)}(1 + \frac{1}{\alpha}) = -\frac{1}{\alpha}\frac{g_{m3}}{C_{gs3}} \quad (11)$$

$$\omega_{p3} \approx -\frac{g_{m3}}{C_L} \frac{r_{0C}}{1 + g_{m2} R_f}(1 + \frac{1}{\alpha} + \frac{R_f}{\alpha r_{0C}}) \approx -$$
$$\approx -\frac{\alpha}{R_f C_L}(1 + \frac{1}{\alpha}) = -\frac{1+\alpha}{R_f C_L} \quad (12)$$

2.3 Noise study

The input-referred mean-square noise of the VGA is given by this expression,

$$\overline{v_{ni}^2} \approx -\frac{1}{g_{m1}^2}(\overline{i_{n1}^2} + \overline{i_{n2}^2}) + \overline{v_{n,Rs}^2} + \overline{v_{n,Rf}^2}\left|\frac{1}{A_{V0}}\right|^2 +$$
$$+ \overline{i_{n3}^2}\left|\frac{1 + g_{m1}R_s(1 + g_{m2}R_f)}{g_{m1}(-1 + g_{m3}R_f)}\right| \quad (13)$$

Where:

$$\overline{i_{ni}^2} \approx 4kTg_{mi}\Delta f$$

$$\overline{v_{n,Ri}^2} \approx 4kTR_i\Delta f$$

If we consider that $g_{m2}R_f >> 1$ and $g_{m3}=g_{m2}$, (13) can be estimated to (14),

$$\overline{v_{ni}^2} \approx -\frac{1}{g_{m1}^2}(\overline{i_{n1}^2} + \overline{i_{n2}^2}) + \overline{v_{n,Rs}^2} + \overline{v_{n,Rf}^2}\left|\frac{1}{A_{V0}}\right|^2 +$$
$$+ \overline{i_{n3}^2}|R_s|^2 \quad (14)$$

2.4 Common Mode Rejection Ratio(CMRR)

The common mode rejection ratio CMRR is by definition the ratio of the common-mode gain to differential-mode gain. It describes the ability of an amplifier to reject the common mode signal while amplifying the differential signal [11-12]. It is usually expressed in dB andcan be described as:

$$CMRR = 20Log\left|\frac{A_{dm}}{A_{cm}}\right| \quad (15)$$

Where A_{dm} is the differential mode gain and A_{cm} is the common mode gain which are defined by the following expressions respectively:

$A_{dm}=(A_{11}-A_{12}-A_{21}+A_{22})/2$ (16)

$A_{cm}=(A_{11}+A_{12}+A_{21}+A_{22})/2$ (17)

Where A_{ij} are the small signal voltage gains given below:

$$A_{11} = \frac{v_{out}^+}{v_{in}^+}\Big|v_{in=0}^- \quad (18)$$

$$A_{12} = \frac{v_{out}^+}{v_{in}^-}\Big|v_{in=0}^+ \quad (19)$$

$$A_{21} = \frac{v_{out}^-}{v_{in}^+}\Big|v_{in=0}^- \quad (20)$$

$$A_{22} = \frac{v_{out}^-}{v_{in}^-}\Big|_{v_{in=0}^+} \quad (21)$$

2.5 Phase Margin

The phase margin given for an operational amplifier is the difference between the operational amplifier phase shift and -180 deg at the unity-gain frequency.

Phase margin of the VGA cell is described by formula (22),

$$\phi_M = 180° - \cot an(\frac{GBW}{f_{P_1}}) - \cot an(\frac{GBW}{f_{P_2}}) + \cot an(\frac{GBW}{f_Z}) \quad (22)$$

Where : f_{pi} is the frequency of the i-th pole, f_z is the zero fequency.

2.6 R_s and R_f implementation

2.6.1 R_s implementation

In this work, the source degeneration resistor$R_s$is implemented using the current conveyer techniques. The studied structure is used in [13,14,15] (figure 2), it is based on high linearity second generation topology, operating at low voltage low power environment. Currents mirrors (M_5, M_6) and (M_7, M_8) ensure current following between X and Z paths. Differentiel part of the curent conveyer structure ensures voltage following betwen Y and X nodes. C_1 and C_2 are used in order to improve frequency response and circuit stability. R_x and R_z impedances depend on bias current, supply voltage and transistors sizes, and can be described by formula (23) and (24).

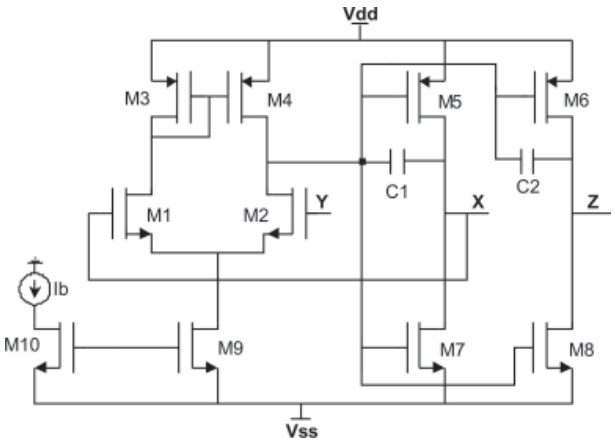

Figure 2: Low-voltage low-power current conveyors

$$R_x = \frac{1}{\frac{r_{05}+r_{07}}{r_{05}r_{07}} + g_{m1}\frac{r_{01}}{2}(g_{m7}+g_{m5})} \approx \approx \frac{2}{g_{m1}\frac{r_{01}}{2}(g_{m7}+g_{m5})} \quad (23)$$

$$R_Z = \frac{1}{g_{ds8}+g_{ds6}} \quad (24)$$

Expression 24 shows that $R_x$resistor variation depend on bias current I_b. Thus the circuit is a current conveyer CCII.R_x is considered a floating positive resistor controlled by the current and it is composed by two current conveyer CCII (figure 3).

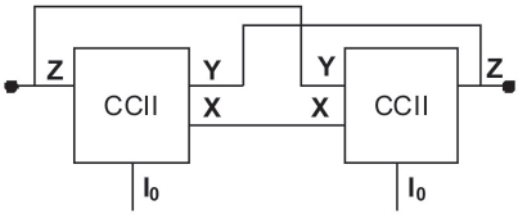

Figure 3: $R_s$architecture

2.6.2 $R_f$implementation

The feedback resistor $R_f$is implemented using two polycilicon resistor R_{f1} and R_{f2} [10]. It is demonstrated in [10] that R_f is used to determine the bandwidth of the VGA circuit. Figure 4 shows the used architecture for R_f implementation.

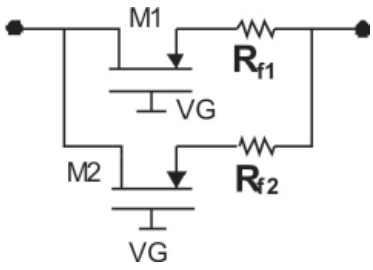

Figure 4: R_fArchitecture

3 VGA Circuit Optimization

In electronics fields, optimization helps designers to achieve best results. Optimization can be performed to transistors sizes, bias current, voltage and passive components.

3.1 Problem formulation

Solving an optimization problem consists to find a solution that minimizes or maximizes a particular criterion. In most cases, the optimum found is not unique. Thus there exist a set of solutions minimizing or maximizing the considered criterion. An optimization problem can be described as follows [16]:

Minimize $f(\vec{x})$: function to optimize

Subject to $\vec{g}(\vec{x}) \leq 0$: constraints to satisfy

Where $\vec{x} \in R^n$, $\vec{g}(\vec{x}) \in R^q$: *n* parameters

In this work, we are looking for optimizing the transistors sizes and the bias current of the VGA circuit. The optimization program is written in C++ language while considering steps listed below.

3.2 Optimization approach

The adopted optimization methodology is based on the following steps:

Constants initialization: μ_n, C_{ox}, V_{tn}, V_{tp}, Vdd, f_0, R_f and R_s. Parameters to optimize: transistors length: [0.35 µm, 0.45 µm], transistors width [1 µm, 800 µm] and bias current: [4 µA, 300 µA]

Model determination: VGA modelization is described in the previous section. Gain, noise figure, phase margin, linearity conditions and CMRR expressions are listed. These parameters represent the constrains of the algorithm where: Gain>20 dB, NF<25 dB, PM>45° and CMRR>100 dB.

Test vector generation (including bias current and transistos sizes).

Constraints verifications: if these constrains are verified the vector test represents a valid solution which can be used, if not another test vector will be generated.

Table 2: Ttransistors sizing after optimization

Transistors	W/L
M1a,b	4/0.35
M2a,b	30/0.35
M3a,b	10/0.35
M4a,b	90/0.35

The optimized value of the bias current is 5 µA.

3.3 Optimization results

After several iterations, many valid vectors test were obtained. The chosen solution is listed in table 2.

4 Simulation Results

The VGA cell is simulated using the Advanced Design System ADS tool with AMS 0.35 µm CMOS process parameters under ±0.75 V power supply. Current sources are implemented using cascode current mirrors. The bias current is set to 5 µA. The R_f and R_s resistors are implemented using architectures mentioned in section 2. Preliminary simulations of the VGA circuit shows that specifications needed for WiMAX standard are not satisfied especially in term of gain (simulated value of the gain = 25 dB << 72 dB = desired value). This problem can be solved by cascading several VGA cells. To attempt a gain of 72 dB, three VGA cells cascaded are required (figure 5).

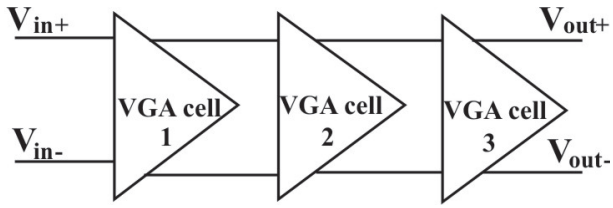

Figure 5: Overall VGA architecture

Simulations results for gain and noise figure are depicted in figures 6, 7, 8 and 9. High gain is obtained by maximizing R_f and minimizing R_s. Figure 6 shows that the maximum gain obtained by cascading three VGA cells is above 80 dB. R_f and R_s control allows to provide the gain necessary for mobile WiMAX application. The corresponding noise figure curve is shown in figure 7. Noise shown in figure 7 is equal to 19.83 dB which

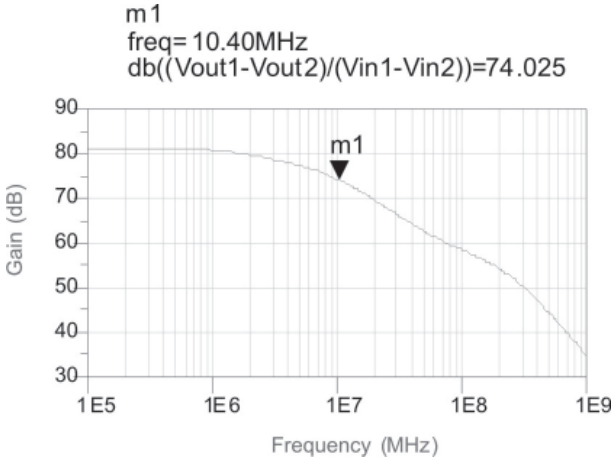

Figure 6: Max gain determination

comply with our application requirements. By adjusting R_f and R_s values, Graph 8 is obtained showing the minimum gain of three VGA cells which is around 25 dB. The corresponding noise is illustrated in figure 9 (21 dB). Bandwidth is maintained at 10 MHz for both max and min gain.

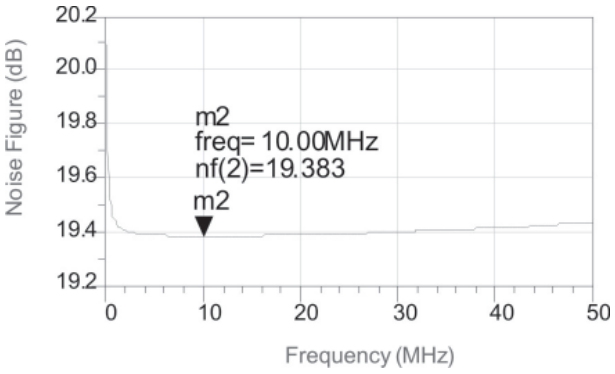

Figure 7: Noise figure determination for max gain

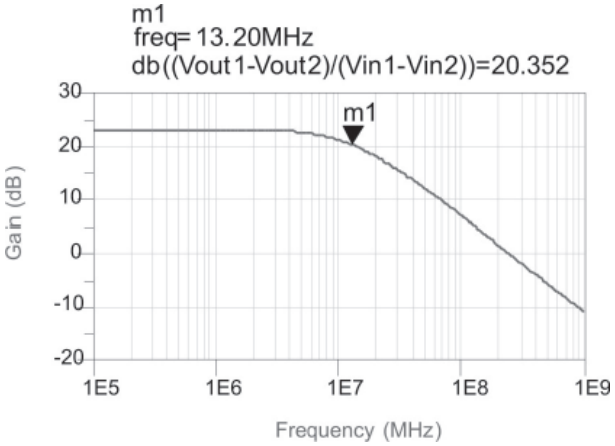

Figure 8: Min gain determination

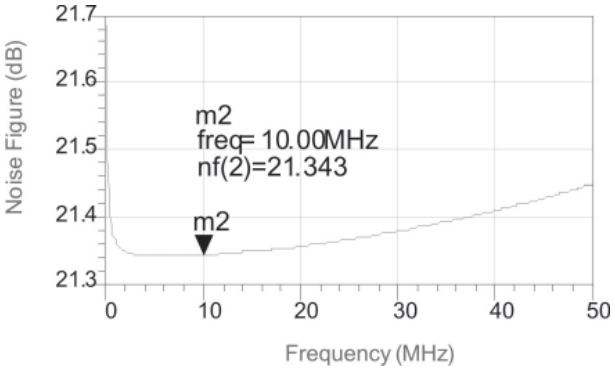

Figure 9: Noise figure determination for min gain

The simulated values of the PM and CMRR are presented in figures10 and 11. Figure 10 shows a CMRR equal to 81 dB at 10M Hz. A PM of 97.32 dB is obtained.

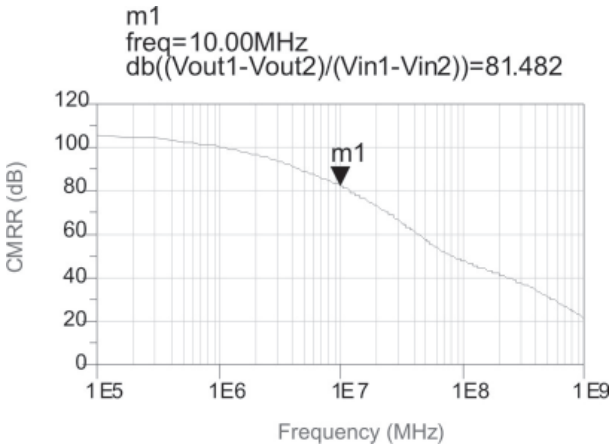

Figure 10: CMRR simulation

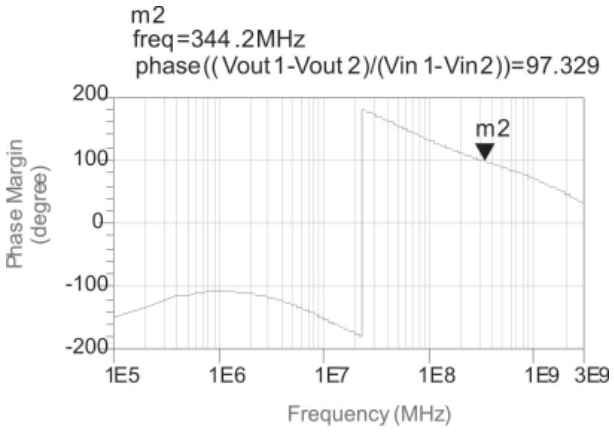

Figure 11: PM simulation

Figure 12 shows the ICP1 simulation curve. The ICP1 is equal to -15.5 dBm, so the IIP3 is around -5.5 dBm.

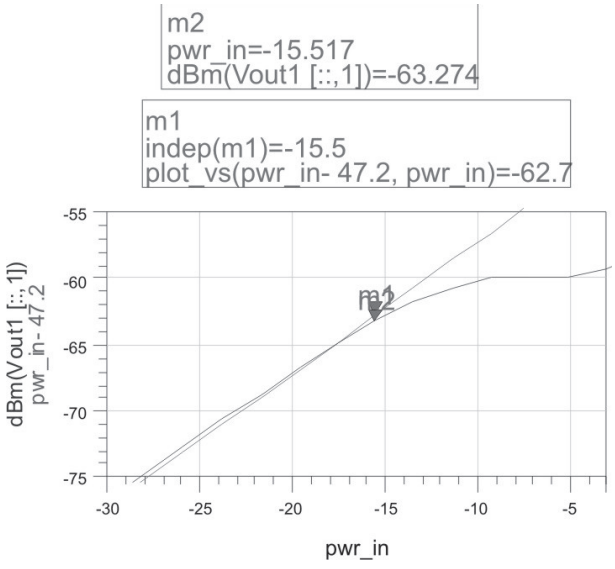

Figure 12: ICP1 simulation

Table 3: summarizes simulation results and a comparison with the standard specifications.

Table 3: Simulation results recapitulation

	Simulation Results	WiMAX Specifications
Supply Voltage	1.5 V	--
Gain range	20.35 dB@74.025 dB	21 dB@72 dB
Bandwidth (gain max)	10.40 MHz	10 MHz
Bandwidth (gain min)	13.20 MHz	10 MHz
NF (gain max)	19.383 dB	<20 dB
NF (gain min)	21.343 dB	<17 dB
IIP3	-5.5 dBm	18 dBm
Phase Margin	97 degré	>45
CMRR	81.49 dB	>100 dB--
Technology	CMOS 0.35 µm	--
Consumed Power	15 mW	--

Max gain is obtained for Rf=120 KΩ and Rs=1 KΩ, min gain is obtained while fixing Rf=30 KΩ and Rs=50 KΩ.

5 Conclusion

A variable gain amplifier designed for mobile WiMAX standard was presented. Device sizes and bias current conditions of the different blocks of the VGA are optimized for high gain, low noise and low power consumption. In order to attempt WiMAX requirements, three VGA cells were used and cascaded.The final circuit is designed in CMOS 0.35 µm AMS process technology. The simulation results showed a gain up to 74 dB,a minimum gain of 20 dB, a noise figure less than 21 dB, an input IIP3 above -3 dBm, a CMRR of 82 dB and a margin phase of 97 °. VGA circuit consumes power of 15 mW from a ±0,75 V supply voltage, however the current conveyer consumes only 1.5 mW. In future work we intend to improve VGA linearity by using a novel architecture.

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