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Modeling of Power Module for 48 V High Power Inverter

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Abstract: The paper presents simulation and measurement results of high current three-phase inverter power modules used in 48 V motor applications. Firstly, FEM (Finite Element Method) is used to extract circuit parasitics. With the inclusion of MOSFET and parasitic component SPICE models, a highly accurate simulation model is created. Switching characteristics of the power modules are simulated at 300 A load current and 48 V battery voltage. Thermal simulations estimate maximum transistor temperatures at given power losses. Electrical simulations are compared to actual measurements under identical test conditions. The comparison shows good matching between simulations and measurements. The phase voltage rise and fall times are the same in simulations and measurements. The overshoot voltages are also the same in both cases, at around 28 V. The mismatch can be found in the currents of secondary loops. The gate voltage signal is similar with small mismatch of Miller plateau voltage, due to transistor model parameters mismatch.

Keywords: power module; FEM analysis; thermal analysis; MOSFET

Modeliranje močnostnega modula za 48 V pretvornik visokih moči

Izvleček: Članek predstavlja načrtovanje, rezultate simulacij in meritev trifaznega močnostnega modula za velike tokove, ki je uporabljen pri 48 V motorskih pogonih. Najprej je uporabljena metoda končnih elementov (FEM) za izračun parazitnih elementov vezja. Z vključitvijo SPICE modela MOS tranzistorja in parazitnih elementov v model je nastal visokoločljivostni simulacijski model. Preklopne karakteristike so simulirane pri 300 A bremenskega toka in 48 V baterijske napetosti. Termične simulacije prikažejo največje temperature tranzistorja pri določenih močnostnih izgubah in nam podajo termično upornost tranzistorja do hladilnika. Narejena je tudi primerjava električnih simulacijskih rezultatov in dejanskih meritev, ki pokaže dobro ujemanje med njimi. Časa vzpona in padca fazne napetosti sta v primeru simulacij ter meritev enaka. Vrh preklopnega prenihaja je v obeh primeru enak 28 V. Slabše ujemanje je le pri sekundarnih tokokrogih, kjer se v simulacijah pojavi tudi rahli fazni zamik. Potek napetosti vrat je podoben, z manjšimi odstopanji napetosti Milerjevega platoja, zaradi odstopanja modela tranzistorja.

Ključne besede: močnostni modul; FEM analiza; termična analiza; MOSFET

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1 Introduction

Power modules are already well-known parts of all electric motor drives [1]. They work as an interface-inverter and supply the high current required for the operation of electric motors. The requirements for high voltages and high currents are constantly increasing, as high-power motors are needed for all sectors of industry, especially for transportation [2]. The demand for high voltage drives originated in battery-powered motor vehicles, where voltages reach 600 V and above [3]. Normal electric motor drives start at 12 V where automotive applications in vehicles use 12 V auxiliary drives to optimize vehicle performance [4]. The next interesting voltage level is 48 V, where it is the limit for low voltage systems. The parts of the 48 V system are inexpensive and the electrical architecture sits alongside the car's original 12 V system [5].

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The inverters for drives can use different switching electronic components such as silicon MOSFETs [6], SiC transistors [7], IGBT transistors [8], and so on. Each of these switching components has its own advantages and disadvantages. For the lower voltage domain where maximal voltage is 60 V, silicon MOSFET transistors are the right choice for a good price-performance ratio. One of the main issues, besides efficient driving of the inverter stage is also heat dissipation. The cooling system in motor drives can be of various types [9] and can further complicate the assembly and increase final system cost.

In the second chapter of the paper, the design of a 48 V three-phase motor drive, using MOSFETs as switching devices is presented. The third chapter presents power module modeling and parasitics extraction. It continues with thermal and electrical simulations. The paper concludes with the final chapter where a comparison is made between simulations and measured results performed on the prototype system.

2 Design of power module

2.1 Power module

A power module is a part of a three-phase (3P) 48 V Permanent Magnet Synchronous Motor (PMSM) inverter. It is designed to drive a motor with continuous power of 12 kW, maximum peak power of 20 kW and peak current of 600 Arms. Figure 1 shows the cross-section of a module mounted on a heat sink.

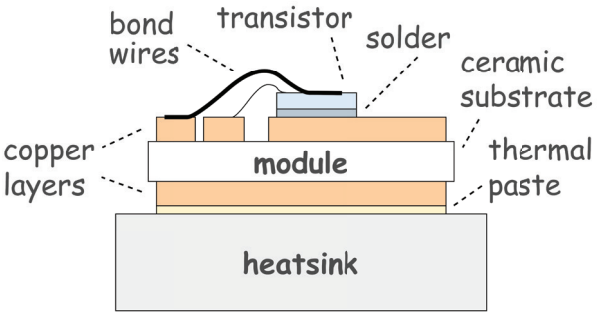

Figure 1: Power module cross section with all important elements annotated. Figure also represents module thermal structure.

Because of high currents and considerable power losses, the circuit is implemented on a ceramic substrate that gives the module a good heat conduction characteristic [10]. The ceramic substrate is a multilayer structure with a 500 µm thick Al_2O_3 (alumina) base and 300 µm copper plating on both sides. The bottom side of the ceramic module is attached to the heatsink via a thin thermal paste layer and additionally glued to the surface with nonconductive adhesive as shown in Figures 1 and 2.

In Figure 2, a gold-plated module is shown with bonded power transistors, capacitors and required gate resistors. High power switching is done by 100 V bare die MOSFET transistors in half-bridge configuration. For increased current carrying capability, four transistors are connected in parallel [14, 15]. Transistors are soldered to wide copper traces with their bottom side (drain) and are connected appropriately to other module connections by aluminum bonds from the top side (source).

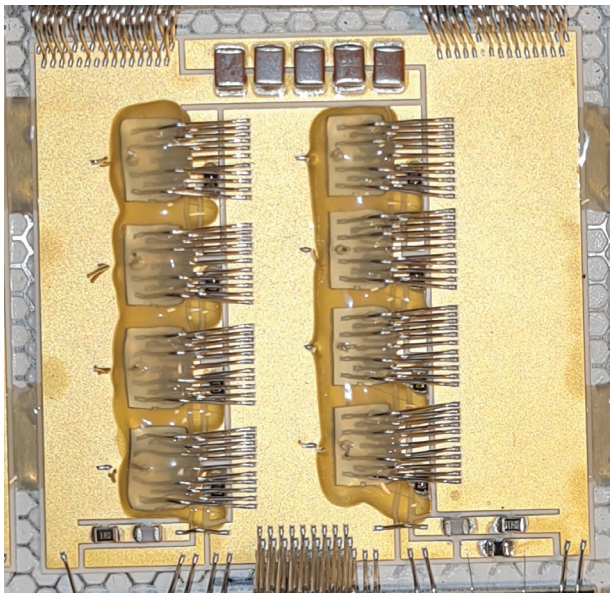

Figure 2: Module top view with 8 bonded transistors.

There are two types of bonds-main high current bonds with 380 µm diameter for source bonding and thin 50 µm gate signal bonds. Additionally, each transistor has its own individual gate resistor to minimize parasitic oscillations, provide the necessary damping and gate decoupling [15]. Module connections to other necessary circuits such as DC-link capacitor plate and driver module are also implemented using thick 380 µm bond wires. Any unwanted drain-source ringing is suppressed by RC snubbers, while onboard ceramic capacitors provide decoupling for high frequency switching transients [18]. An NTC thermistor is also mounted on the module board to monitor the temperature.

2.2 Layout

The board layout design enables three of the power modules to be placed side by side, forming a full 3P inverter power stage. The modules are connected to the power supply leads and capacitor plate on the upper side and

driver board from the bottom side of the 3P system. The capacitor plate is bolted to the busbar for an electrical connection to the power modules. Connections from battery terminals to capacitor plate are done from the top. Phases are connected from the bottom, where the motor is stationed. They are not included in Figure 3, as they can change with application. The geometric limits are the main constraint for power MOSFET placement and parasitics minimization as shown in Figure 3. For this reason, the MOSFETs are placed on rectangular baseplates, as this is the simplest and most intuitive solution, as already shown in Figure 2. The main parasitic components that most affect driver operation are inductances. They are minimized by reducing the loop sizes of the module current paths and maximizing the number of bond wires for all high-power interconnects [16].

The parasitic capacitances were not studied precisely as they are in the range of 10 pF to 100 pF, according to simulations, and do not affect the final module operation, as their value is much smaller than for instance MOSFET input capacitance, which is in the range of 10 nF. Moreover, adding parasitic capacitances in our case hardly affects the switching performance in the simulation. Therefore, the parasitic capacitances are considered as less important and are neglected; a similar approximation is also taken by other authors [17].

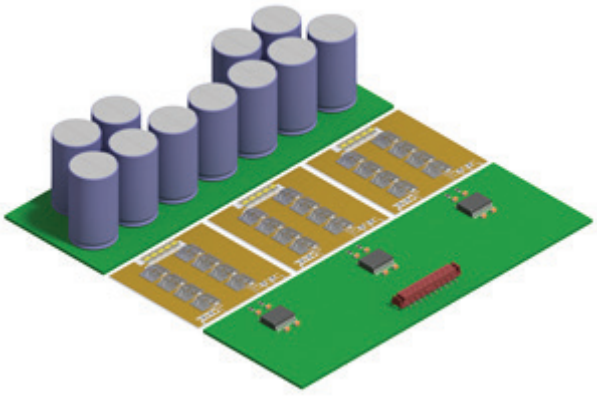

Figure 3: Proposed basic layout of the system (on upper side capacitor plate and at the bottom side controller plate). Connections to the battery and motor terminals are excluded from the image.

3 Simulations

3.1 Modeling

The power module is designed using Autodesk Inventor 3D CAD software. All details from the placement of the components to the shapes and connection geometries are modeled. Therefore, the used 3D model closely represents a real power module. The Ansys Q3D simulation software utilizes represented geometry model and extracts its parasitic circuit structure. The Ansys model is shown in Figure 4. For the simulation purposes, only parasitic resistances and inductances are extracted, capacitances are neglected. This parasitic circuit is used in combination with PSpice models of remaining module components to form a general level 3 [17] simulation model, used in Ansys Twin Builder. In addition to the module model, parasitic circuits of the driver and capacitor boards are also extracted and used.

The module is 47.5 mm wide and 46 mm long. The total 3P system is 103 mm wide. These are optimized dimensions that allow modularity and just enough room for transistor soldering and bonding. The width of the on-module connection traces for gate and electronic components connections are also optimized, not to influence the circuit performance. The typical trace width for the gate connection is 1 mm. Other connections are wider.

Figure 4 presents the Ansys model, including copper, bonds and solder pads, which all influence parasitic components. The MOSFET transistor die models are obtained from the manufacturer's packaged device electro-thermal model [19]. The original packaged device model is adapted by removing the package pins, internal bond wires and lead frame. Their resistances and inductances are removed from the model. Therefore, only the transistor die model remains.

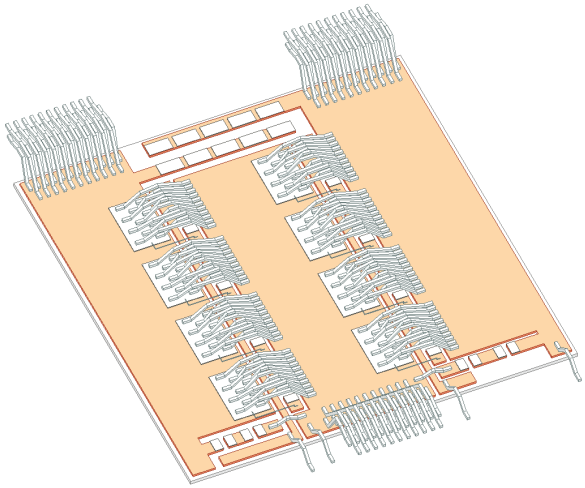

Figure 4: The Ansys Q3D module model, with all passive and active elements removed.

The thermal circuit of the bonds and lead frame are also removed so that the transistor can be simulated at constant junction temperature. The electrical behavior of the transistor is simulated in PSpice. Static and dynamic simulation results match the datasheet parameters.

Passive component parameters are obtained from the original manufacturer's Spice models, datasheets and some from similar measured components. Models for the module-mounted capacitors and DC link capacitors include series parasitic resistances, inductances and capacitances provided by manufacturers, while resistors are modeled as series RL circuits with typical package inductance values [17]. The transistor driver output stage is also obtained from the manufacturers PSpice model. In simulations performed, the gate driver peak currents match calculated values, therefore the gate driving circuit is correctly modeled.

3.2 Electrical simulations model

Parasitic circuit extraction is done at DC for the resistive part, so that circuit steady-state conditions are modeled correctly. Higher frequencies are used for inductive part extraction, so that a good approximation for fast switching transients is obtained [17]. Typical extracted values of parasitics are shown in Table 1.

Table 1: Typical self-inductances.

Lsl, Lsh	5 nH
Ldl, Ldh	2.5 nH
Lcap-, Lcap+	15 nH
Lcer	0.6 nH
Lel	7.5 nH
Lcable-, Lcable+	300 nH

The labels used in Table 1 correspond to the elements drawn in Figure 5. The parasitic extraction also calculates mutual coupling. The method firstly removes all active or passive soldered components from the model, so only basic metallic structure remains (see Fig. 4). To each net, a common sink connection is assigned, like a common surface at the *Vbat+* or *Vbat-* bonds. Nodes of transistors, capacitors and resistors are presented as sources. Together they form a net of connections with different parameters. For each separated connection in the net, Ansys Q3D calculates individual and coupled parasitic parts. Coupled inductances are also calculated between source-sink pairs of different nets. The frequency at which parasitic inductances are extracted is experimentally determined and corresponds to the highest signal frequency used in the circuit. The final result is obtained using frequency at which matching between measurements and simulation is highest. Initial simulations were done using the frequencies in the range of a few MHz [11], meaning typical switching times for MOSFET transistors [12] (see Fig. 9 and 10). The calculated inductances in this case are too small and the initial voltage overshoot is almost not visible. Decreasing the frequency in range of a few 10 kHz increases matching between the two results. The parasitic matrix, formed by Ansys is not presented as it includes a lot of nodes and does not clearly represent the parasitic mesh. The sum of important inductances is presented in Table 1.

Electrical simulations are focused on the inverter switching transients. For basic simulation, a simplified inverter model version is used. A 3P inverter is simplified to a single half-bridge power module. With this simplification, the simulation accuracy is not affected [13], but the total simulation time is considerably shortened. The DC capacitor plate and driver board parasitic models are fully included, as they were already designed and extracted separately for each phase.

The double pulse test (DPT) is used for simulation [13]. The DPT is a well-known test where the upper transistors of the inverter are turned off and the bottom transistors are driven by two pulses of different lengths. The expected load is connected to the output. Current value and the transient behavior are observed, subjecting transistors to worst case operating conditions without the need for prolonged simulations.

The circuit is simulated at 48 V battery voltage, motor load current of 300 A_{rms} and 25 °C transistor temperature. Bottom transistor gates are connected to gate driver driven by a voltage source. Top transistors are connected in body diode configuration, meaning in the off state. The simulation schematic is shown in Figure 5.

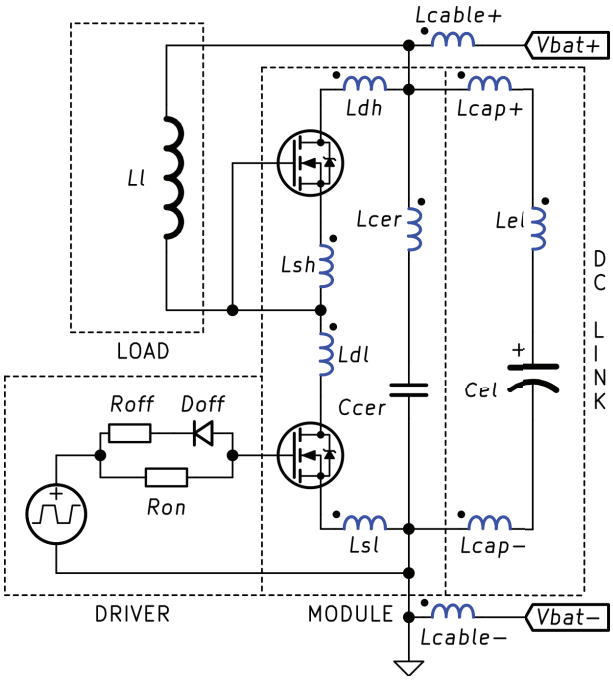

Figure 5: Simplified simulation schematics.

All parasitic inductances in the circuit are marked with a blue inductor symbol and dot showing the relative magnetic field polarity for mutual coupling. Their values are presented in Table 1. As can be noticed, also inductance of cables and bonds are considered. The inductive load is connected from the middle point (phase connection) to the positive battery connection. The simulation results are shown and discussed the in simulation-measurement comparison chapter.

3.3 Thermal simulations

The ceramic power module is placed on the 10 mm thick aluminum plate, serving as a cooler, with thermal conductivity of 237.5 W/mK. The 100 µm thick interface material is thermal paste with thermal conductivity of 2.5 W/mK. Copper and alumina (Al2O3) thermal conductivities are 394 W/mK and 24 W/mK, respectively. The thermal model of solder and transistor consists of two blocks with thicknesses of 100 µm and 220 µm stacked one on top of another. Their thermal conductivities are 63 W/mK for solder and 130 W/mK for silicon MOSFETs [12].

With such a power module model, the thermal simulations are performed, using Ansys Icepack program. The simulation result is shown in Figure 6, where thermal conditions are presented in the top view using a temperature scale on the left.

The aluminum plate bottom surface is maintained at a constant temperature of 65 °C. Module maximal temperature of 85 °C is reached in the middle of transistors where cooling is least effective.

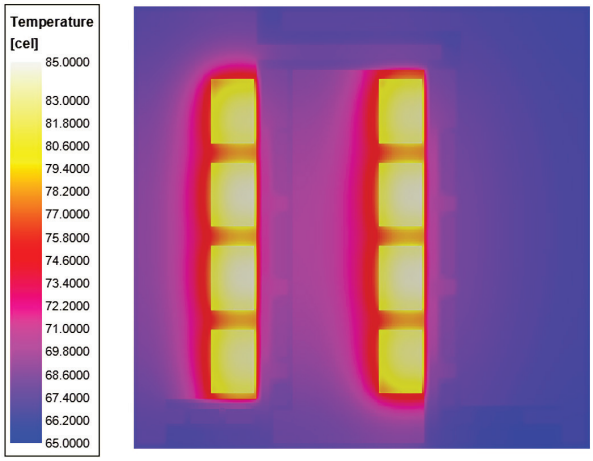

Figure 6: Module temperature conditions simulated in Ansys Icepack. Total module power loss is 200 W or 25 W per transistor.

The system thermal resistance R_{th} can be determined by the equation:

$$R_{th} = (T - 65°\mathrm{C}) / P \quad (1)$$

where T is maximum transistor temperature and P is module power loss. Calculated R_{th} at several power conditions is shown in Table 2.

Table 2: Maximum transistor temperature in relation to dissipated power.

P [W]	100	150	200	250	300	350
T [°C]	74.3	79.0	83.7	88.4	93.0	98.0
Rth [K/W]	0.093	0.093	0.094	0.094	0.093	0.094

As can be seen in Table 2, the temperature linearly depends on the power dissipated, under given conditions. The thermal resistance is constant 93 mK/W. The temperature values reached are not critical; simulated dissipation on the module is around 200 W at 300 A current (transistor channel resistance is 1.7 mΩ, typically).

The obtained thermal data can be used in a heatsink design, which must be carefully adapted due to power loss data from electrical simulations.

Basic thermal measurements are also performed. The module is measured in the saturation region with constant current and voltage, so that the losses applied are more accurate. Measuring module losses while under real load would be difficult. Temperature is measured using two thermocouples, one fixed in the middle of the module and another 0.5 cm away from the edge, directly on the heatsink.

At the 100 W load, the measured temperature difference is 6 °C, which corresponds to the 0.06 K/W thermal resistance between the heatsink and the module. In a simulation, the middle of the module is heated to about 71.5 °C giving us thermal resistance of 0.03 K/W. The difference between the simulation and measurements can be attributed to several factors. After the module inspection, imperfectly applied thermal paste is thought to be the main cause for the difference.

4 Measurements

For the prototype measurements, a single phase module is tested, using an artificial load. The driver was designed and assembled by us and is capable of driving several different kinds of power transistors. In Figure 7 the measurement setup is presented. Setup includes Tektronix MDO4054C oscilloscope and TPP0500B probes for voltage waveform capturing. The load current is measured by the CWT1 Ultra-mini Rogowski current transducer. The Agilent 33500B is connected as a

double pulse generator to control low side transistors. The EA-PS 9080-60 T laboratory power supply generates 48 V for high power switching circuit, other low voltages needed for a driver board are generated using the GWinstek GPD-3303S DC source.

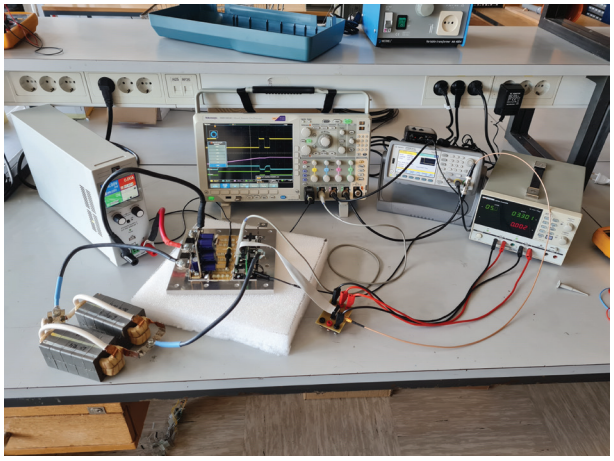

Figure 7: Measurement setup.

The signal generator was manually triggered. At trigger, a gate driver enables low side transistors for 500 us to energize the load coil and the current to reach 300 A. Then the bottom transistor is turned off for 25 µs, and again turned on for another 25 µs. Transistor turn-on and turn-off transients are measured during switching. They are measured directly on transistors. The typical signal curves and measurements results are shown in Figure 8. In Figure 8, on the first top trace, voltage drop on the fourth transistor channel from the module low side can be seen. This transistor is farthest from the power distribution and it suffers from the high parasitic influence on its behavior. Due to that fact, the transients on this transistor are high and greatly expressed. At the first turn on, there are no overshoots due to no current present, but when transistor is turned off, the

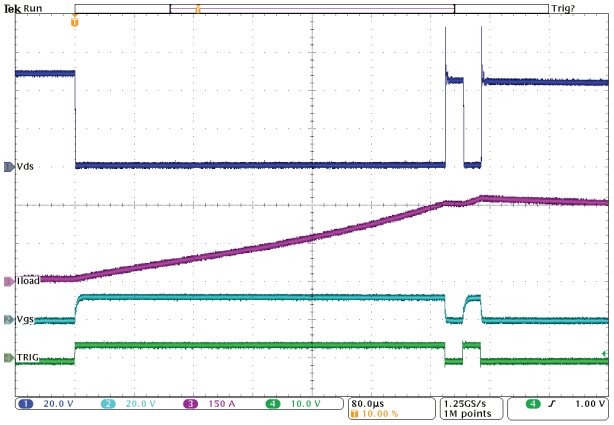

Figure 8: Measurement results - V_{ds} of the fourth transistor, load current, V_{gs} and double pulse trigger as the last waveform.

spikes and "ringing" can be detected. In the next trace, the current through the load is shown. After turn on, current linearly rises up to 300 A and then drops for a bit in off time and then again rises for another 30 A on the second turn on, yields final 330 A of current. The third trace presents V_{gs} signal – transistor control signal with rounded pulse shape in transients – typical RC shape, influenced by the gate resistor and the transistor's C_{gs}. Also, the different shapes and duration of a rise and fall time can be observed. This is due to the different current driving defined by R_{on} and R_{off}. The last trace presents the generator pulse on circuit input.

5 Comparison

In this chapter, simulation and measurement results are presented and discussed. All results shown are valid for the fourth bottom transistor as it is one of the active devices in DPT. The time scales of the top and bottom subgraphs in Figures 9 and 10 are aligned. In Figure 9, V_{gs} and V_{ds} transitions are shown, at full load of 300 A. Figure 9 in the top window, presents the transition of the V_{ds} voltage when the transistor switches on. There are no deviations between simulated (dashed line) and measured results – the voltage drops from 48 V to approx. 0.55 V in 0.8 µs. The V_{gs} transition in the bottom window is not so smooth due to the parasitic capaci-

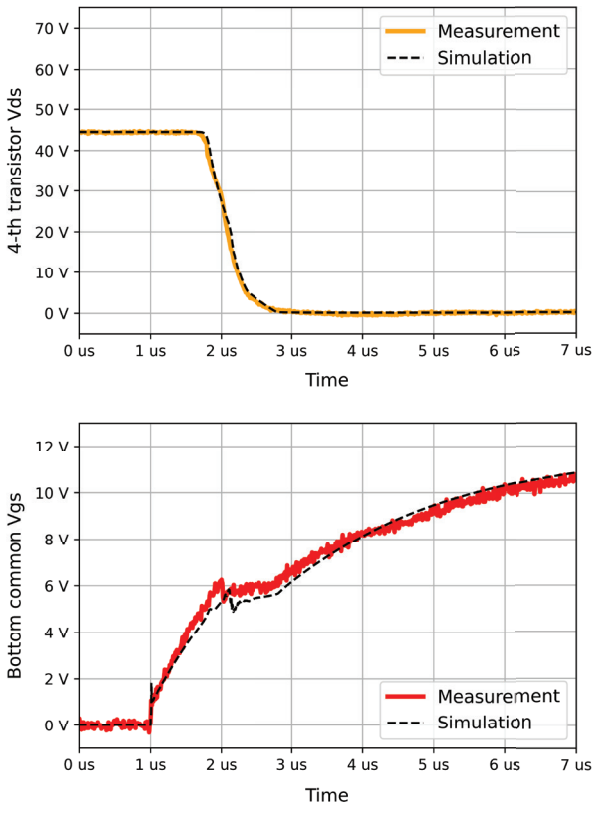

Figure 9: Comparison of V_{ds} and V_{gs} results at turn-on.

tances, and it consists of three parts. First, the voltage V_{gs} starts to rise and when a threshold V_{th} is reached, V_{ds} starts to discharge C_{gd} into the gate. This is the time when V_{gs} is constant in the middle of the rise transition – it is called Muller plateau. When the gate capacitance C_{gd} is fully discharged and the V_{ds} is almost zero the V_{gs} continues its rising to the full value. There is a small discrepancy between simulation and measurement – the Muller plateau is a bit higher, which means that a threshold value is a bit different in simulation; nevertheless, its duration is the same that means the capacitances in the model are correct. Also, C_{gd} is a nonlinear function of V_{ds}, but in this case V_{ds} was the same for the simulation and for the measurement.

Figure 10 presents the same two voltages at the turn off moment. At that time when 300 A current is flowing through the load and transistors, the loop is disconnected. It must be emphasized that this transition is done with a different gate current value, due to the changed gate resistance. The current is higher and turn off occurs faster. We start at the bottom graph, where V_{gs} is presented.

After a 1 µs delay, the V_{gs} is turned off. As can be noticed it starts to fall quickly – discharging the C_{gs}, till Muller plateau is reached. Then the C_{ds} starts to discharge and when discharge is done, the transistor is turned off. The

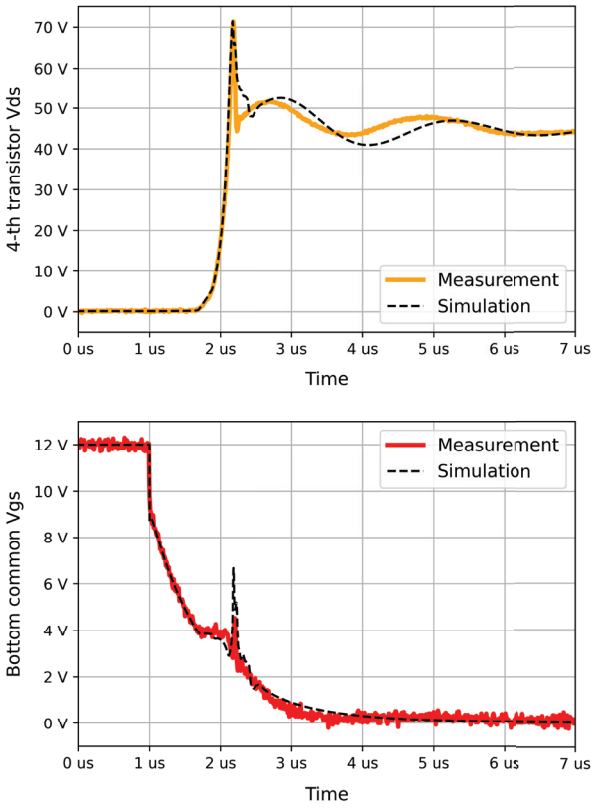

Figure 10: Measured and simulated waveforms compared. Turn-off at 300 A load current.

transient continues until C_{gs} is not discharged completely. The voltage V_{ds} jumps to 48 V at the moment, when C_{ds} is discharged, causing overshoot due to the huge amount of energy in the load and additional parasitic inductances of the system. The initial voltage overshot is suppressed by the DC capacitors mounted on the power module top side. After 28 V overshot, small oscillations can appear which are suppressed with the onboard snubber circuit. There is a bit difference in the simulated and the measured signal curve. The measured curve sharply declines, but the simulation shows a slight hump. Different parasitic inductances variations result in just a small shortening of the hump. Changes to transistor parameters also change waveforms. Usage of AC parasitic resistances instead of DC, decreases the hump but also lowers the initial spike. The lower frequency oscillations, after the overshot, are caused by the energy exchange between ceramic capacitors on the module and electrolytic capacitors placed on a bit remote board. The oscillations can be found also in the simulation results. The signal frequency and amplitude are almost the same.

From the results obtained, it can be concluded that the inductances and capacitances of the module were modeled correctly.

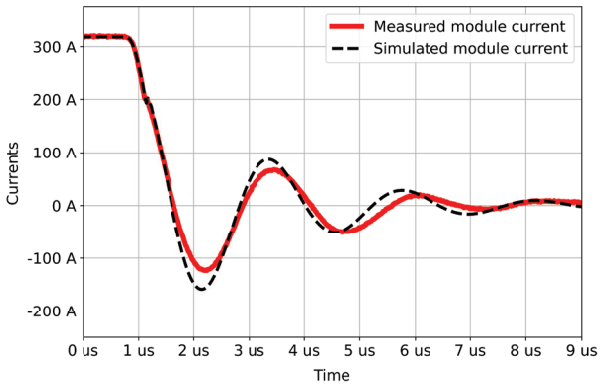

Figure 11: The $I_{Zdh} - I_{ce}$ current.

One of the interesting curves to observe is a total current from the module positive connection, shown in Figure 11. It can be noticed that at the turn-off moment, the transition is smooth. The overshoot in negative current is approximately 1/3 of the "ON" current and it matches well with the simulations. We can say that simulations predict a bit worse result as it is measured. The energy flow can be easiest presented with comparison of three main currents, shown in Figure 12.

It can be found that when the transistor is switched off, the necessary current deficit for the load comes from ceramic capacitors mounted on the module, and therefore satisfy the inductance request for slow current flow change. The oscillations then appear between different capacitors.

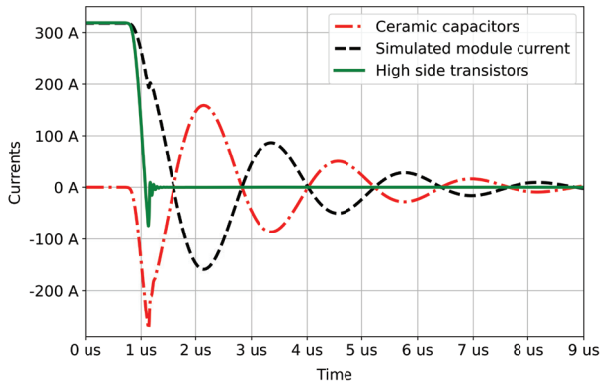

Figure 12: Current values at the on-off transition of module positive terminal, ceramic capacitors and transistors.

6 Conclusion

In the paper, power module design used in a high power motor inverter was presented. The main issue of the design flow is how to minimize parasitic components and include them correctly in the model to perform reliable simulations, which reflect in the correct system operation. The modeling chapter summarized the main steps for modeling and optimization of the model and minimization of parasitic components in a real board. The measurement setup presented main equipment used and explained the DPT test. The last chapter presented a comparison of measured and simulated results, which shows good main curve alignment and confirms values calculated and used in the inverter model. Both simulation and measurements give identical overshoot results of 28V. Small divination can be noticed only during secondary oscillations between different capacitors on the module and DC link caps. A gate-source voltage prediction mismatch only by a small amount due to MOSFET model inaccuracy. A presented model also gives good insight into circuit conditions that cannot be measured due to physical constraints.

7 Acknowledgments

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8 Conflict of interest

The authors confirm there are no conflicts of interests in connection to the work presented.

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