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Charge Pump Using Gain-Boosting and Positive Feedback Techniques in 180-nm Digital CMOS Process

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Abstract: The charge pump (CP) circuit is an essential element in a delay-locked loop (DLL). This paper proposes a new CP using gain-boosting technique. Two possible solutions for gain-boosting circuit implementation are presented. One solution is based on common-source amplifier. In another solution, positive feedback method is employed at the output stage to increase the output resistance of the amplifier. Therefore, DC-gain of the amplifier is improved. In addition, nonlinear current mirror is employed in which the gain is dependent to the input current. To evaluate the performance of the proposed CPs, simulations are done in a 0.18 µm CMOS process with the supply voltage of 1.8 V. The simulation results indicate that the proposed CPs can obtain good current matching characteristics in the low power applications. The mismatch between up and down CP currents is less than 1%.

Keywords: Charge pump; Common-source amplifier; Gain-boosting; Positive feedback; Nonlinear current mirror

Črpalka naboja z uporabo tehnik povečanja ojačanja in pozitivne povratne zveze v 180-nm digitalnem procesu CMOS

Izvleček: Vezje črpalke naboja (CP) je bistven element v zanki z zakasnitvijo (DLL). Ta članek predlaga novo CP s tehniko povečanja ojačenja. Predstavljeni sta dve možni rešitvi za izvedbo vezja za povečanje ojačenja. Ena rešitev temelji na ojačevalniku skupnega vira. Pri drugi rešitvi je na izhodni stopnji uporabljena metoda pozitivne povratne zveze za povečanje izhodne upornosti ojačevalnika. Zato se izboljša enosmerno ojačanje ojačevalnika. Poleg tega je uporabljeno nelinearno tokovno zrcalo, pri katerem je ojačenje odvisno od vhodnega toka. Da bi ocenili delovanje predlaganih ojačevalnikov, so simulacije izvedene v 0,18 µm procesu CMOS z napajalno napetostjo 1,8 V. Rezultati simulacij kažejo, da lahko predlagani ojačevalniki dosežejo dobre karakteristike tokovnega ujemanja v nizkoenergijskih aplikacijah. Neskladje med tokovi CP navzgor in navzdol je manjše od 1 %.

Ključne besede: črpalka naboja; ojačevalnik s skupnim virom; povečanje ojačenja; pozitivne povratna zanka; nelinearno tokovno ogledalo

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1 Introduction

Phase-locked loops (PLL) and delay-locked loops (DLL) have been widely employed for clock synchronization applications. Nowadays, the DLL can be used for synchronization, clock generation, and digital transceivers in serial links [1-3]. Several problems should be considered for designing the high-performance DLL. To increase the input frequency range of the DLL, the precision of the phase detector (PD), the matching between the up and down charge pump (CP) currents, and the

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delay cells bandwidth requirement in a voltage-controlled delay line (VCDL) should be regarded [4-5]. By increasing the input frequency, the phase resolution is limited by the phase offset of the PD. The current mismatch between the up and down signal may lead to static phase error between the input and output clocks [6-10]. Increasing the number of the delay cells or the input clock frequency will result in harmonic-locked problem provided that the total intrinsic delay is greater than the period of the input clock.

Several methods for designing CP have been suggested in the literatures [11-19]. A conventional CMOS CP circuit consists of UP and DN switches made by PMOS and NMOS transistors, respectively. This method suffers from current mismatch between Up and Down paths. It is due to the different output impedances of PMOS and NMOS transistors [11]. Some ideas have been suggested to overcome the shortcoming of the basic CP. In [12], it is shown that by employing of dummy devices and dummy loads, current mismatch can be reduced significantly. In another method, cascade topology is utilized to reduce current mismatch and reference spurs [13]. It is indicated that operational amplifiers (op-amps) as a unity gain amplifier can be successful in alleviating the current mismatch [14]. Another design method proposed in [15] reduces the output current glitch by canceling the spurious jump phenomenon.

In [16], the CP circuit performance in terms of current matching is improved by the operational trans-conductance amplifier (OTA). The mismatch between I_{ch} (charge current) and I_{dis} (discharge current) of the CP circuit is reduced significantly. But, current variation is not considered in this method. It is shown that I_{ch} and I_{dis} are dependent on output voltage variation. Therefore, CP-PLLs stability and transient response may be affected [17]. In another method [18], the gain-boosting technique is proposed to increase the output impedance of the CP circuit. In this method, the output current will remain more constant and the result indicates good current matching characteristic. In addition, using the bulk-driven method, the output voltage swing is improved while the power dissipation (Pdiss) is reduced. In [19], the gain-boosting is used to increase the output impedance of the CP as well as a low-voltage cascode current mirror is used to enhance its current matching. The low-voltage cascode current mirror is used to copy I_{ch} and I_{dis} from a single current source to ensure that both current values are equal.

Some techniques have been developed to reduce the power consumption and increase the power efficiency of the CP circuits. In [20], To improve the charge transfer characteristic a feedback loop is utilized. In [21], a CP is introduced based on a four-phase clock and boost capacitors on the switch transistors which eliminates the influence of threshold voltage of the transistor. In [22], an optimized method is suggested that relies on the determination of the optimal stage number to minimize the power consumption. In [23], the charge sharing method is employed for a four-phase charge pump to enhance the power efficiency. The technique in [24], which combines the charge sharing technique with multi-step capacitor charging can alleviate the overall power consumption compared to the conventional four-phase CP and also the charge sharing based CP.

In this paper, a new CP is proposed using the gain-boosting technique. Two circuit implementations of the gain-boosting are presented. One implementation is based on a common-source amplifier, and the other is based on a positive feedback amplifier. In addition, nonlinear current mirror with gain dependent on the input current is utilized for the proposed CP. The results indicate the superiority of the proposed technique in terms of current matching compared to the existing methods. In Section 2, the proposed CP is described. The performance evaluations of the CP and comparison results are provided in Section 3. Finally, Section 4 concludes the paper.

2 Proposed CPs

In this Section, two CPs using the gain-boosting techniques are presented. The designing details are provided as follows.

2.1 Common-source amplifier based CP

Figure 1 shows the circuit configuration of the proposed CP using the gain-boosting technique. In this circuit, M_1 and M_2 are the current sources. Up and Down controlled switches are implemented by M_4 and M_3, respectively. (M_5, $M_{7)}$ and (M_6, M_8) form the gain-boosting loop where M_7 and M_8 works as a common-source amplifier. M_9 to M_{14} are current mirror transistors. M_{15} acts as reference current generator. The output impedance can be described as follows:

$$R_{out} = (g_{m5}r_{o5}g_{m3}r_{o3}r_{o1})(g_{m7}r_{o7}) \,\|\, (g_{m6}r_{o6}g_{m4}r_{o4}r_{o2})(g_{m8}r_{o8}) \qquad (1)$$

In the above equations, g_m and r_o denote the trans-conductance of the transistor and the drain-source resistor of the related transistor, respectively.

Nonlinear current mirrors based on flipped voltage follower (FVF) [25-27] have been used for the output active loads made by transistor sets (M_9, M_{10}, $M_{11)}$ and (M_{12}, M_{13}, M_{14}). The nonlinearity of the current mirrors results in the

desired output current boosting. The current mirrors are used to ensure that I_{UP} and I_{DOWN} currents are equal.

If V_{b1} is chosen to bias M_{10} in the triode region, the following equations are obtained:

$$I_9 = \frac{1}{2}\beta_9 V_{od9}^2 \tag{2}$$

$$I_{10} = \beta_{10} V_{od10} V_{DS10} \tag{3}$$

where $\beta=\mu_n C_{ox} W/L$ and V_{od} represents the overdrive voltage of the transistor. It should be mentioned that μ_n, C_{ox}, W and L are electron mobility, gate-channel capacitance density, transistor channel width, and transistor channel length, respectively. Assuming $\beta_9=\beta_{10}$ and using equations (2) and (3), we have:

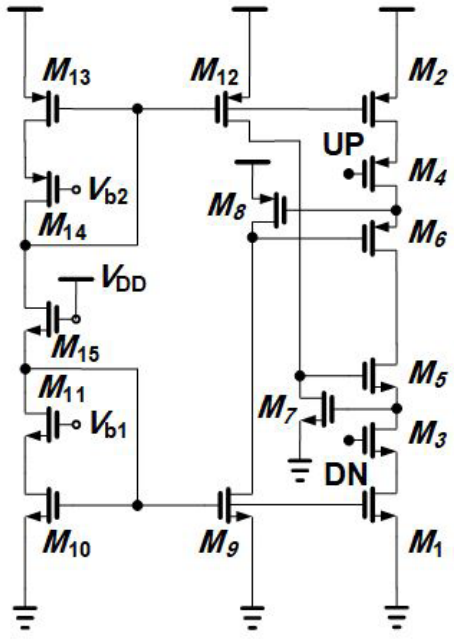


Figure 1: The first proposed CP.

$$I_9 = \frac{I_{10}^2}{2\beta_9 V_{DS10}^2} \tag{4}$$

Since $V_{DS10}=V_{b1}-V_{tn}-V_{od11}$ (V_{tn} is the threshold voltage), I_9 is given as below:

$$I_9 = \frac{I_{10}^2}{2\beta_9 (V_{b1} - V_{tn} - \sqrt{\frac{2I_{10}}{\beta_{11}}})^2} \tag{5}$$

As can be seen from (5), a nonlinear relation exists between I_9 and I_{10}. It is worth to mention that biasing M_{10} in the saturation region leads to the obtaining conventional linear current mirror.

2.2 Positive feedback based CP

The OTAs are used in many applications such as high-resolution ADCs and DACs, and sample-and-hold amplifiers (SHAs) [25-30]. Figure 2 shows another possible solution for the CP in which the gain-boosting circuit implementation is performed by the OTA. The proposed OTA to provide higher DC-gain compared to the common-source amplifier is shown in Figure 3.

In the proposed OTA, the transistors (M_{1a}, M_{1b}, M_{2a}, M_{2b}, M_{3a}, M_{3b}) constitute a flipped voltage follower (FVF) [25-27] to bias the input differential pairs. Input signals are applied to the split transistor sets (M_{4a}, M_{4b}) and (M_{4c}, M_{4d}) which have the same aspect ratio. Consider a situation in which V_{in+} and V_{in-} increases and decreases, respectively. Thus, the source-gate voltages of the (M_{4a}, M_{4b}) and (M_{4c}, M_{4d}) decrease and increase, respectively.

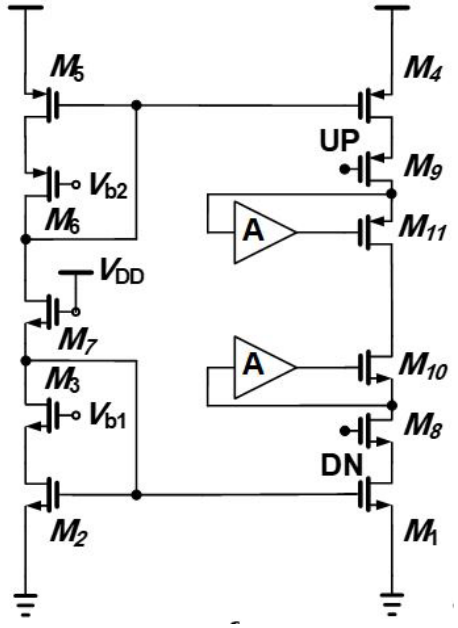


Figure 2: The second proposed CP.

Therefore, the current through them decrease and increase, respectively. M_5 and M_6 are used as common-gate transistors. M_7 to M_{10} are active load transistors of the common-gate transistors. M_{11} to M_{14} act as improved recycling structure (IRS) [30]. The IRS technique presents different paths for DC and AC currents, which results in enhancing the trans-conductance. By applying the output signal V_{out+} to the bulk terminal of M_5 and V_{out-} to the bulk terminal of M_6, a positive feedback loop is created. In order to control the gain of the feedback loop and also avoiding instability, the resistors (R_1, $R_{2)}$ and (R_3, R_4) are used. The resistor sets work as the voltage divider. The division factor is defined as below:

$$k = \frac{R_2}{R_1 + R_2} \tag{6}$$

The DC-gain of the OTA is explained as:

$$A_d = G_{meff\,1} R_{out} \tag{7}$$

The G_{meff1} is calculated in [25] as below:

$$G_{meff\,1} = g_{m\,4a}(1+\alpha_1) + g_{m\,9} \tag{8}$$

where $\alpha_1 = g_{m13a}/g_{m13b}$ means that M_{13a} aspect ratio is α_1 times greater than that of M13b.

In order to derive the output resistance of the OTA, the equivalent resistance from the drain of M_5 should be determined (see Figure 4).

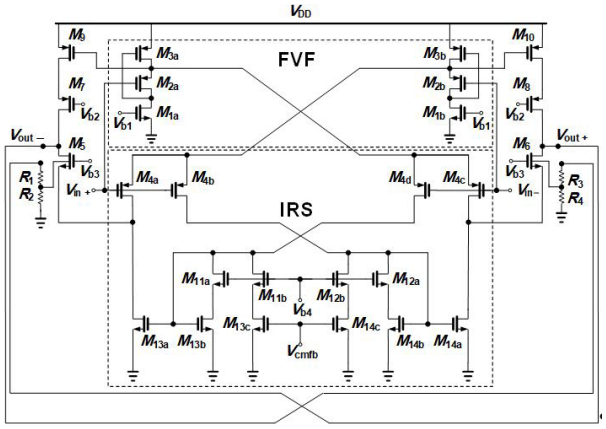


Figure 3: The proposed OTA.

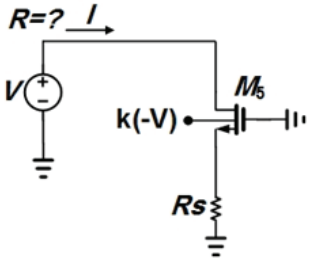


Figure 4: Model to calculate the equivalent resistance from the drain. of M_5.

$$R = \frac{V}{I} = \frac{r_{o5} + g_{m5} r_{o5} R_s + R_s}{1 - g_{mb5} k r_{o5}} \tag{9}$$

Therefore, the R_{out} is defined as follows:

$$\begin{aligned} R_{out} &= [g_{m7} r_{o7} r_{o9} \,\|\, \mathrm{R}] \\ &= [g_{m7} r_{o7} r_{o9} \,\|\, \frac{r_{o5} + g_{m5} r_{o5} R_s + R_s}{1 - g_{mb5} k r_{o5}}] \end{aligned} \tag{10}$$

In the above equations, R_{out} is the output resistance of the OTA and $R_s = r_{o4a} \| r_{o13a}$. Moreover, g_{mb5} denotes the trans-conductance of the bulk-driven transistor M_5 that represents the body effect. Using the positive feedback, the output resistance can be increased. If the denominator of equation (9) is chosen so that $1\text{-}g_{mb5}k\text{-}r_{o5}>0$, close to zero, then the differential voltage gain is enhanced significantly, and the circuit is stable.

It is worth to mention that the dominant pole is determined by the output resistance and capacitive load as follows:

$$\omega_{p1} = \frac{1}{R_{out} C_L} \tag{11}$$

Equation (11) reveals that the positive feedback technique moves the dominant pole to the lower frequency.

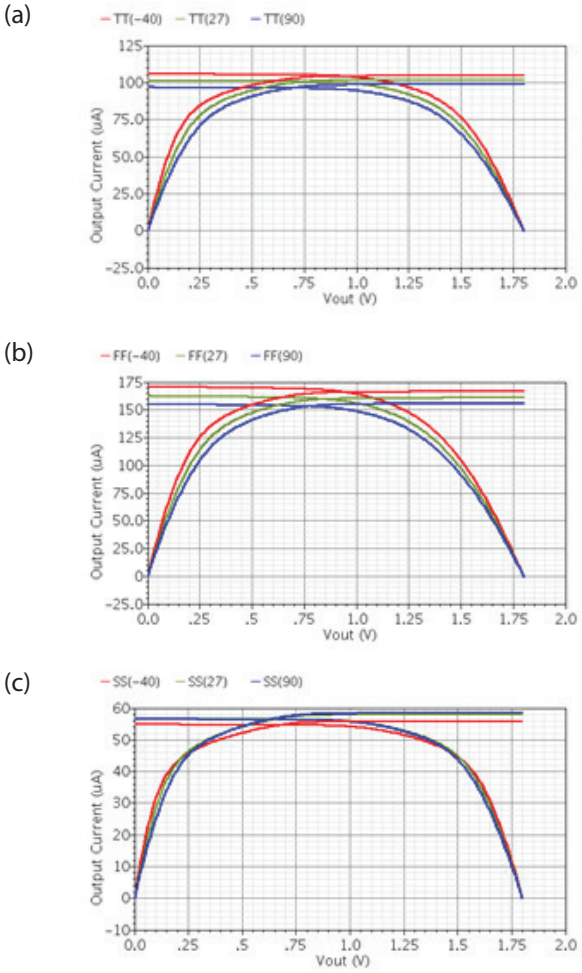


Figure 5: Charge and discharge current output versus the output voltage of the first proposed CP in the process and temperature corners: (a) TT(-40°C), TT(27°C), TT(90°C), (b) FF(-40°C), FF(27°C), FF(90°C), (c) SS(-40°C), SS(27°C), SS(90°C).

3 Simulation Results

In order to verify the performance of the proposed CPs, some simulations are performed. Both of the CPs are designed in a 0.18 µm CMOS process with 1.8V supply voltage using Cadence software. Figure 5 shows the charge and discharge current output versus the output voltage of the first proposed CP circuit in process and temperature corners. The CP current is about 100 µA, and the mismatch between I_{UP} and I_{DOWN} is less than 1% over the output voltage dynamic range from 0.2V to 1.79V, which covers 88% of the 1.8V supply voltage. Layout of the first proposed CP is shown in Figure 6 in which the layout area is 12µm×18µm.

The Bode diagrams of the proposed OTA using the positive feedback technique are shown in Figure 7. As can be seen from the Figure 7, the proposed OTA exhibits 79 dB DC-gain. UGBW and phase margin of the proposed OTA are 160 MHz and 75^0, respectively. The phase margin shows that the OTA is stable. In order to the slew rate (SR) calculation, a square wave, 1 Vpp at 5 MHz was applied to the OTA, and the result is shown in Figure 8. The OTA specifications along with a comparison to the existing methods are summarized in Table 1. As seen from the results, the proposed OTA has the highest DC-gain, at least 9 dB more than the other methods. In addition, the proposed OTA has high values for both figure of merits (FOMs).

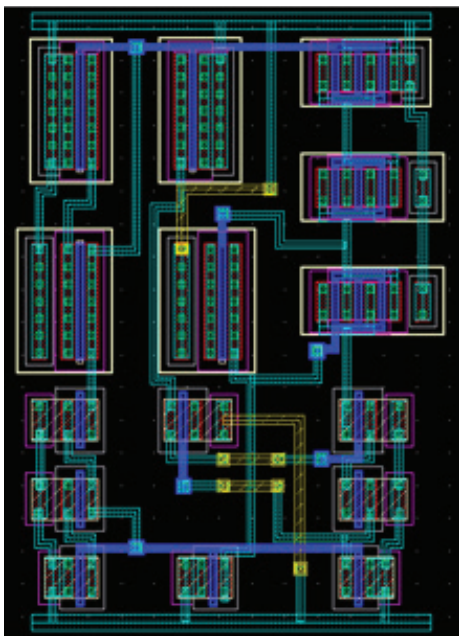


Figure 6: Layout of the first proposed CP.

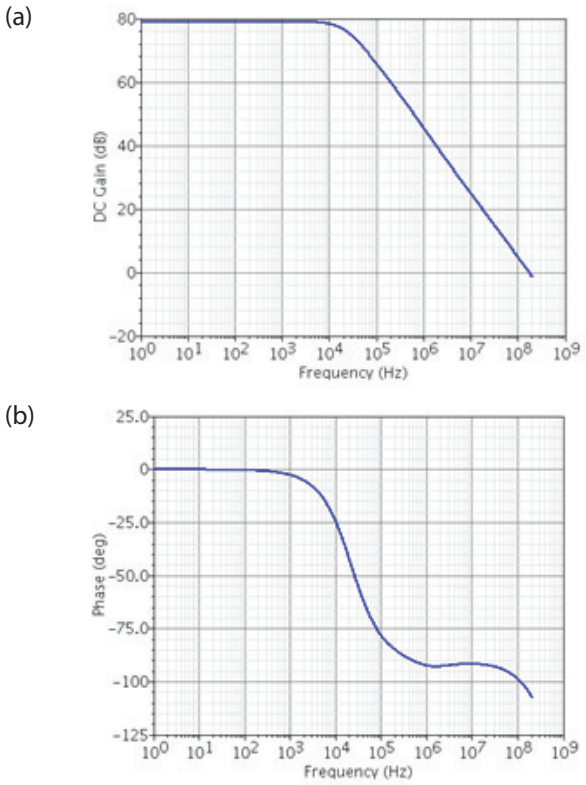


Figure 7: Frequency responses of the proposed OTA: (a) magnitude and (b) phase.

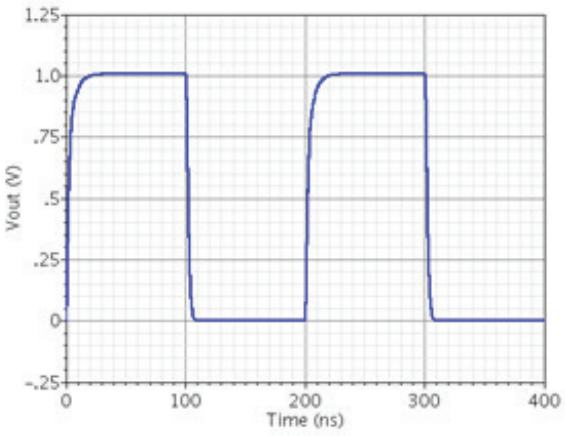


Figure 8: OTA large signal step response.

Table 1: Performance Comparison of the Proposed OTA and the Existing Methods.

Parameter	[28]	[29]	[30]	This work
Bias current	260µA	260µA	260µA	260µA
CL(pF)	7	7	7	7
UGBW(MHZ)	24.6	50	83	160
Gain(dB)	56	65	70	79
Phase margin (deg)	87	80	70	75

SR (V/µs)	12	23	38	47
$FOM_S = \frac{MHz.pF}{mA}$	662	1346	2235	4308
$FOM_L = \frac{V.pF}{ì\ s.mA}$	323	619	1023	1265

Monte Carlo (MC) simulations for the proposed OTA are done by considering both process and mismatch variations. Figure 9 indicates the MC histograms of the proposed OTA using 100-run simulations. From the Figure 9, the mean and standard deviation values for the DC-gain are 76.5 and 4.6, respectively. For the phase margin, the mean and standard deviation values are 75.1 and 1.8, respectively. The layout of the OTA is depicted in Figure 10. The area of the layout is 35µm×86µm.

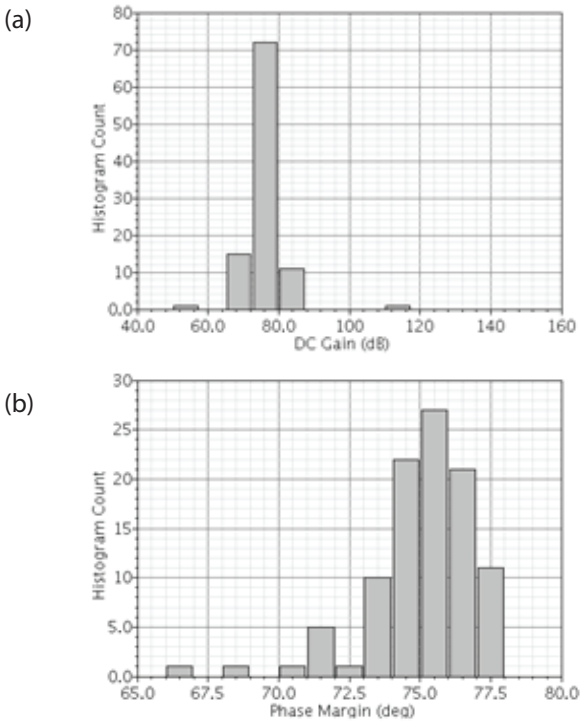


Figure 9: Histogram of MC simulation for the proposed OTA. (a) DC Gain, (b) Phase Margin.

Figure 11 shows the charge and discharge current output versus the output voltage of the second solution for the CP in the process and temperature corners. The current boosting factor of the nonlinear current mirror

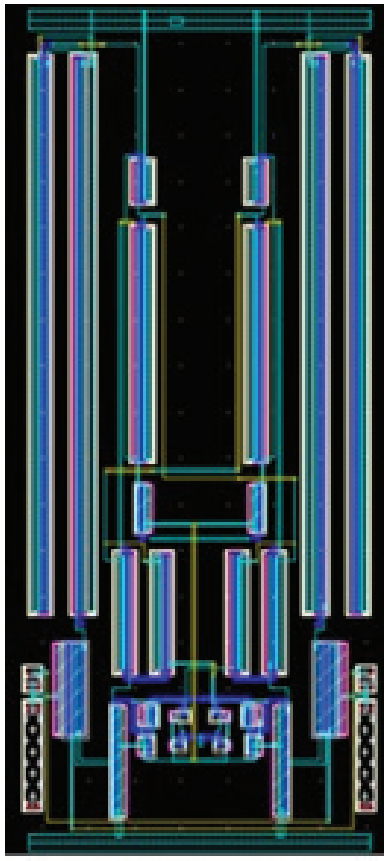


Figure 10: The layout of the OTA.

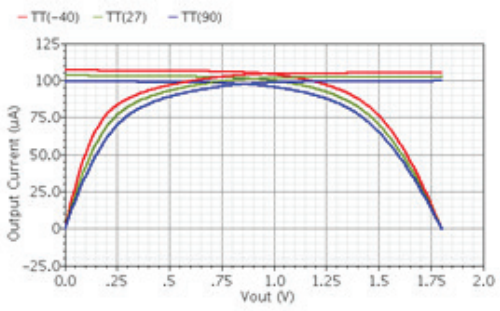
is equal to 1.5. The CP current is about 100 µA, and the mismatch between I_{UP} and I_{DOWN} is less than 0.3% over the output voltage dynamic range from 0.2V to 1.79V, which covers 88% of the 1.8V supply voltage. It has the less current mismatch compared to the first solution.

Table 2 presents the post-layout comparison parameters among the proposed CPs and other existing CP circuits. The second CP has the lowest current mismatch while it has the higher power dissipation due to using the gain-boosting OTA (1.2 mW in the CP2 compared to the 0.6 mW in the CP1). In addition, the CPs have the wide range for the output voltage. In conclusion, the proposed CPs achieve the best trade-off.

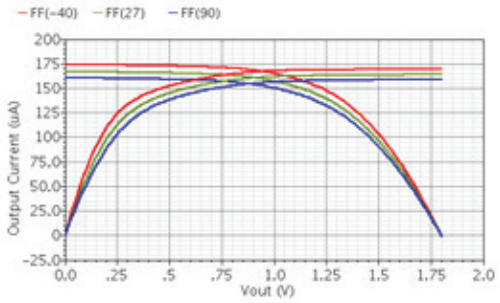
Table 2. Comparison parameters of the proposed CPs and other existing CP circuits.

	CP1	CP2	[6]	[7]	[8]	[9]	[10]
Technology	0.18µm	0.18µm	0.18µm	0.13µm	0.18µm	0.18µm	0.18µm
Supply Voltage (V)	1.8	1.8	1.2	1.2	1.8	1.8	1.8
Current Mismatch	1%	0.3%	0.5%	3.2%	0.5%	1%	0.5%
Output Voltage Range	88%	88%	83%	67%	83%	70%	83%

(a)



(b)



(c)

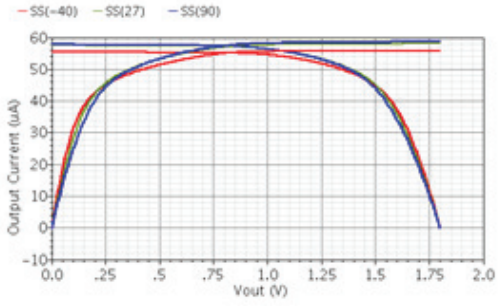


Figure 11. Charge and discharge current output versus the output voltage of the second proposed CP in the process and temperature corners: (a) TT(-40^{0}C), TT(27^{0}C), TT(90^{0}C), (b) FF(-40^{0}C), FF(27^{0}C), FF(90^{0}C), (c) SS(-40^{0}C), SS(27^{0}C), SS(90^{0}C).

4 Conclusions

In this paper, new charge pumps in a 0.18 µm CMOS process with a 1.8 V supply voltage have been presented. The charge pumps were based on the gain-boosting techniques. Common-source amplifier and positive feedback-based OTA were suggested to implement gain-boosting techniques. Nonlinear current mirrors have been employed to generate desired current boosting. The power dissipation of the CP1 and CP2 were 0.6 mW and 1.2 mW, respectively. In order to evaluate the effectiveness of the CPs, several simulation scenarios have been done in the process and temperature corners. The results indicated the superiority of the proposed CPs in terms of current matching characteristics. The mismatch between I_{UP} and I_{DOWN} of the CP1 and CP2 were less than 1% and 0.3%, respectively.

5 Conflicts of Interest

The authors declare no conflict of interest.

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