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A 3.0 – 3.6 GHz LC-VCO with ETSPC Frequency Divider in 0.18-micron CMOS technology

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Abstract: This paper proposes the design, implementation, and measurement of a fully integrated voltage controlled oscillator (VCO) and frequency divider for multi-band transceivers in 0.18-micron IBM 7RF CMOS technology. The VCO is composed of a cross-coupled NMOS transistor-pair and LC tank as a core circuit and 4-bit digitally-switched capacitor block with linearly varying varactors for enhancement of the wide oscillation frequency bandwidth. A design of frequency divider is based on extended true-single-phase-clock (ETSPC) flip-flops with divide values ranging from 2 to 256 for very wide output frequency range. The measured results indicate that the LC-VCO frequency range is from 3.02 GHz to 3.55 GHz, and the phase noise is -108.89 dBc/Hz at 1 MHz offset from 3.55 GHz carrier. The power consumption of the LC-VCO with ETSPC frequency divider including all the buffers and other circuits is about 212 mW for 2.49 dBm of output power. The active area of the test chip occupies only 0.65×0.65 mm^2 and the whole chip size including the ESD protection circuits and pads is 1.5×1.5 mm^2.

Keywords: Frequency divider; integrated circuits (IC); phase noise; transceivers; tuning range; voltage controlled oscillator (VCO).

3.0 – 3.6 GHz LC-VCO z ETSPC frekvenčnim delilnikov v 0.18 mikronski CMOS tehnologiji

Izvleček: Članek obravnava dizajn, implementacijo in meritve polno integriranega napetostno krmiljenega oscilatorja (VCO) in frekvenčnega delilnika za več pasovne sprejemno oddajne enote v 0.18 mikronski IBM 7BF CMOS tehnologiji. VCO je sestavljen iz sklopljenega para NMOS tranzistorjev, vezja LC, 4 bitnega digitalno preklopnega kondenzatorskega bloka z linearno spremenljivo kapacitivnostjo za izboljšanje frekvenčnega območja oscilatorja. Frekvenčni delilnik temelji na razširjenem ETSPC flip flopu v razponu vrednosti od 2 do 256. Merive izkazujejo frekvenčno območje LC-VCO od 3.02 – 3.55 GHz in fazni šum -108.89 dBc/Hz pri 1 MHz odmika od nosilne frekvence 3.55 GHz. Poraba moči LC-VCO skupaj s frekvenčnim delilnikom in ostalim vezjem je 212 mW pri 2.49 dBm izhodne moči. Aktivna površina čipa je 0.65×0.65 mm^2, celotno vezje pa 1.5×1.5 mm^2

Ključne besede: frekvenčni delilnik; integrirana vezja; fazni šum; sprejemno oddajna enota; nastavljivo območje; napetostno krmiljen oscilator

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1 Introduction

With the rapid growth of wireless communication systems, standards, and very wide frequency bands, the demand of fully-integrated, multi-band, multi-standard RF transceivers becomes significant in recent years [1], [2]. Existing multi-band, multi-standard RF transceivers provide a variety of services ranging from basic mobile telephony to ubiquitous broadband internet access. However, most modern multi-band, multi-standard RF transceiver architectures consist of several LNAs, LC-VCOs, PLLs, Mixers, and PAs for each frequency band. For this reason, it leads to large chip area, high cost, and high power consumption. Therefore, IC designers encounter many challenges in developing new architectures of the basic blocks of multi-band, multi-standard RF transceivers.

In a RF transceivers, a voltage-controlled oscillator (VCO) is a crucial building block that is used as local oscillator in high-frequency phase locked loops (PLLs) whose output is used to up- and down-convert signals. In general, high-frequency VCOs can be classified into two main types: the ring-VCO and the LC-VCO. The ring-VCOs occupy a small chip area and offer a wide tuning range. Despite these advantages, LC-VCOs are more common in high performance transceiver chips due to

usually better phase noise performance, lower power consumption and less sensitive to temperature- and supply-variations compared to ring-VCOs. For these reasons, in this paper the LC-VCO is designed.

Another challenge for designers of RF transceivers is high frequency clock division. Common types of clock dividers, such as CML, are becoming inefficient with rapid improvement of CMOS technologies [3], [4]. The true-single-phase-clock (TSPC) and extended TSPC (ETSPC) topologies are becoming more popular because of lower occupied chip area and power consumption [5]. Therefore high-speed ETSPC frequency divider is employed in proposed design.

The goal of this work is the design, implementation and experimental characterization of a 3.0 – 3.6 GHz LC-based VCO and and its output frequency ETSPC divider with divide values ranging from 2 to 256, in a 0.18 µm IBM 7RF CMOS technology. The reconfigurable LC tank can simply adjust oscillation frequency of VCO by the combination of a digitally-switched capacitors for coarse frequency tuning and tuned varactor blocks for fine tuning. This architecture and wide range of divide values make this LC-VCO suitable to multi-band, multi-standard RF transceivers.

This paper is organized as follows: Section 2 describes the analysis of the proposed 3.0 – 3.6 GHz LC-VCO architecture and design of circuits. In Section 3, the design of the divide-by-2…256 frequency ETSPC frequency divider is given. The following Section 4 describes the measurement results, and finally, Section 5 summarizes the most important conclusions of this work.

2 LC-LDO Architecture

Fig. 1 shows the proposed LC-VCO architecture, which consists of the following elements: LC-VCO circuit with digitally-switched capacitor and tuned varactor blocks, DC decoupling stage, differential to single-ended stage, and output buffer. Each of these elements are discussed in more detail below.

LC-VCO core circuit. Fig. 1 also shows a differential-pair negative-impedance LC-VCO circuit, which provides better phase noise characteristics and faster switching of the cross-coupled NMOS differential pair [6]-[8]. The proposed LCVCO consists of the following elements: high-quality inductor (L), digitally-switched capacitors block, varactors block, cross-coupled transistors. The cross-coupled pair consists of NMOS transistors M1 and M2, and generates the negative impedance to cancel the energy loss in the LC tank. The inductor of the LC tank is realized using a two turn spiral differential inductor of 1.97 nH.

Frequency tuning is achieved by two steps: coarse-tuning through a digitally-switched capacitor block and the fine-tuning by the bias of varactors block from the node V_{tune}. In this design, a 4-bit switched capacitor block is used. The block consists of 4 arrays of capacitors connected in parallel, which individually can be turned on or off depending on the required capacity. All switches, that used to turn on or off capacitors, are realized using NMOS transistors. Thus, the sixteen curves of the sub-band cover the wide frequency range.

The fine-tuning is obtained using the varactors block in order to get more precise operation frequency. This block consists of matrix of 12×2 parallel connected multi-finger structure NMOS varactors to enhance the Q-factor and to maximize the tunability of the proposed LC-VCO. The external voltage V_{tune} is used for linear variation of the equivalent capacitance of NMOS varactors.

Similar architectures of the LC-VCO are presented in our previous works and the work of others [9]-[12].

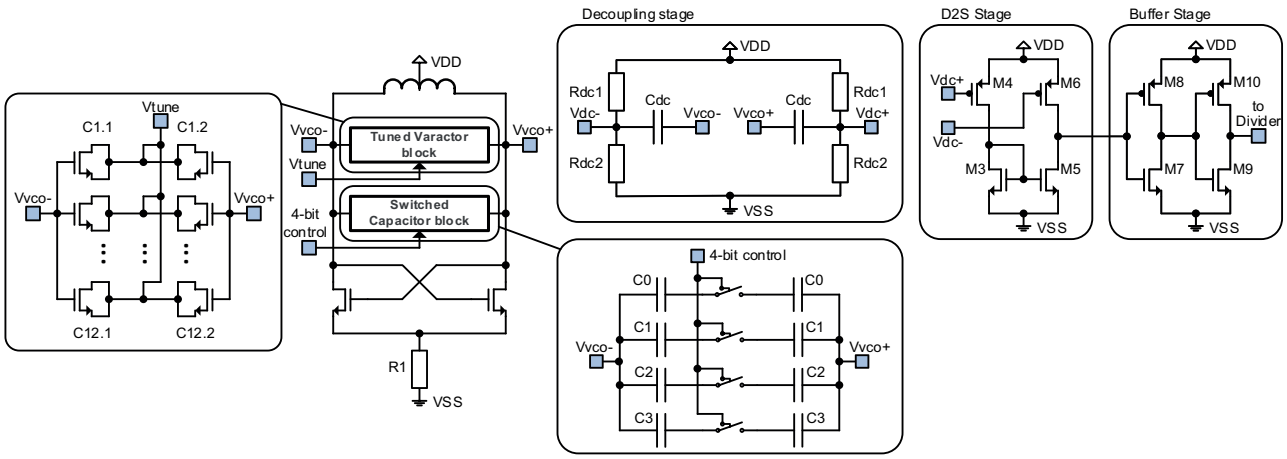


Figure 1: The proposed LC-VCO architecture

DC decoupling stage. The DC output of this proposed LC-VCO topology is biased at V_{DD} through the inductor, so that the output swing of the LC-VCO can reach as high as twice V_{DD}. For this reason, this architecture requires the DC decoupling circuit. The decoupling capacitors C_{dc} removes the DC voltage at the output of the proposed LC-VCO, and the resistances R_{dc} fixes the DC voltage at the input of the differential to single-ended stage circuit.

Differential to single-ended stage. The proposed LC-VCO circuit is implemented with a differential to singleended (D2S) converter. Since input of the frequency divider is single-ended and the LC-VCO output is differential, D2S converter is used as interface between two circuits. This D2S circuit converts the differential signal to single output and produce waveforms that swing rail-to-rail.

Buffer stage. The proposed LC-VCO circuit includes also a buffer stage to drive large capacitive loads with high speed, to increase high input-output isolation and wide output swing range.

3 Frequency Divider

The frequency divider operates at high frequency, equal to the frequency of signal, generated by the LC-VCO. It results in increased chip power consumption. So choosing topology of main block in the divider – flip-flop, is classical engineering task – searching of compromise between operating frequency and power consumption.

There are many suitable topologies of CMOS Flip-flops, which can achieve high operating frequency. Most common are Razavi [3], Wang [4] and CML topologies. Disadvantage of these circuits are high power consumption. In recent years, because of CMOS technology scaling, true-single-phase-clock (TSPC) and extended TSPC (ETSPC) topologies are becoming more popular choice for flip-flops, working at multi-gigahertz frequencies. Advantage of these flip-flops are much simpler schematics and low power dissipation. [13] extensively covers different TSPC and ETSPC structures.

In this paper proposed divide-by-N (where N = 2, 4, 8, 16, 32, 64, 128, 256) frequency divider is based on ETSPC flip-flops. Structure of this divider is shown in Fig. 2. It is made of eight divide-by-2 divider stages, connected in daisy-chain.

Each divide-by-2 divider stage lowers frequency of the signal by half, also relaxing requirements for following divider. So three different divide-by-2 dividers are used: first flip-flop, operating at highest frequency (Fig. 2 [H]), 2nd and 3rd dividers, operating at intermediate frequency (Fig. 2, [I]), and 4th – 8th dividers working at low frequencies (Fig. 2, [L]). Usage of different dividers in daisy-chain allows minimization of power consumption and occupied chip area.

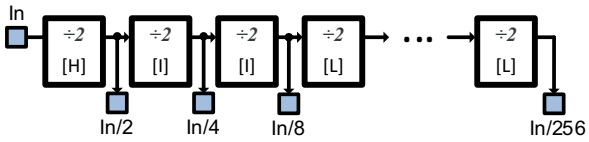


Figure 2: Structure of divide-by-N frequency divider. ÷2 [H]– divideby2 divider working at highest frequency, ÷2 [I]– divideby2 divider working at intermediate frequency, ÷2 [L]– divideby2 divider working at low frequency. In – input signal, In/N– input signal divided by N, where N = 2, 4, 8, 16, 32, 64, 128, 256

Schematics of divide-by-2 dividers are shown in Fig. 3. All divider stages share same structure. Different operating frequency is achieved by different transistor sizing.

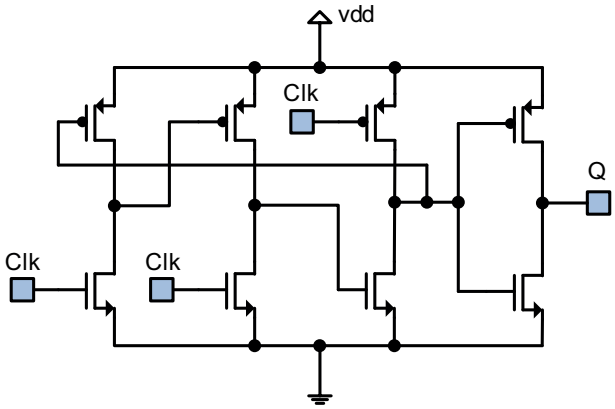


Figure 3: Structure of ETSPC divide-by-2 frequency divider. Clk – input signal. Q – divided by 2 output signal

As we can see from the schematics, ETSPC divider consists of three branches (ETSPC flip-flop), made of two transistors, and output inverter. This inverter is used, because minimal configuration of ETSPC flip-flop has only inversed output. Output inverter also serves as output buffer. Inversed output is connected to the input of the flipflop, hence clock division by 2 is achieved.

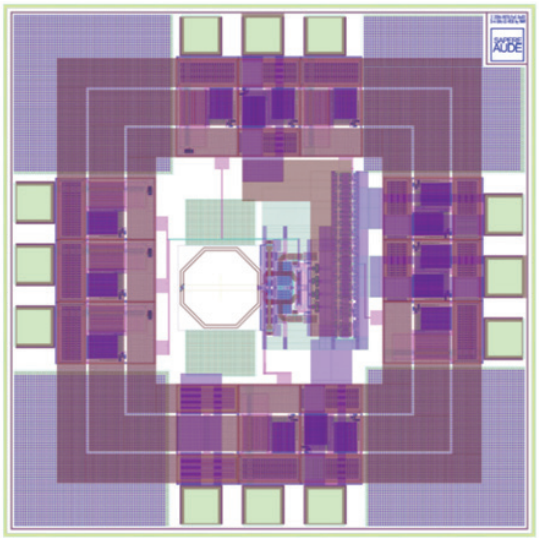
It is also seen from Fig. 3, that there can be situations, when both transistors of branches, consisting clock transistor, are open during half of the clock period. In such situation, output level of the branch is determined by ratio of PMOS and NMOS transistor sizes. This means, that static power dissipation exists in ETSPC flip-flops and it is higher at lower input frequencies.

4 Measurement Results

The proposed LC-VCO with frequency divider chip was designed and fabricated in a 0.18 µm IBM 7RF CMOS technology. The layout and micro-photography of the chip is shown in Fig. 4. The total chip area, including the ESD protection circuits and pads, is 1.5×1.5 mm^2, where the active area occupies only 0.65×0.65 mm^2. The chip was packaged in a 12-pin OCP-QFN package. For testing and measurement purposes, the chip was assembled with standard SMD reflow and chip-on-board technology on Rogers RO4000 high frequency laminate.

It should be noted that all measurement results, which presented in this paper are obtained when division ratio of the ETSPC frequency divider is 8.

a)



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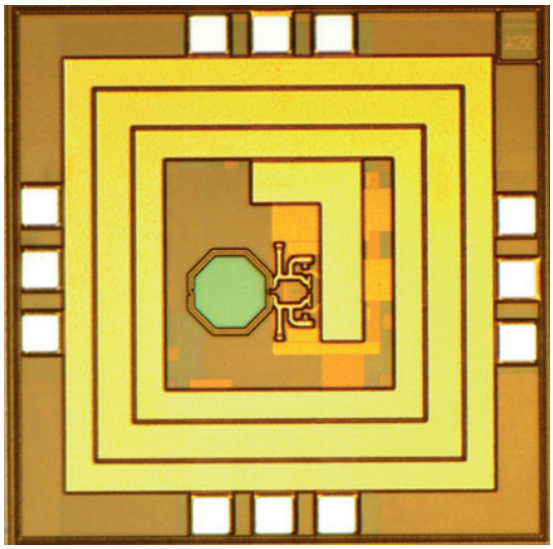

Figure 4: The layout (a) and micro-photograph picture (b) of the proposed LC-VCO with frequency divider

The measured tuning characteristics of the proposed LCVCO with frequency divider, when changing the V_{tune} voltage and the digitally switched capacitor block code, are shown in Fig. 5. These characteristics were obtained by multiplying the measurement results of 8. The tuning range extends from 3.02 GHz up to 3.55 GHz among 16 subbands. With a tuning voltage V_{tune} ranging from 0 V to 2.5 V, the upper sub-band achieves a tuning range from 3.44 GHz to 3.55 GHz and the lower sub-band achieves a tuning range from 3.02 GHz to 3.09 GHz.

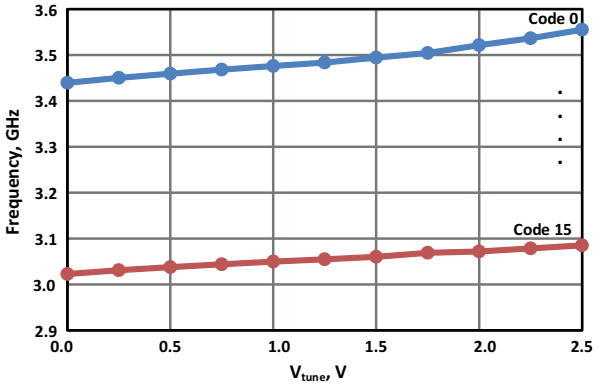

Figure 5: The measured tuning range of the proposed LC-VCO with frequency divider

Fig. 6 shows the measured frequency spectrum of the proposed LC-VCO with frequency divider, when V_{tune} = 2.5 V and the code of digitally-switched capacitor block is set to 0. This combination gives the highest possible frequency of the LC-VCO tuning range. All measurements were performed using a Tektronix RSA5126B real-time spectrum analyzer. The output power spectrum at divide-by-8 output frequency of 444.38 MHz is about 2.49 dBm.

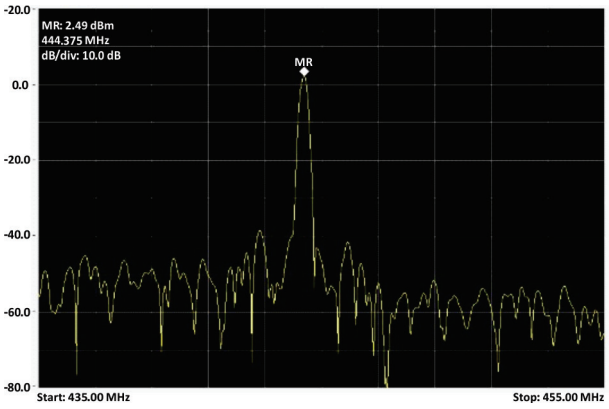

Figure 6: The measured frequency spectrum, when V_{tune} = 2.5 V and the switched capacitor block code = 0

Fig. 7 shows the measured phase noise. The phase noise is about -108.89 dBc/Hz at 1 MHz offset from 3.6 GHz carrier. A summary of the measurement results are shown in Table 1.

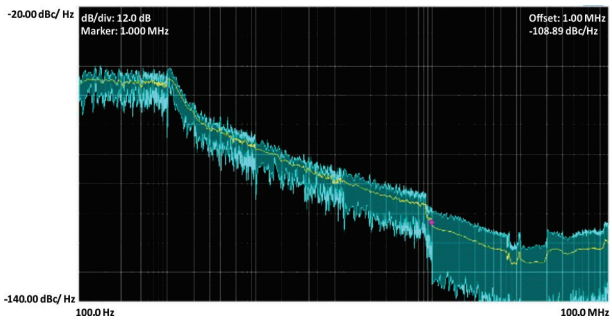

Figure 7: The measured phase noise, when V_{tune} = 2.5 V and the switched capacitor block code = 0

Table 1: Performance summary of the LC-VCO with frequency divider

Characteristics	Value
Technology	0.18 µm RF CMOS
Supply Voltage	2.5 V
Operating Current	85 mA
LC-VCO Tuning Range	3.02 GHz ~ 3.55 GHz
Phase Noise @ 1MHz Offset from 3.6 GHz carrier	-108.89 dBc/Hz
Active area of the test chip	0.65×0.65 mm2

5 Conclusions

A fully integrated 3.0 – 3.6 GHz LC-VCO with an ETSPC frequency *divider* is designed and fabricated in a 0.18 µm IBM 7RF CMOS technology. The total chip area, including the ESD protection circuits and pads, is 1.5×1.5 mm^2. The active part of this fabricated chip occupies *only* 0.65×0.65 mm^2. Using 4-bit switched capacitor block and linearly varying varactors, the LC-VCO achieves a tuning range from 3.02 GHz to 3.55 GHz. The output signal of the LC-VCO is divided down through ETSPC divider, with divide values ranging from 2 to 256. The measurement results of the proposed LC-VCO with frequency divider show a phase noise better than -108.89 dBc/Hz @ 1 MHz offset from 3.6 GHz carrier and a total power consumption of about 212 mW for 2.49 dBm of output power.

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