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Novel Voltage-Mode PID Controller Using a Single CCTA and All Grounded Passive Components

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Abstract: A compact voltage-mode proportional-integral-derivative (PID) controller based on the utilization of a single current conveyor transconductance amplifier (CCTA) is presented in this paper. The presented active PID controller is made up of a single CCTA, and four truly grounded passive components, i.e. two resistors, and two capacitors. The design consideration of the controller parameters has been examined. Besides, the crucial sensitivity performances of the controller parameters for ideal and non-ideal conditions have also been discussed. An application on the closed-loop test system is demonstrated to validate the practicability of the proposed PID controller circuit. To confirm the theoretical behavior, the proposed circuit is simulated with the PSPICE program using TSMC 0.35-μm CMOS process technology. Experimental test results based on commercially available CFOA AD844 and OTA CA3080 integrated circuits are also provided to demonstrate the practicality of the proposed circuit.

Keywords: Current Conveyor Transconductance Amplifier (CCTA); proportional-integral-derivative (PID) controllers; feedback control system; voltage-mode circuit

Nov krmilnik PID v napetostnem načinu z uporabo enega CCTA in ozemljenih pasivnih komponent

Izvleček: V članku je predstavljen kompakten napetostni proporcionalno-integralno-derivativni (PID) krmilnik, ki temelji na uporabi enega samega tokovnega ojačevalnika (CCTA). Predstavljeni aktivni krmilnik PID je sestavljen iz enega CCTA in štirih ozemljenih pasivnih komponent, tj. dveh uporov in dveh kondenzatorjev. Preučena je bila zasnova parametrov krmilnika. Poleg tega so bile obravnavane tudi ključne občutljivosti parametrov regulatorja za idealne in neidealne pogoje. Za potrditev uporabnosti predlaganega vezja PID regulatorja je prikazana uporaba na zaprtem preskusnem sistemu. Za potrditev teoretičnega obnašanja je predlagano vezje simulirano s programom PSPICE z uporabo 0,35-m CMOS procesne tehnologije TSMC. Za dokazovanje praktičnosti predlaganega vezja so na voljo tudi rezultati eksperimentalnih preskusov, ki temeljijo na komercialno dostopnih integriranih vezjih CFOA AD844 in OTA CA3080.

Ključne besede: tokovni transkonduktančni ojačevalnik (CCTA); proporcionalno-integralno-derivativni krmilniki (PID); povratni krmilni sistem; napetostno vezje

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1 Introduction

Proportional-Integral-Derivative (PID) controllers are the most commonly employed control actions in feedback control systems, and process industries [1]. They have been extensively utilized for several decades since they feature a variety of desired properties, including design simplicity, low cost, robustness, and broad application, as well as easy parameter tuning [2]. Their wide range of applications have stimulated and sustained the design and invention of various PID controller circuits and sophisticated hardware modules. Over the last two decades, the enormous literature on PID process controllers has featured a wide range of design techniques based on numerous active compo-

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nents, such as operational transconductance amplifiers (OTAs) [3], second generation current conveyors (CCIIs) [4]-[5], current feedback operational amplifiers (CFOAs) [6]-[9], current differencing buffered amplifiers (CDBAs) [10], differential voltage current conveyor transconductance amplifiers (DVCCTAs) [11], current follower transconductance amplifiers (CFTAs) [12]-13], voltage differencing transconductance amplifiers (VDTAs) [14], voltage differencing current conveyors (VDCCs) [15], and second generation voltage conveyors (VCIIs) [16]. In [3]-[4], [6], [9]-[10], the PID controllers designed with the signal-flow graph approach have been proposed. However, for the realizations in [3]-[4], [9]-[10], [16], at least four active components were required. Furthermore, PID controller realizations of [4]-[6], [9]-[11], [13]-[15] include a number of passive components, i.e., at least five passive components, some of which are also floating. Floating passive components were used to design single active element-based PID controller circuits in [7]-[8], [12]-[13], [15]-[16]. Active circuit structures with all grounded passive elements are well recognized to be useful for fully integrated circuit (IC) design as well as IC hybrid fabrication processes. This is due to the fact that the usage of grounded passive elements is helpful for the electronic adjustability and permits the elimination/accommodation of various parasitic effects for IC implementation. Another point to note is that the performance and application of the previously discussed controllers [3]-[7], [10]-[15] were evaluated solely through computer simulations. For acceptability purposes, experimental measurements are the important method to evaluate the practicability of the circuit.

The current conveyor transconductance amplifier (CCTA) is a contemporary versatile active circuit block that is a cascade of a CCII and an OTA [17]. The CCTA has been extensively used in the design of analog signal processing circuits and solutions like as analog filters [18]-[20], sinusoidal oscillators [21]-[22], resistor-less inductance simulator [23], and high-frequency active meminductor emulator [24].

Therefore, this work aims at proposing a CCTA-based voltage-mode PID controller with a canonic and low-component count. It is made up of only one CCTA as an active component and all grounded passive components, such as two resistors and two capacitors. There is no element-equality criteria required for the controller realization. Non-ideal gain effects on the controller performance and sensitivity analysis are also investigated. The functionality of the proposed PID controller is evaluated in a closed-loop system. As an example plant circuit, a second-order lowpass filter was built to design the closed-loop system. To test the behavior of the proposed PID controller circuit, some computer simulations using the PSPICE software and experimental measurement data using off-the-shelf integrated circuits AD844 and CA3080 are presented.

Table 1 illustrates the comparative analysis of all previously mentioned PID controllers as having the following desirable properties to substantiate the proposition of the proposed controller: (i) the number of active elements, (ii) the number of passive elements, (iii) the use of all grounded passive elements, (iv) electronic tunability, (v) simulation technology, (vi) simulation supply voltages, (vii) simulated total power consumption, (viii) experimental technology, and (ix) experimental supply voltages.

2 Circuit description

2.1 CCTA properties

Basically, the CCTA is a versatile active building block designed by the cascade connection of CCII followed by an OTA [17]. The schematic symbol of the CCTA is depicted in Fig.1. The voltage drop at terminal x follows the applied voltage at terminal y in magnitude. The output currents at terminals z and zc follow the current through terminal x in magnitude. The voltage drop at terminal z is converted to an output current at terminal o with the transconductance gain (g_m). The terminal relationship of the ideal CCTA can be described by the following set of equations:

$$\begin{bmatrix} i_y \\ v_x \\ i_z \\ i_{zc} \\ i_o \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 1 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 \\ 0 & 0 & g_m & 0 \end{bmatrix} \begin{bmatrix} i_x \\ v_y \\ v_z \\ v_o \end{bmatrix} \quad (1)$$

In general, the transconductance g_m can be modified electronically by adjusting the externally provided current I_B.

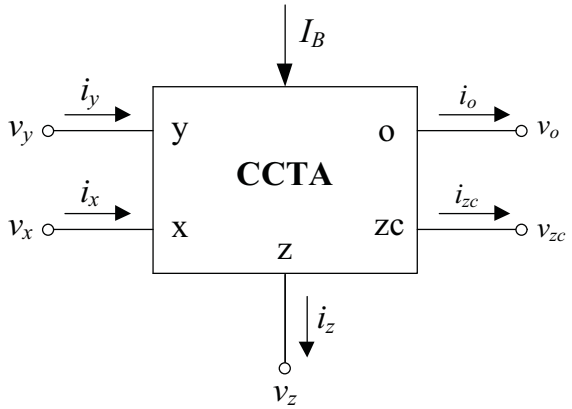


Figure 1: Schematic symbol for the CCTA

2.2 Proposed single CCTA-based PID controller circuit

In a general PID controller, three modes of controller with proportional, integral, and derivative actions must be incorporated. As a consequence, the transfer function of a standard voltage-mode PID controller is generally defined as follows: [25]

$$T(s)=\frac{V_{out}(s)}{V_{in}(s)}=K_P+\frac{K_I}{s}+sK_D \quad (2)$$

where $V_{in}(s)$ is the input voltage, $V_{out}(s)$ is the output voltage, K_P is the proportional coefficient, K_I is the integral coefficient, and K_D is the derivative coefficient.

Fig.2 shows the proposed voltage-mode PID controller based on CCTA as an active component. The controller comprises only a single CCTA, and all grounded passive components, i.e. two resistors and two capacitors.

From the aspect of an integrated circuit, it is critical to employ all grounded passive components. The circuit analysis of the proposed PID controller in Fig.2 gives the following voltage transfer function.

$$G_c(s)=\frac{V_{oc}(s)}{V_{ic}(s)}=\frac{R_2}{R_1}\left(1+\frac{g_mR_1C_1}{C_2}\right)+\frac{g_mR_2}{sR_1C_2}+sR_2C_1 \quad (3)$$

By comparing the above obtained function with the general equation of the PID controller given in equation (2), the various coefficients of the proposed controller are determined to be as follows:

$$K_P=\frac{R_2}{R_1}\left(1+\frac{g_mR_1C_1}{C_2}\right) \quad (4)$$

Table 1: Comparative features of the proposed circuit with previously reported PID controllers

Circuit	(i)	(ii)	(iii)	(iv)	Simulation results			Experimental results	
					(v)	(vi)	(vii)	(viii)	(ix)
Ref. [3] in 2001	OTA = 8	C = 2	yes	yes	0.8-µm AMS	±5V	N/A	--	--
Ref. [4] in 2001	VB = 4, CCII+ = 4	R = 8, C = 2	no	no	AD844	±12V	N/A	--	--
Ref. [5] in 2006	CCII+ = 1, DO-CCII+ = 1	R = 3, C = 2	yes	no	0.35-µm TSMC	±1.5V, +0.5V	N/A	--	--
Ref. [6] in 2001	CFOA = 6	R = 12, C = 2	no	no	--	--	--	--	--
Ref. [7] in 2013	CFOA = 1	R = 2, C = 2	no	no	AD844	±12 V	N/A	--	--
Ref. [8] in 2018	CFOA = 1	R = 2, C = 2	no	no	0.18-µm TSMC	±2 V	N/A	AD844	±12 V
Ref. [9] in 2021	CFOA = 2	R = 3, C = 2	no	no	AD844	N/A	N/A	AD844	±12 V
Ref. [10] in 2006	CDBA = 4	R = 8, C = 2	no	no	0.8-µm AMS	±2.5V, ±1V	N/A	--	--
Ref. [11] in 2019	DVCCTA=1	R = 3, C = 2	no	yes	0.25-µm TSMC	±1.5 V, -1 V	N/A	--	--
Ref. [12] in 2015	ZC-CFTA = 1	R = 2, C = 2	no	yes	0.35-µm BiCMOS	±1 V	23.7 mW	--	--
Ref. [13] in 2021	CFTA = 2	R = 4, C = 2	no	yes	0.18-µm TSMC	±0.6 V	1.12 mW	--	--
Ref. [14] in 2016	VDTA = 2	R = 3, C = 2	no	yes	0.18-µm MOSIS	±0.9 V	N/A	--	--
Ref. [15] in 2021	VDCC = 1	R = 4, C = 2	no	yes	0.18-µm TSMC	±0.9 V	N/A	--	--
Ref. [16] in 2022	VCII = 1	R = 2, C = 2	no	no	0.18-µm TSMC	±0.9 V	N/A	AD844	±15 V
Proposed circuit	CCTA = 1	R = 2, C = 2	yes	yes	0.35-µm TSMC	±1.5 V	35.8 mW	AD844, CA3080	±5 V

N/A = not available, " -- " = not provided
VB = voltage buffer, CCII+ = plus-type CCII, DO-CCII+ = dual-output plus-type CCII, ZC-CFTA = z-copy CFTA,

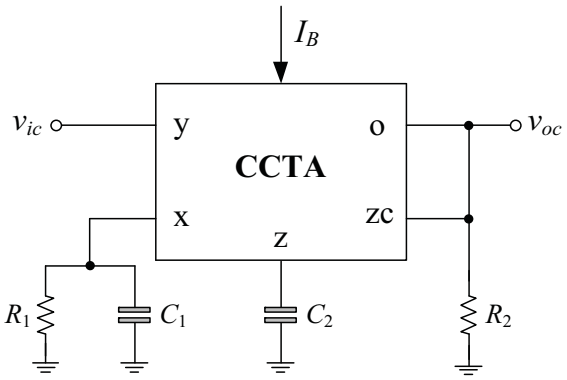


Figure 2: Proposed single CCTA-based PID controller using all grounded passive elements.

$$K_I = \frac{g_m R_2}{R_1 C_2} \tag{5}$$

and

$$K_D = R_2 C_1 \tag{6}$$

As seen from the above expressions, the various gain coefficients of the PID controller can be controlled electronically. The expressions also show that the three coefficients can be determined by appropriately setting the values of g_m, R_1, R_2, C_1 and C_2. The design considerations will be outlined in the following section. Because the primary contribution of this work is the design of a compact analog PID controller with a minimal number of active and passive components, independent tuning of the gain coefficients K_P, K_I and K_D is not expected. Due to the low component count, the circuit requires a small chip area. As a result, the production cost is lowered.

2.3 Practical design considerations

In order to realize the desired gain parameters of the proposed PID controller indicated in equations (4)-(6), the design procedure for setting the circuit components is described as follows.

From equations (5) and (6), the values of capacitors C_1 and C_2 so obtained are expressed as

$$C_1 = \frac{K_D}{R_2} \tag{7}$$

and

$$C_2 = \frac{g_m R_2}{R_1 K_I} \tag{8}$$

Therefore, substituting these relations into equation (4), we then obtain

$$K_P = \frac{R_2}{R_1} + \frac{g_m K_I K_D}{R_2} \tag{9}$$

According to the PID design criteria, the coefficients K_I and K_D are supposed to be arbitrarily determined parameters. By taking

$$R_2 = xR_1 \tag{10}$$

the gain K_P modifies to

$$K_P = x + \frac{g_m K_I K_D}{xR_1} \tag{11}$$

The minimum value of K_P derived from equation (11) is obtained at

$$x = \sqrt{\frac{g_m K_I K_D}{R_1}} \tag{12}$$

and its minimum value can be given below:

$$K_{P(\min)} = 2\sqrt{\frac{g_m K_I K_D}{R_1}} \tag{13}$$

It can be realized from equation (13) that the value of $K_{P(\min)}$ is determined by the given values of K_I and K_D. As a result, the useful value for the gain K_P should satisfy the following relationship:

$$K_P \geq 2\sqrt{\frac{g_m K_I K_D}{R_1}} \tag{14}$$

Rearranging equation (11), we found that

$$.x^2 + xK_P + \frac{g_m K_I K_D}{R_1} = 0 \tag{15}$$

Based on the condition of the K_P value specified in equation (14), equation (15) has two real roots, as illustrated below.

$$x_{1,2} = \frac{K_P}{2} \pm \sqrt{\frac{K_P^2}{4} - \frac{g_m K_I K_D}{R_1}} \tag{16}$$

Therefore, the basic steps in the sequel are followed to determine the required controller parameters, and satisfy the K_P value given in equation (14).
Step (1): Choose g_m and R_1 arbitrarily.
Step (2): Determine x from equation (16).
Step (3): Determine R_2 from equation (10).
Step (4): Determine C_1 from equation (7).
Step (5): Determine C_2 from equation (8).

2.4 Non-ideal effects

The non-ideal condition of the real CCTA is investigated in this section. The port relationship of the non-ideal

CCTA, including tracking errors, can be modeled by the following matrix equation:

$$\begin{bmatrix} i_y \\ v_x \\ i_z \\ i_{zc} \\ i_o \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & \beta & 0 & 0 \\ \alpha & 0 & 0 & 0 \\ \alpha & 0 & 0 & 0 \\ 0 & 0 & \delta g_m & 0 \end{bmatrix} \begin{bmatrix} i_x \\ v_y \\ v_z \\ v_o \end{bmatrix} \quad (17)$$

where $\beta = 1 - \varepsilon_v$ and $\alpha = 1 - \varepsilon_i$ are the non-ideal gains. The parameters ε_v ($|\varepsilon_v| << 1$) and ε_i ($|\varepsilon_i| << 1$) represent the voltage and current tracking errors from the y to the x terminals and from the x to the z and zc terminals, respectively. The non-ideal gain $\delta = 1 - \varepsilon_{gm}$, where ε_{gm} ($|\varepsilon_{gm}| << 1$) is the transconductance tracking error between the z and o terminals.

By taking the non-ideal CCTA into effect, the voltage transfer function of the proposed PID controller in Fig.2 can be derived as:

$$G_c(s) = \frac{\alpha\beta R_2}{R_1}\left(1 + \frac{\delta g_m R_1 C_1}{C_2}\right) + \frac{\alpha\beta\delta g_m R_2}{sR_1 C_2} + s\alpha\beta R_2 C_1 \quad (18)$$

In this case, the non-ideal gain parameters of the PID controller can then be obtained as:

$$K_P = \frac{\alpha\beta R_2}{R_1}\left(1 + \frac{\delta g_m R_1 C_1}{C_2}\right) \quad (19)$$

$$K_I = \frac{\alpha\beta\delta g_m R_2}{R_1 C_2} \quad (20)$$

and

$$K_D = \alpha\beta R_2 C_1 \quad (21)$$

The above expressions clearly show that the non-ideal gains β, α and δ of the CCTA have a direct effect on the PID gain parameters K_P, K_I and K_D. The absolute coefficients of the active and passive sensitivity versus PID gain parameters are found to be less than or equal to unity, as shown by the following equations:

$$S_{g_m}^{K_P} = S_{\delta}^{K_P} = \frac{1}{\left(1 + \frac{C_2}{\delta g_m R_1 C_1}\right)} < 1 \quad (22)$$

$$S_{\alpha}^{K_P} = S_{\beta}^{K_P} = 1 \quad (23)$$

$$S_{R_1}^{K_P} = -\frac{1}{\left(1 + \frac{\delta g_m R_1 C_1}{C_2}\right)} < -1 \quad (24)$$

$$S_{R_2}^{K_P} = 1 \quad (25)$$

$$S_{C_1}^{K_P} = \frac{1}{\left(1 + \frac{C_2}{\delta g_m R_1 C_1}\right)} < 1 \quad (26)$$

$$S_{C_2}^{K_P} = -\frac{1}{\left(\frac{1}{\delta} + \frac{C_2}{\delta g_m R_1 C_1}\right)} < -1 \quad (27)$$

$$S_{g_m}^{K_I} = S_{\alpha}^{K_I} = S_{\beta}^{K_I} = S_{\delta}^{K_I} = 1 \quad (28)$$

$$S_{R_1}^{K_I} = -S_{R_2}^{K_I} = S_{C_2}^{K_I} = -1 \quad (29)$$

$$S_{\alpha}^{K_D} = S_{\beta}^{K_D} = 1 \quad (30)$$

and

$$S_{R_2}^{K_D} = S_{C_1}^{K_D} = 1 \quad (31)$$

3 Simulation results

The theoretical assumptions are validated through PSPICE simulation utilizing 0.35-µm CMOS process parameters provided by TSMC. For simulation, the CMOS implementation of the CCTA shown in Fig.3 was used with symmetrical supply voltages of ±1.5 V. Transistor aspect ratios are provided in Table 2. The transconductance of the CCTA is found as:

$$g_m = \sqrt{KI_B} \quad (32)$$

where $K = \mu C_{ox}(W/L)$. Here, the parameters µ, C_{ox}, W, and L denote electron mobility, oxide capacitance per unit gate area, effective channel width, and effective channel length, respectively. The transconductance g_m is dependent on the process parameter K, and the external bias current I_B, according to equation (32). The plot in Fig.4 also illustrates the variations in g_m for the CMOS CCTA in Fig.3, which are relatively dependent on variations in I_B. It has been analyzed that, when I_B is varied from 40 µA to 230 µA, the percentage inaccuracy in g_m is less than 9% compared to the theoretical g_m value.

Table 2: Aspect ratios of the transistors of CMOS CCTA in Fig.3

Transistor	W/L (µm/µm)
M_1-M_2, M_{12}-M_{13}	16/0.7
M_3-M_6, M_{16}	7/0.7
M_7-M_{11}, M_{19}-M_{20}	21/0.7
M_{14}-M_{15}	28/0.7
M_{17}-M_{18}	8.5/0.7

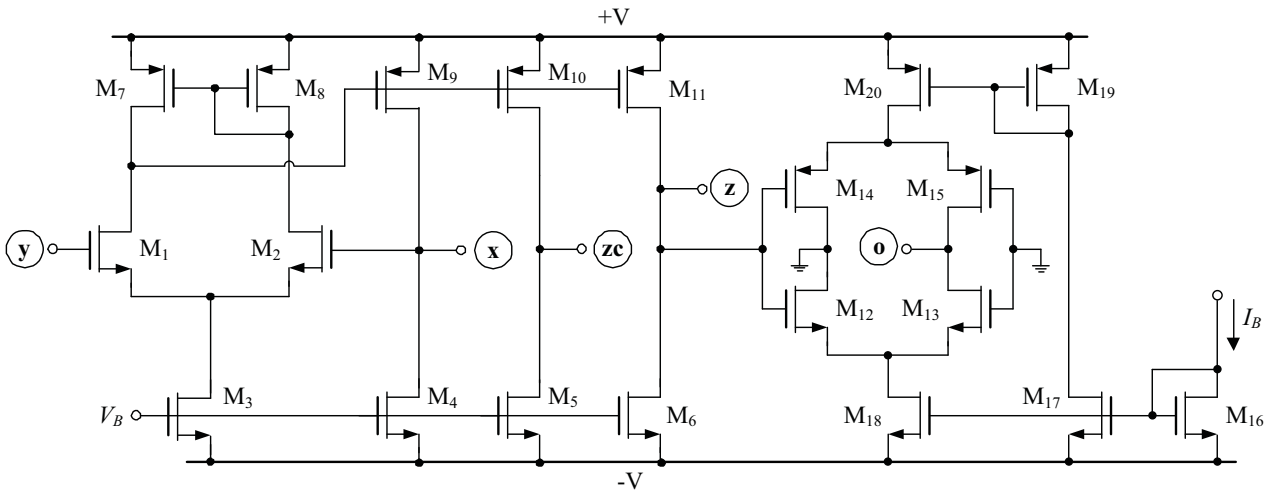


Figure 3: Possible CMOS realization of the CCTA used in simulations

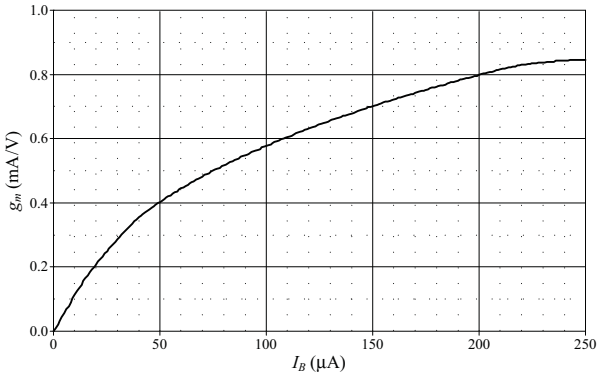


Figure 4: g_m plot for variations in I_B for the CMOS CCTA in Fig.3

Firstly, the proposed PID controller circuit in Fig.2 was designed with the following components: g_m = 0.61 mA/V (I_B = 100 μA), R_1 = 1 kΩ, R_2 = 5 kΩ, and $C_1 = C_2$ = 1 nF. The corresponding controller gains are obtained as: K_P = 8, K_I = 3 Ms, and K_D = 5 μs. The ideal and simulated transient responses of the proposed controller, for a 100-mV triangular input voltage with a frequency of 500 kHz, are shown in Fig.5. For frequency-domain performance analysis, the ideal and simulated responses with identical component values are shown in Fig.6. The total power consumption of the proposed PID controller is found as 35.8 mW.

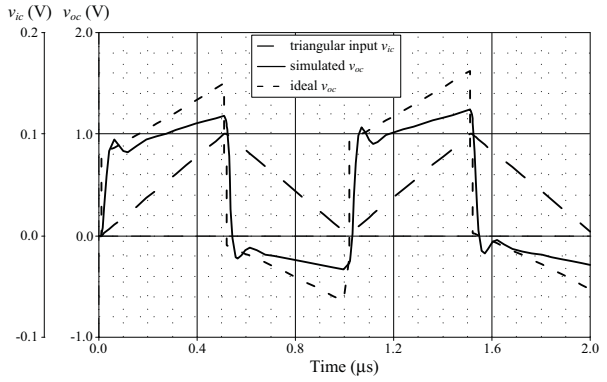


Figure 5: Time-domain responses of the proposed PID controller

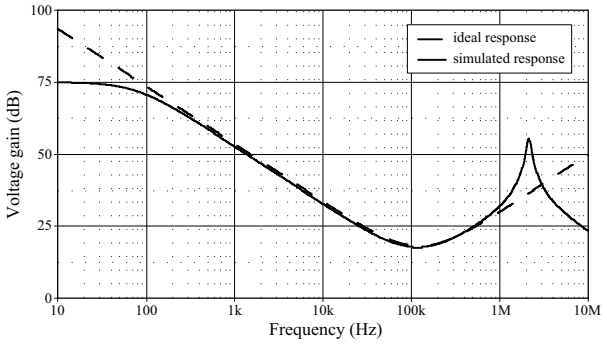


Figure 6: Frequency-domain responses of the proposed PID controller

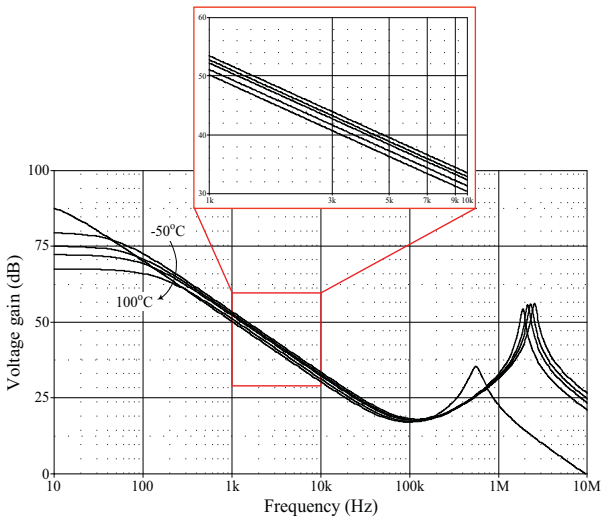


Figure 7: Frequency-domain responses of the proposed PID controller at temperature ranges -50°C, 0°C, 27°C, 50°C, and 100°C.

Additionally, the temperature-dependent variation of the frequency-domain responses of the proposed PID controller analysis was performed at industrial ranges T = -50°C, 0°C, 27°C, 50°C, and 100°C. The simulation results of the industrial temperature analysis are given in Fig.7, where it can be observed that the gain characteristic of the controller diminishes with increasing temperature.

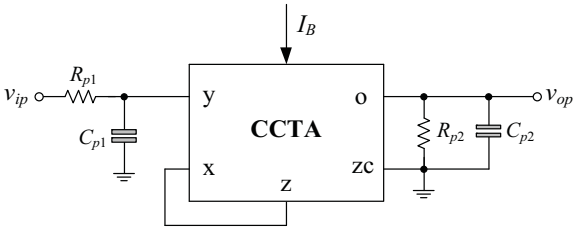


Figure 8: Single CCTA-based lowpass filter using only grounded capacitors

For the performance evaluation of the proposed PID controller circuit in Fig.2, a voltage-mode lowpass filter using a single CCTA and four passive elements is realized as shown in Fig. 8. The voltage transfer function of the filter with $R_{p2} = 1/g_m$ is given by

$$G_p(s) = \frac{V_{op}(s)}{V_{ip}(s)} = \frac{\left(\frac{g_m}{R_{p1}C_{p1}C_{p2}}\right)}{s^2 + s\left[\frac{g_m(R_{p1}C_{p1}+C_{p2})}{R_{p1}C_{p1}C_{p2}}\right] + \left(\frac{g_m}{R_{p1}C_{p1}C_{p2}}\right)} \quad (33)$$

where the pole frequency (ω_p) and the quality factor (Q) are derived as:

$$f_p = \frac{\omega_p}{2\pi} = \frac{1}{2\pi}\sqrt{\frac{g_m}{R_{p1}C_{p1}C_{p2}}} \quad (34)$$

and

$$Q = \left(\frac{1}{R_{p1}C_{p1}+C_{p2}}\right)\sqrt{\frac{R_{p1}C_{p1}C_{p2}}{g_m}} \quad (35)$$

The negative feedback system has been given to evaluate the practical ability of the proposed PID controller circuit. The block diagram of the closed-loop system is represented in Fig.9. In the study that follows, the step response of the system is analyzed to observe the effect of the proposed controller on this system. For the lowpass filter in Fig. 8, the component values were set as follows: g_m = 0.61 mA/V, R_{p1} = 1 kΩ, R_{p2} = 1.5 kΩ, and $C_{p1} = C_{p2}$ = 1 nF, giving f_p = 124.3 kHz and Q = 1.28. Fig.10 shows the ideal and simulated transient responses of $e(t)$ and $u(t)$ for the closed-loop system in Fig.9 with the ramp input voltage $v_{in}(t)$ rising time of 3 µs/100 mV. The overall power consumption of the closed-loop system in Fig.9 is estimated to be 108 mW predicated on simulations.

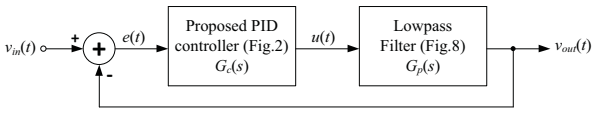


Figure 9: Feedback control system to evaluate the performance of the proposed PID controller.

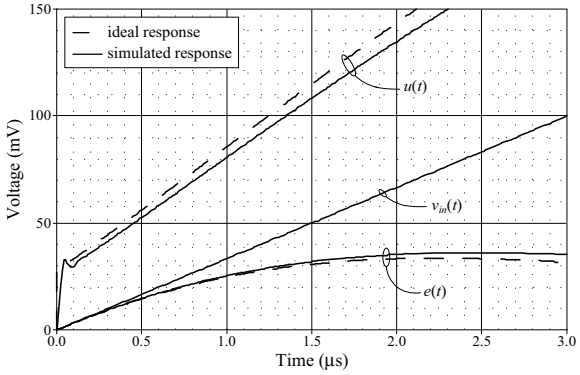


Figure 10: Ramp-input responses of $e(t)$ and $u(t)$ for the closed-loop system in Fig.9.

In addition to observing the step response of the system, a step input with amplitude of 100 mV was applied, and the obtained results are displayed in Fig.11. These results are provided to demonstrate the transient response characteristics of the system for four different values of the tuning controller gain parameters. The first set of gain parameters in Fig.11(a) for case 1 were K_P = 1.9, K_I = 0.86 Ms, and K_D = 1 µs with g_m = 0.86 mA/V, $R_1 = R_2$ = 5 kΩ, and $C_1 = C_2$ = 1 nF. The second parameters in Fig.11(b) were modified to K_P = 6.9, K_I = 1.9 Ms, and K_D = 5 µs by selecting g_m = 0.38 mA/V, R_1 = 1 kΩ, R_2 = 5 kΩ, and $C_1 = C_2$ = 1 nF for case 2. The gain parameters in case 3 of Fig.11(c) were K_P = 8, K_I = 3 Ms, and K_D = 5 µs with g_m = 0.61 mA/V, R_1 = 1 kΩ, R_2 = 5 kΩ, and $C_1 = C_2$ = 1 nF. For case 4, the gains in Fig.11(d) were K_P = 13.6, K_I = 8.6 Ms, and K_D = 5 µs by setting g_m = 0.86 mA/V, R_1 = 1 kΩ, R_2 = 5 kΩ, C_1 = 1 nF, and C_2 = 0.5 nF.

4 Experimental results

In experimental measurements, the CCTA has been practically constructed with commercially available ICs such as AD844s [26] and CA3080 [27], as depicted in Fig.12. In this case, the CCTA's transconductance gain (g_m) is proportional to the external bias current (I_B) and has the following relationship: $g_m = 20I_B$ [27]. The symmetrical bias voltages of the AD844s and CA3080 were set at ±5V. Also, for the laboratory testing circuit, the active and passive elements were chosen as g_m = 0.86 mA/V (I_B = 43 µA), $R_1 = R_2$ = 5 kΩ, and $C_1 = C_2$ = 1 nF,

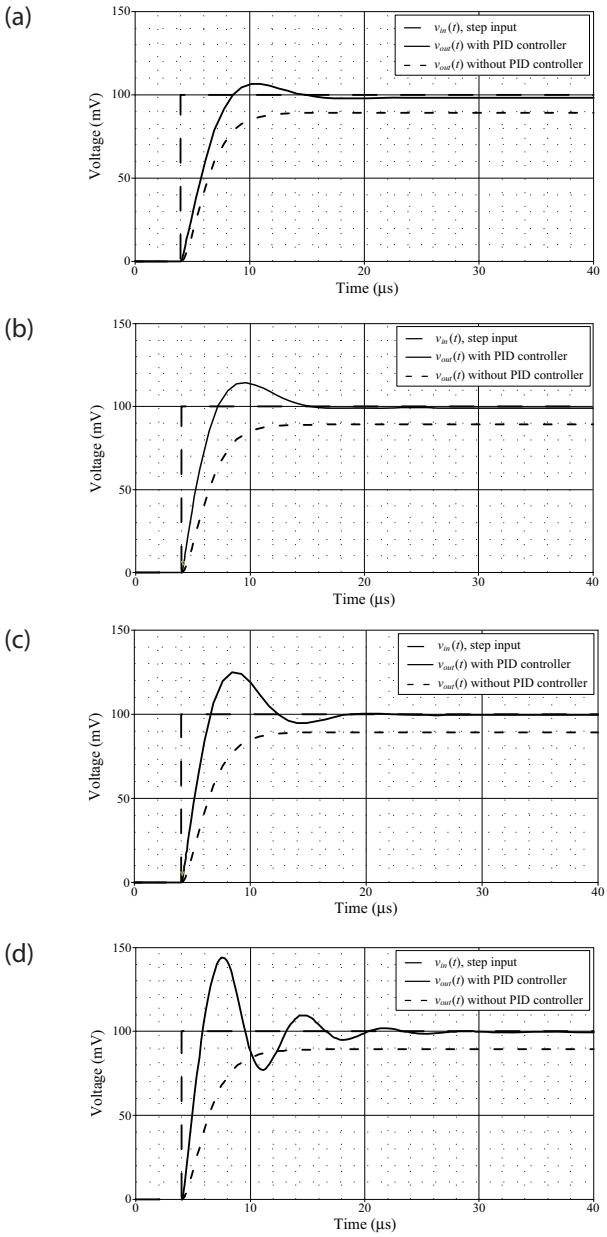


Figure 11: Simulated step-input response characteristics of the closed-loop system in Fig.9. (a) Case 1; (b) Case 2; (c) Case 3; (d) Case 4

which leads to K_P = 1.9, K_I = 0.86 Ms, and K_D = 1 μs as in case 1. A step input voltage with amplitude of 100 mV was applied to the input of the experimental test circuit. Fig.13 shows the measured input voltage and associated output waveforms for the uncontrolled filter $v_{op}(t)$ and the controlled filter $v_{out}(t)$.

To evaluate the impact of the proposed PID controller on the step response of the closed-loop system in Fig.9, the measured transient responses for three different controller gains are given in Fig.14. The experimental test results were obtained using the same component settings as in simulation verification, namely

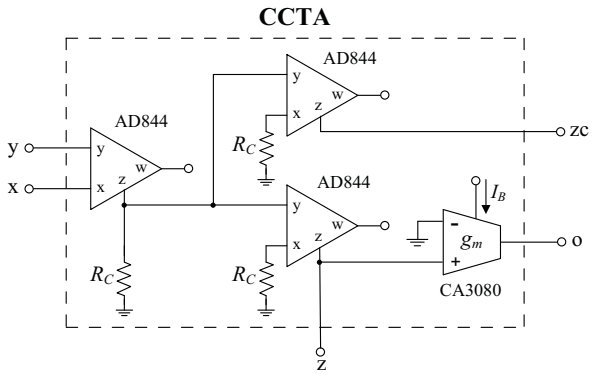


Figure 12: Practical CCTA implementation using readily available ICs AD844s and CA3080.

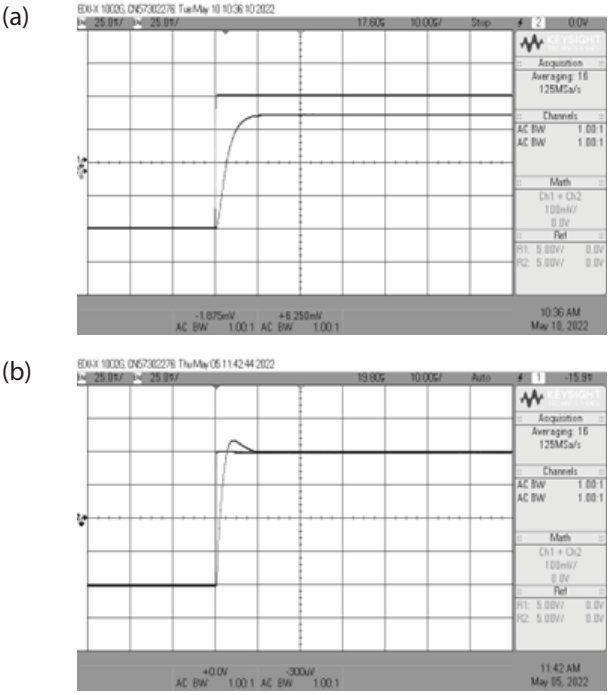
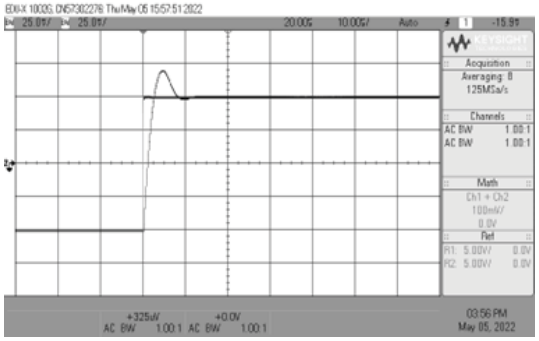


Figure 13: Measured step responses of the closed-loop system in Fig.9 for case 1. (a) without PID controller; (b) with PID controller

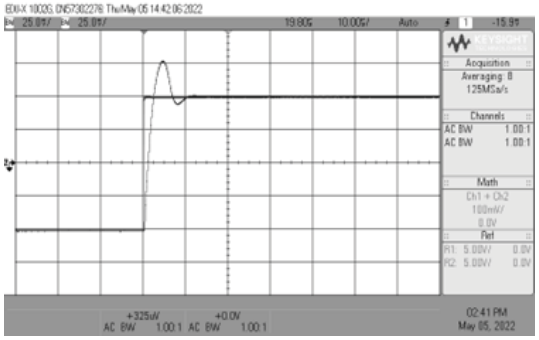
case 2, case 3, and case 4. From Figs.13 and 14, the performance comparison in terms of delay time (t_d), rise time (t_r), peak time (t_p), peak output (p_o), maximum overshoot (M_p), and settling time (t_s) are also measured and summarized in Table 3. As observed in Table 3, the use of the proposed PID controller clearly improves the system's performance in the desired manner.

On the other hand, the ideal, simulated and measured frequency-domain responses of the closed-loop system in Fig.9 for the four mentioned cases of the controller gain values are given in Fig.15. The experimental results validate the ideal responses within the working range of the proposed PID controller. Nevertheless, the slight deviation in these responses is mostly due

(a)



(b)



(c)

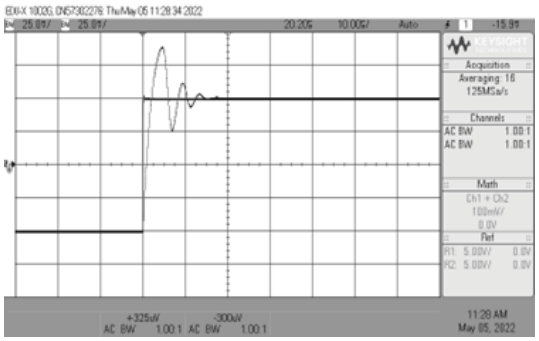


Figure 14: Measured step responses of the closed-loop system in Fig.9 with variable controller gains. (a) Case 2; (b) Case 3; (c) Case 4

to the non-ideal characteristics of AD844s and CA3080 in Fig.12, such as non-ideal transfer gains and parasitic impedances. Some techniques [28]-[29] that reduce non-ideal transfer gains and parasitic elements can be used to minimize the difference between ideal and measured responses.

5 Conclusions

This paper suggests a novel voltage-mode PID controller based on CCTA. A single CCTA, two resistors, and two capacitors are used in the suggested circuit. Because all of the passive components in this realization are grounded, it is ready for further integration. The implementation does not need element-matching requirements and can be simply accomplished using commercially available integrated circuits. The controller gain parameters K_P, K_I, and K_D are all adjustable. An application example of the proposed PID controller as the closed-loop system is included. The analysis of the theoretically proposed circuit has been validated through simulation findings and experimental test results.

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7 Conflict of Interest

The authors confirm that this article content has no conflict of interest.

Table 3: Comparison of the performance of the uncontrolled filter and the controlled filter

Parameter	Uncontrolled filter	Controlled filter with proposed PID controller			
		Case 1: $K_P = 1.9$, $K_I = 0.86$ Ms, $K_D = 1$ µs	Case 2: $K_P = 6.9$, $K_I = 1.90$ Ms, $K_D = 5$ µs	Case 3: $K_P = 8$, $K_I = 3$ Ms, $K_D = 5$ µs	Case 4: $K_P = 13$, $K_I = 8.6$ Ms, $K_D = 5$ µs
t_d (µs)	2.6	1.0	1.2	1.0	1.2
t_r (ns)	12.4	2.4	2.6	2.2	2.2
t_p (µs)	12.4	4.0	4.6	4.4	4.4
p_o (mV)	87	107.8	118.75	125.95	137.82
M_p (%)	0	7.8	18.75	25.95	37.82
t_s at 2% (µs)	10	7.0	9.8	9.4	13.6
t_s at 5% (µs)	8.2	5.6	7.0	8.4	11.6

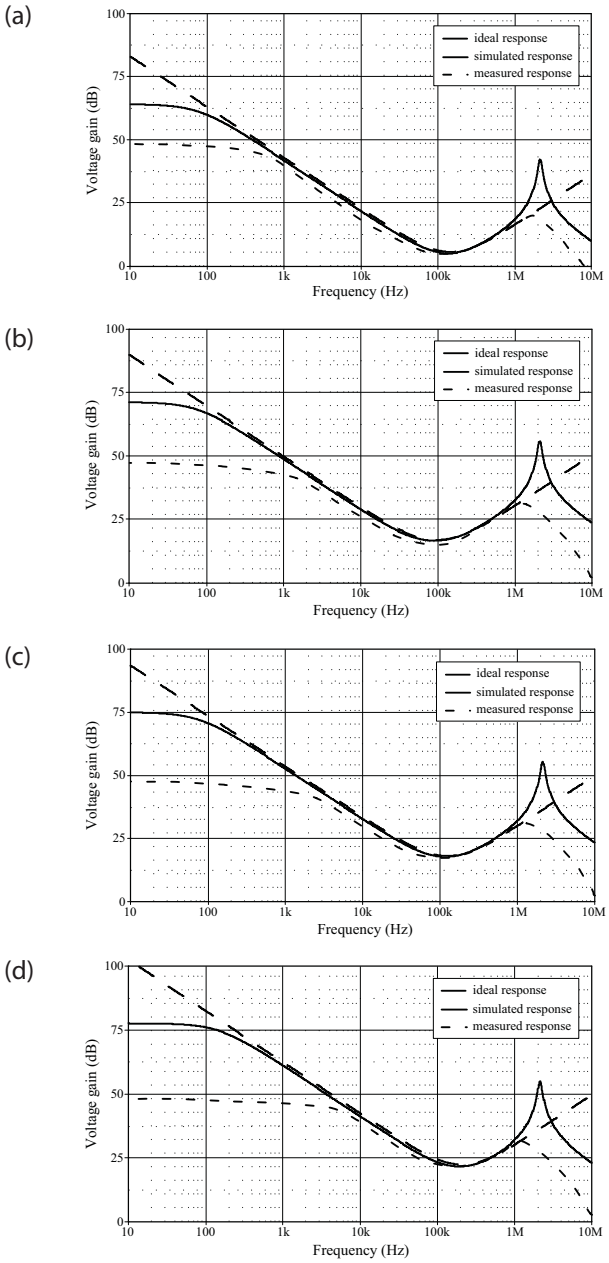

Figure 15: Frequency-domain performance of the closed-loop system in Fig.9 with variable controller gains. (a) Case 1; (b) Case 2; (c) Case 3; (d) Case 4

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