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A New Quantum-Based Building Block for Designing a Nano-Circuit with Lower Complexity

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Abstract: Next-generation nano-scale computational systems are being hampered by two significant obstacles: shrinking transistor size and power dissipation. Moore's law does not hold when transistor size reaches the atomic level. So, it becomes necessary to investigate alternative technologies that surpass traditional Complementary Metal Oxide Semiconductor (CMOS) technology's physical constraints. Quantum Dot Cellular Automata (QCA), a transistor-free computational paradigm, is thought to be the best alternative to CMOS technology for designing nano-scale logic circuits. However, not many designs cut energy usage and offer straightforward access to inputs and outputs. Moreover, adders, the primary component in logic circuits and digital arithmetic, are crucial in developing several efficient QCA designs. In this context, the 4-bit Ripple Carry Adder (RCA) is a straightforward type of adder that can help produce circuits with minimal necessary space and power consumption because of its exceptional qualities. The synthesis of high-level logic further demonstrates the design's effectiveness. The outcomes of QCADesigner demonstrated that the proposed circuits are less complicated and use less power than earlier designs compared to conventional design approaches.

Keywords: Nanotechnology; Quantum-dot cellular automata; XOR gate; Majority voter gate; Full adder; Ripple Carry Adder

Nov gradnik na kvantni osnovi za načrtovanje nano vezja z manjšo kompleksnostjo

Izvleček: Računalniške sisteme naslednje generacije v nano merilu ovirata dve pomembni oviri: zmanjševanje velikosti tranzistorjev in razprševanje energije. Moorov zakon ne velja, ko velikost tranzistorja doseže atomsko raven. Zato je treba raziskati alternativne tehnologije, ki presegajo fizikalne omejitve tradicionalne tehnologije kovinsko oksidnih polprevodnikov (CMOS). Quantum Dot Cellular Automata (QCA), računska paradigma brez tranzistorjev, naj bi bila najboljša alternativa tehnologiji CMOS za načrtovanje logičnih vezij nano velikosti. Vendar pa ni veliko zasnov, ki bi zmanjšale porabo energije in omogočile neposreden dostop do vhodov in izhodov. Poleg tega so seštevalniki, glavna komponenta v logičnih vezjih in digitalni aritmetiki, ključni pri razvoju več učinkovitih zasnov QCA. V tem kontekstu je 4-bitni Ripple Carry Adder (RCA) enostavna vrsta seštevalnika, ki lahko zaradi svojih izjemnih lastnosti pomaga pri izdelavi vezij z minimalno potrebnim prostorom in porabo energije. Sinteza logike visoke ravni dodatno dokazuje učinkovitost zasnove. Rezultati programa QCADesigner so pokazali, da so predlagana vezja manj zapletena in porabijo manj energije kot prejšnje zasnove v primerjavi z običajnimi pristopi načrtovanja.

Ključne besede: nanotehnologija; kvantni točkovni celični avtomati; vrata xor; vrata večinskega volivca; popolni seštevalnik; ripple carry adder

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1 Introduction

High leakage power and sub-node scaling of 22 nm technology are issues that transistor-based technologies must deal with [1]. These problems motivate designers of Very Large-Scale Integration (VLSI) to create a different technology for the next Integrated Circuits (ICs) and diode-based technologies [2-4]. To address the issues with CMOS technology [5], VLSI designers are looking into a number of other technologies, including Quantum-dot Cellular Automata (QCA), single

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electron transistors, and tunnel field effect transistors. Compared to competing technologies, QCA technology provides a number of advantages, including a smaller footprint need, quick switching times, and reduced power dissipation [6].

QCA is a very intriguing and well-liked technology for creating nano-scale logic circuits. There are no transistors in the QCA technology. The QCA cell, which comprises 4 quantum dots, is the fundamental unit of QCA [7]. This method is energy-efficient since there is no actual charge movement between QCA cells. Logical values are determined based on the electrons' location in quantum dots. Due to Coulombic contact, electrons in a QCA cell are situated at the opposing corners. There are two logics 1 or 0 values in each cell. On the other hand, these advantages led researchers to develop a number of projects that explain how to construct QCA circuits [8]. Adders, SRAM [9], ALUs, switching, encoder-decoders [10], reversible logic, and memories are just a few of the recently invented circuits. Full adders play a very prominent part in digital circuits since they are employed in the creation of logical and mathematical processes [11]. Therefore, building a QCA-based adder with reduced space, shorter delays, straightforward access to inputs and outputs, and lower complexity will be more crucial than ever [11]. This paper uses a novel, low-complexity, and low-power three-layer full adder circuit to suggest a new QCA-based ripple carry adder (RCA) design for improving the previous designs. With simple access to inputs and outputs, XOR and majority gates were used to create an RCA circuit, and the results were compared to earlier designs. All protected Nano-communication networks [12] are designed using adders and RCA designs. QCADesigner-E as a usually used tool for power analysis, will be utilized in this paper for simulation and assessment.

The structure of this essay is as follows. The background of QCA is presented in Section 2, with a focus on its distinctive cells. The 4-bit RCA's detailed architecture is shown in Section 3. Section 4 displays the simulation's findings. Finally, the paper is concluded in the last section.

2 QCA background and related works

This section discusses the important and basic parts of this technology and the best previous works related to the subject.

1.1 QCA Cells and Wires

A QCA cell is a square nanostructure with four quantum dots (micro), roughly as shown in Figure 1(a). In the context of QCA, "micro" refers to the individual components or elements of the system, namely the quantum dots. These quantum dots are the building blocks of QCA and serve as the basic units of information processing [13]. In the cell, a tunnel junction connecting two pairs of quantum dots allows for the passage of two electrons between them. The two electrons are positioned in the cell at opposite ends because of Coulombic repulsion [14, 15]. In the context of QCA (Quantum-dot Cellular Automata), nonlinear and linear refer to different types of behavior exhibited by the system. Linear QCA refers to a system where quantum dots' behavior can be described using linear operations, similar to classical digital logic gates, while nonlinear QCA involves more complex interactions between quantum dots, resulting in nonlinearity due to quantum effects like Coulomb interactions and electron tunneling [16]. There is no cell-to-cell tunneling; tunneling only takes place within the cell. Bisectional behavior results from the interaction of the discrete electronic charge, Coulombic repulsion, and quantum confinement. Binary "0" and "1" with polarisations of "1" and "+1", respectively, can be represented by the two charge configurations. A QCA "wire" is a chain of cells contiguous to one another, as opposed to a physical wire, as depicted in Figure 1 (b). As there are no electron tunnels between cells, QCA offers a method of information transfer without current flow [17].

1.2 QCA Logic Gates

The fundamental gates of QCA are inverters and three-input majority gates. A majority gate comprises 4 cells that achieve the function of M (a, b, and c) = ab+bc+ac, as shown in Figure 2 (a) [18]. Cells are placed diagonally from one another to achieve the inversion functionality, as shown in Figure 2 (b). Inverters and majority gates make up a universal set that can be employed to implement any logic operation. By setting one of the

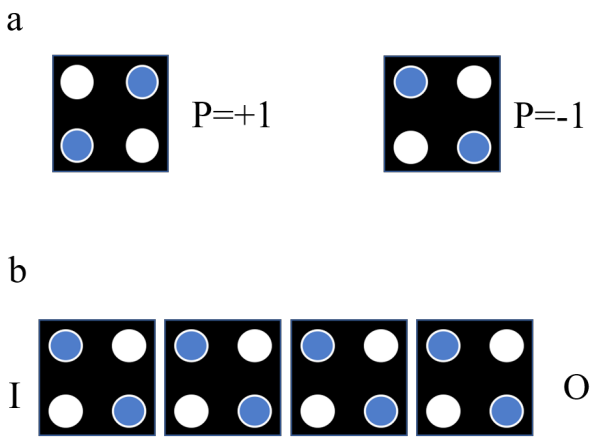

Figure 1: Structure of basic QCA: (a) QCA cells, and (b) QCA wire.

majority gate inputs to "0," for instance, AND (a, b) = M (a, b, 0) = ab, a two-input AND gate is realized. In the same manner, an OR gate is implemented by setting one input to "1," i.e., OR (a,b) =M (a,b,1) = ab + b 1 + a 1 = a + b [19].

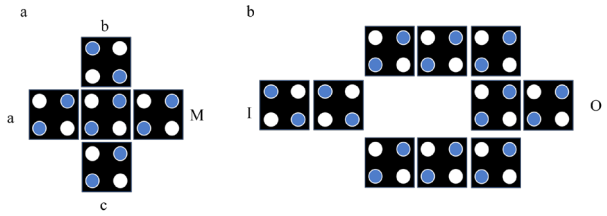

Figure 2: Structure of basic QCA: (a) Three-input majority gate, and (b) Inverter gate.

1.3 QCA Clocking

To drastically reduce metastability issues and enable long pipelines, adiabatic switching is used for QCA clocking. One-half of the wire is used for signal transmission during each clock cycle, and the other half is left unpolarized [20]. The cells in the active clock zone that is still present cause the newly activated cells to become polarized during the subsequent clock cycle, which deactivates half of the previously active clock zone [21]. As a result, signals continue from one clock zone to the next. Four-phase clock signals are used to control four different circuit areas. Each zone of the clock signal has four states: high, low, low to high, and high. When the status changes from high to low, the cell starts to calculate and keeps the value while the state is low. The cell is released when the clock is in the low-to-high state and not operating [22].

1.4 Related work

This section reviews numerous significant and useful recommendations for the design of sophisticated and straightforward QCA RCA circuit designs. Abedi, et al. [23]. propose a cross-level QCA architecture in a full adder QCA design. Additionally, supplied proposed a RCA that is based on this design. Using *QCADesigner*, these designs have been accuracy-tested and assessed. Compared to earlier methods, conventional evaluation methodology and particular cost function QCA were applied for superior performance. The suggested RCA has a delay period of 1.75 clock cycles and uses 262 cells in a 0.208 μm^2 area. Also, Balali and Rezai [14] proposed a QCA structure for the full adder to create a high-speed, efficient, and reliable four-bit RCA using the QCA technology. Their modeling results have demonstrated that there are significant increases in circuit speed and latency. To verify the accuracy of these designs, QCADesigner was employed. The four-bit RCA that is suggested in the QCA technology is designed with minimum complexity and high speed. It has a delay of 1.25 clock cycles and 209 cells in a 0.3 μm^2 area. Also, the fundamental QCA and QCA-based digital design concepts have been put out by Chan, et al. [24]. The creation of straightforward digital logic utilizing certain QCA approaches has been discussed in this article. The four-bit ripple adder has been provided using a combinational notion from the traditional RCA and the CLA. These circuits were implemented utilizing the 5-input majority gate, which theoretically can lower the latency of the traditional QCA-based RCA. The recommended adder has a latency of 3.25 clock cycles, an area of 2.5 μm^2, and 1246 cells. The designed structures have been verified using the QCADesigner. Finally, Hashemi and Navi [25] suggest a reliable QCA and an RCA full adder circuit based on a successful five-input majority gate. These circuits have employed a robust crossover design in comparison to similar designs. Owing to the full adder circuit's efficient architecture, it has been employed for RCA design in a variety of scales. The coherent and bistable simulation engines of the QCADesigner have used to simulate the suggested designs. The proposed RCA uses 442 cells with an area of 1 μm2 and a delay of 2 clock cycles.

2 Proposed design

This part presents and simulates new designs and effective architectures for a one-bit QCA full adder and four-bit QCA RCA. One-bit QCA full adder block diagram is illustrated in Figure 3, and the exploited full adder's QCA-based layout with a three-input majority gate and three-input XOR gate is shown in Figure 4. This complete adder comprises 15 cells and uses 0.5 clock cycles to generate outputs with a 0.01 μm2 area and simple input and output connectivity. This three-layer implementation of a QCA full adder uses ordinary QCA cells. Input cells are A, B, and C, and output cells are COUT and SUM. In this design, the first layer acts as an XOR gate and is used to generate the SUM, while the second layer is utilised to transmit values to the third layer, where all of the circuit's inputs are applied and the COUT output is generated.

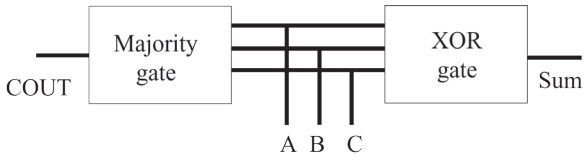

Figure 3: QCA-based full adder diagram

The proposed adder can easily implement the higher adder designs. Higher adders, such as 4-bit RCA, have been designed using this Complete adder with fewer QCA cells, which is entirely distinct from earlier ver-

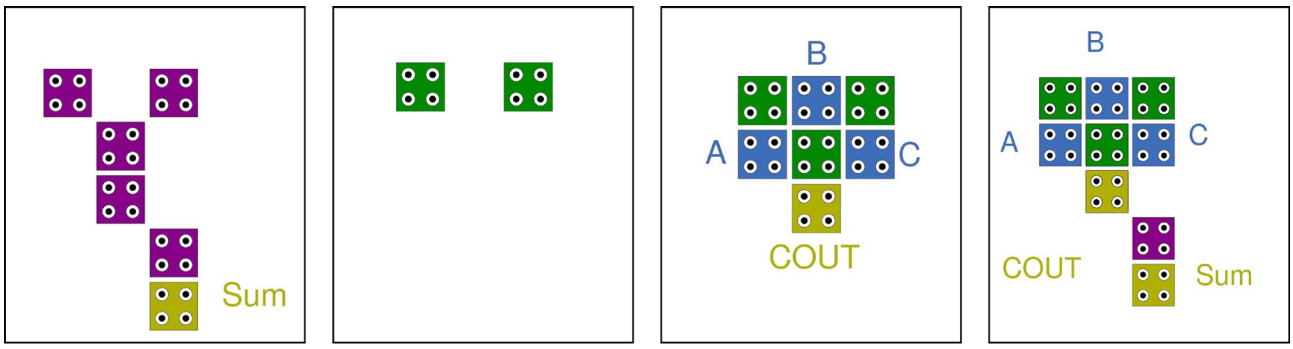

Figure 4: QCA-based full adder layouts and layers

sions. The proposed four-bit RCA design is illustrated in Figure 5 with its structure. Also, a four-bit QCA-based RCA that uses four one-bit full adder QCA-based circuits as its structural unit is also depicted in Figure 6. The 72 cells in the suggested four-bit QCA-based RCA have an area of 0.11 μm^2 and a delay of 1.75 clock cycles. All of the inputs and outputs on this three-layer circuit are accessible. There are five outputs (S0-S3, COUT) and 9 inputs (A0-A3, B0-B3, C). The outputs in this design are easily accessible because they are not encircled by other cells. To transfer signal output, this structure does not need a wire in other words. Thus, it is simple to feed the outputs to another QCA input.

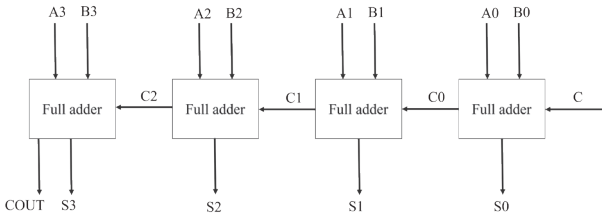

Figure 5: The proposed schematic for 4-bit RCA

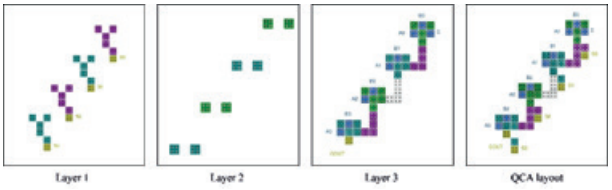

Figure 6: Three layers of the proposed QCA-based 4-bit RCA

3 Simulation tool and results

The software QCADesigner-E is used in this paper to simulate the suggested design [26]. Fast design, layout, and simulation of QCA circuits are made possible by QCADesigner software. Table 1 contains all of the simulation parameters for the simulated objects. The default parameters for all simulation measures and conditions are used in this tool [27].

Table 1: Simulation parameters

Parameter	Bistable approximation engine Value	Coherence Vector engine Value
Cell size	18 *18 nm^2	18 *18 nm^2
Radius of effect	65 nm	80 nm
Relative permittivity	12.9000000	12.9000000
Clock high	9.8e−22J	9.8e−22J
Clock low	3.8e−23J	3.8e−23J
Clock amplitude factor	2.000000	2.000000
Clock shift	0.000000e+000	0.000000e+000
Layer separation	11.5000 nm	11.5000 nm
Maximum iterations per sample	100	-
Number of samples	12800	-
Convergence tolerance	0.001000	-

The constructed full adder circuit simulation results are shown in Figure 7. All possible states have been applied to the circuit's inputs, and the outputs have created the desired outcomes, as shown in the correct table. Both outputs are formed concurrently after two clock cycles. The third layer of this full adder, designed in three layers, receives the three inputs and processes them to produce the COUT output from the third layer and the SUM output from the first layer. The accuracy of the suggested designs was demonstrated by these simulations, which were run using the default settings. Tables 2 and 3 compare the supplied full adder and RCA circuit cell, latency, and space usage to the best previous designs.

Table 2: Comparisons among the designs

Designs	Area (μm^2)	Cells	Delay (Clock cycle)
Proposed design	0.01	15	0.5
Ahmadpour, et al. [28]	0.01	20	0.5
Seyedi and Navimipour [6]	0.01	22	0.75
Sarmadi, et al. [29]	0.04	30	1.0
Sayedsalehi, et al. [30]	0.02	33	0.75

Figure 8 displays the simulation results for the QCA-based RCA circuit. The circuit generates the proper output when subjected to every possible condition. Actually, Figure 8 displays the outcomes of the simulation for the variables A0, A1, A2, A3, B0, B1, B2, B3, and C. As depicted in the figure, the circuit receives input from all potential states and generates the desired output. Also, simulation results show strong polarization of the output cells for this circuit.

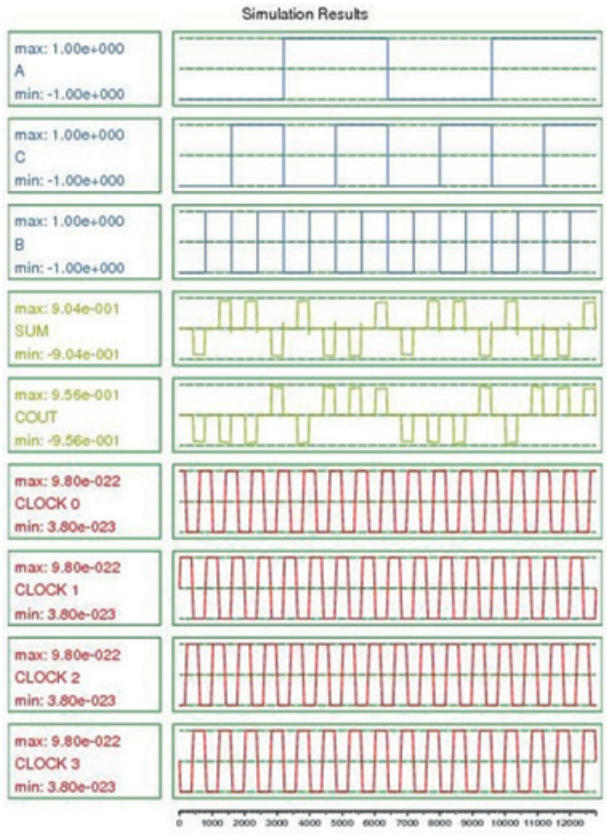

Figure 7: Simulation outcomes of the proposed design

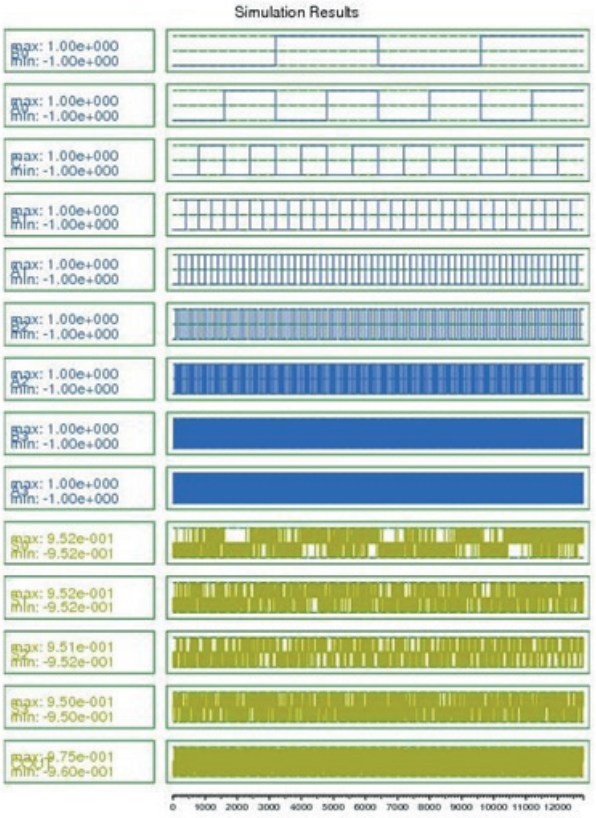

Figure 8: Simulation result of the proposed RCA

Table 3: Comparisons among the RCA designs

Designs	Area (μm^2)	Cells	Delay (Clock cycle)
Proposed design	0.11	72	1.75
Balali and Rezai [31]	0.3	209	1.25
Sonare [32]	0.51	366	2/5
Rashidi and Rezai [33]	0.14	175	1
Abedi, et al. [23]	0.208	262	1.75
Mohammadi, et al. [34]	0.24	237	1.5
Labrado and Thapliyal [35]	0.3	295	1.5

Table 4: Comparison of total and average energy dissipation

Designs	Power and energy analysis	
	Total energy dissipation (eV)	Average energy dissipation (eV)
Proposed full adder design	1.458	1.057
Ahmadpour, et al. [28]	1.25	1.15
Seyedi and Navimipour [6]	1.55	1.56
Sarmadi, et al. [29]	1.80	1.87
Sayedsalehi, et al. [30]	1.69	1.55
Proposed RCA design	2.80	2.63
Balali and Rezai [31]	2.48	2.59
Sonare [32]	2.74	2.70
Rashidi and Rezai [33]	3.02	2.98
Abedi, et al. [23]	3.56	3.15
Mohammadi, et al. [34]	2.89	3.12
Labrado and Thapliyal [35]	2.485	2.84

Additionally, we compared the suggested designs in Table 4 to the best current designs in terms of Total energy dissipation (eV) and Average energy dissipation in order to better comprehend and compare circuits (eV). It is obvious that the current design is the most energy-efficient one.

4 Conclusion and future works

A new and emerging technology that plays a significant role in nanotechnology and has been researched for years is QCA technology. Considering the advantages of QCA, such as fast switching time, low power requirement, and high device density, it can be a good alternative. According to the cases mentioned in this article, this technology has been used to implement adder circuits. In fact, it creates an innovative architecture for a 1-bit QCA full adder. Then, applying this innovative full adder layout, a high-speed adder is developed as a 4-bit RCA. Our study effort is shown to provide fewer cells and smaller areas with realistic simulation results compared to the newly published collector architecture. The presented multi-layer architecture is significantly more durable than the conventional full adder.

The suggested full adder consists of 15 cells and achieves output generation in 0.5 clock cycles. It occupies an area of 0.01 μm^2 and features straightforward input and output connectivity. Additionally, the suggested four-bit QCA-based RCA incorporates 72 cells, covering an area of 0.11 μm^2. The RCA exhibits a delay of 1.75 clock cycles. In this study, QCADesigner-E assessed the total power dissipation of the QCA structure. These circuits have one of the best power consumption rates and are easily accessible to the inputs and outputs. In the future, high-speed adders can be designed that play an essential role in multi-layer designs and further improve computational performance. High-performance QCA circuits and an n-bit ripple carry adder can be created at the nanoscale using the given effective architectures. The suggested concept may therefore have a fundamental impact on the development of high-speed circuits as well as other forms of adders, such as complete subtractors and borrow ripple subtractors.

5 Conflict of Interest

The authors declare that they have no conflicts of interest.

6 References

1. T. Tuncer, E. Avaroglu, M. Türk, and A. B. Ozer, "Implementation of non-periodic sampling true random number generator on FPGA," Informacije Midem, vol. 44, pp. 296-302, 2014.
2. M. A. S. Bhuiyan, "CMOS series-shunt single-pole double-throw transmit/receive switch and low noise amplifier design for internet of things based radio frequency identification devices," Informacije MIDEM, vol. 50, pp. 105-114, 2020.
3. H. Tian, J. Liu, Z. Wang, F. Xie, and Z. Cao, "Characteristic Analysis and Circuit Implementation of a Novel Fractional-Order Memristor-Based Clamping Voltage Drift," Fractal and Fractional, vol. 7, p. 2, 2022.
4. J. Xiang, W. Yang, H. Liao, P. Li, Z. Chen, and J. Huang, "Design and thermal performance of thermal diode based on the asymmetric flow resistance in vapor channel," International Journal of Thermal Sciences, vol. 191, p. 108345, 2023.
5. S. Li, J. Chen, X. He, Y. Zheng, C. Yu, and H. Lu, "Comparative study of the micro-mechanism of charge redistribution at metal-semiconductor and semimetal-semiconductor interfaces: Pt (Ni)-MoS2 and Bi-MoS2 (WSe2) as the prototype," Applied Surface Science, vol. 623, p. 157036, 2023.

6. S. Seyedi and N. J. Navimipour, "An optimized design of full adder based on nanoscale quantum-dot cellular automata," Optik, vol. 158, pp. 243-256, 2018.
7. S. Seyedi and N. J. Navimipour, "Designing a three-level full-adder based on nano-scale quantum dot cellular automata," Photonic Network Communications, vol. 42, pp. 184-193, 2021.
8. S. Seyedi and N. Jafari Navimipour, "Designing a multi-layer full-adder using a new three-input majority gate based on quantum computing," Concurrency and Computation: Practice and Experience, vol. 34, p. e6653, 2022.
9. A. Yan, J. Xiang, A. Cao, Z. He, J. Cui, T. Ni, et al., "Quadruple and Sextuple Cross-Coupled SRAM Cell Designs With Optimized Overhead for Reliable Applications," IEEE Transactions on Device and Materials Reliability, vol. 22, pp. 282-295, 2022.
10. W. Dang, S. Liao, B. Yang, Z. Yin, M. Liu, L. Yin, et al., "An encoder-decoder fusion battery life prediction method based on Gaussian process regression and improvement," Journal of Energy Storage, vol. 59, p. 106469, 2023.
11. A. Kamaraj and P. Marichamy, "Design of fault-tolerant reversible floating point division," Informacije MIDEM, vol. 48, pp. 161-172, 2018.
12. Z. Qu, X. Liu, and M. Zheng, "Temporal-Spatial Quantum Graph Convolutional Neural Network Based on Schrödinger Approach for Traffic Congestion Prediction," IEEE Transactions on Intelligent Transportation Systems, 2022.
13. X. Jianhua, D. Liangming, C. Zhou, H. Zhao, J. Huang, and T. Sulian, "Heat Transfer Performance and Structural Optimization of a Novel Microchannel Heat Sink," Chinese Journal of Mechanical Engineering= Ji xie gong cheng xue bao, vol. 35, 2022.
14. A. Kamaraj, P. Marichamy, and R. Abirami, "MULTI-PORT RAM DESIGN IN QCA USING LOGICAL CROSSING," Informacije MIDEM, vol. 51, pp. 49-61, 2021.
15. J. Gao, H. Sun, J. Han, Q. Sun, and T. Zhong, "Research on recognition method of electrical components based on FEYOLOv4-tiny," Journal of Electrical Engineering & Technology, vol. 17, pp. 3541-3551, 2022.
16. S. Xu, H. Dai, L. Feng, H. Chen, Y. Chai, and W. X. Zheng, "Fault Estimation for Switched Interconnected Nonlinear Systems with External Disturbances via Variable Weighted Iterative Learning," IEEE Transactions on Circuits and Systems II: Express Briefs, 2023.
17. S. Seyedi, B. Pourghebleh, and N. Jafari Navimipour, "A new coplanar design of a 4-bit ripple carry adder based on quantum-dot cellular automata technology," IET Circuits, Devices & Systems, vol. 16, pp. 64-70, 2022.
18. R. M. Macrae, "Mixed-valence realizations of quantum dot cellular automata," Journal of Physics and Chemistry of Solids, vol. 177, p. 111303, 2023.
19. M. Kikelj, B. Lipovšek, and F. Smole, "Orthodox Theory Monte-Carlo Simulation of Single-Electron Logic Circuits," Informacije MIDEM, vol. 48, pp. 241-247, 2018.
20. J. Wang, J. Tian, X. Zhang, B. Yang, S. Liu, L. Yin, et al., "Control of time delay force feedback teleoperation system with finite time convergence," Frontiers in Neurorobotics, vol. 16, 2022.
21. A. Asthana, A. Kumar, and P. Sharan, "N× N Clos Digital Cross-Connect Switch Using Quantum Dot Cellular Automata (QCA)," Computer Systems Science & Engineering, vol. 45, 2023.
22. S. Riyaz and V. K. Sharma, "Design of reversible Feynman and double Feynman gates in quantum-dot cellular automata nanotechnology," Circuit world, vol. 49, pp. 28-37, 2023.
23. D. Abedi, G. Jaberipur, and M. Sangsefidi, "Coplanar full adder in quantum-dot cellular automata via clock-zone-based crossover," IEEE transactions on nanotechnology, vol. 14, pp. 497-504, 2015.
24. S. T. Y. Chan, C. F. Chau, and A. bin Ghazali, "Design of a 4-bit ripple adder using Quantum-dot Cellular Automata (QCA)," in Circuits and Systems (ICCAS), 2013 IEEE International Conference on, 2013, pp. 33-38.
25. S. Hashemi and K. Navi, "A novel robust QCA full-adder," Procedia Materials Science, vol. 11, pp. 376-380, 2015.
26. M. Patidar, U. Singh, S. K. Shukla, G. K. Prajapati, and N. Gupta, "An ultra-area-efficient ALU design in QCA technology using synchronized clock zone scheme," The Journal of Supercomputing, vol. 79, pp. 8265-8294, 2023.
27. D. Manna, C. Mukherjee, A. Banerjee, M. Dhar, S. Panda, and B. Maji, "Towards Energy-Efficient Cost-Effective Toffoli Gate Design using Quantum Cellular Automata," in 2023 IEEE Devices for Integrated Circuit (DevIC), 2023, pp. 56-60.
28. S.-S. Ahmadpour, M. Mosleh, and S. R. Heikalabad, "A revolution in nanostructure designs by proposing a novel QCA full-adder based on optimized 3-input XOR," Physica B: Condensed Matter, vol. 550, pp. 383-392, 2018.
29. S. Sarmadi, S. Sayedsalehi, M. Fartash, and S. Angizi, "A structured ultra-dense QCA one-bit full-adder cell," Quantum Matter, vol. 5, pp. 118-123, 2016.
30. S. Sayedsalehi, M. H. Moaiyeri, and K. Navi, "Novel efficient adder circuits for quantum-dot cellular automata," Journal of Computational and Theoretical Nanoscience, vol. 8, pp. 1769-1775, 2011.

31. M. Balali and A. Rezai, "Design of Low-Complexity and High-Speed Coplanar Four-Bit Ripple Carry Adder in QCA Technology," International Journal of Theoretical Physics, vol. 57, pp. 1948-1960, July 01 2018.
32. N. Sonare, "Design and Simulation Study of Coplanar Full Adder and Ripple Carry adder using Quantum Dot Cellular Automata," 2018.
33. H. Rashidi and A. Rezai, "High-performance full adder architecture in quantum-dot cellular automata," The Journal of Engineering, vol. 1, 2017.
34. M. Mohammadi, M. Mohammadi, and S. Gorgin, "An efficient design of full adder in quantum-dot cellular automata (QCA) technology," Microelectronics Journal, vol. 50, pp. 35-43, 2016.
35. C. Labrado and H. Thapliyal, "Design of adder and subtractor circuits in majority logic-based field-coupled QCA nanocomputing," Electronics letters, vol. 52, pp. 464-466, 2016.

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