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Charge Configuration Memory (CCM) device – a novel approach to memory

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Abstract: Computer technologies have advanced unimaginably over the last 70 years, mainly due to scaling of electrical components down to the nanometre regime and their consequential increase in density, speed and performance. Decrease in dimensions also brings about many unwanted side effects, such as increased leakage, heat dissipation and increased cost of production. However, it seems that one of the biggest factors limiting further progress in high-performance computing is the increasing difference in performance between processors and memory units, a so-called processor-memory gap. To increase the efficiency of memory devices, emerging alternative non-volatile memory (NVM) technologies could be introduced, promising high operational speed, low power consumption and high density. This review focuses on a conceptually unique non-volatile Charge Configuration Memory (CCM) device, which is based on resistive switching between different electronic states in a 1T-TaS_2 crystal. CCM demonstrates ultrafast switching speed <16 ps, very low switching energy (2.2 fJ/bit), very good endurance and a straightforward design. It operates at cryogenic temperatures, which makes it ideal for integration into emerging cryo-computing and other high-performance computing systems such as superconducting quantum computers.

Keywords: Charge Configuration Memory (CCM); 1T-TaS_2; Ultrafast devices; Charge density wave (CDW)

Spominska naprava na podlagi konfiguracije naboja (CCM) – nov pristop do spomina

Izvleček: Računalniške tehnologije so v zadnjih 70-tih letih neverjetno napredovale, predvsem zaradi pomanjševanja električnih komponent na nanometrske dimenzije in posledičnega povečanja gostote, hitrosti in zmogljivosti računalniških vezij. Zmanjševanje dimenzij pa vodi tudi do nezaželenih stranskih učinkov, kot so povečano tokovno puščanje, visoka disipacija toplote in povečani stroški izdelave. Vendar eden največjih vzrokov, ki zavira napredek v visokozmogljivem računalništvu, je vse večja razlika v zmogljivosti med procesorji in spominskimi enotami, oz. t. i. procesorsko-spominska vrzel. Vpeljava novih alternativnih trajnih spominskih (NVM) tehnologij bi lahko povečala učinkovitost, hitrost in gostoto spominskih naprav. Ta pregledni članek opisuje konceptualno novo trajno spominsko napravo na podlagi konfiguracije naboja (CCM), ki temelji na uporovnem preklapljanju med različnimi elektronskimi stanji v kristalu 1T-TaS_2. CCM naprava izraža ultra hitre preklopne čase <16 ps, zelo nizko preklopno energijo (2.2 fJ/bit), zelo dobro vzdržljivost in preprost dizajn. Obratuje pri kriogenih temperaturah, kar jo naredi idealno za integracijo v uveljavljajoče področje krio-računalništva in ostale visokozmogljive računalniške sisteme, kot so npr. superprevodni kvantni računalniki.

Ključne besede: Spomin na podlagi konfiguracije naboja (CCM); 1T-TaS_2; Ultra hitre naprave; Val gostote naboja (CDW)

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1 Introduction

Advances in computer technologies were made possible due to enormous investments of money, time and man-power into research and development of silicon semiconductor technology, which has been very successful with the constant upgrades despite all the problems it has been facing [1], [2]. However, to sustain

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this progress in high-performance computing in the long run, it seems that new alternative technologies have to be introduced to either complement the existing ones or to develop new directions. Augmenting Si CMOS with two-dimensional or memristive materials could produce more efficient 2D transistors, sensors and interconnections [3] or even new technological concepts such as biologically inspired computing and on-chip memory and storage [4]. On the field of memory technologies there is much room for improvement, especially when it comes to efficiency and power consumption. Standard dynamic random-access memory (DRAM) circuits can use up to 30 % of total power consumption [5] of the whole computer system due to constant refreshing and even static random-access memory (SRAM) circuits suffer losses from leakage [6]. Introduction of non-volatility [7] with the combination of a high energy efficient information storing mechanism could result in a memory device of the future. Charge configuration memory (CCM) devices presented here rely on reconfiguration of electronic domains between the ground state and excited metastable hidden (H) state that was recently discovered in a layered transition metal dichalcogenide 1T-TaS_2 crystal [8]. Switching between different electronic states results in a big change of electrical resistance of the device. This review briefly explains the origin of the emergent metastable H state in 1T-TaS_2 and discusses its properties in the content of a novel non-volatile memory device based on reconfiguration of charge.

2 1T-TaS_2 and the phase diagram

The active element in the CCM device is a 1T-TaS_2 crystal, which belongs to the group of transition metal dichalcogenides (TMDs) with a chemical formula MX_2, where M is a transition metal atom (Ta, Mo, W, Ti…) and X is a chalcogen atom (S, Se or Te). One layer of 1T-TaS_2 is made from two triangular lattices of S atoms with a triangular lattice of Ta atoms in between. There are strong covalent bonds inside the layer and weak van der Waals bonds in between the layers. This leads to strong anisotropy of the material which shows in different mechanical, thermal and electrical characteristics. Pronounced quasi 2D characteristic gives birth to interesting new physics not observable in three-dimensional materials [3], [9].

The phase diagram of 1T-TaS_2 is very rich, exhibiting different charge-density-wave (CDW) states, Mott transition, polaronic ordering [10], metastable state [8] and even superconductivity at higher pressures [11]. At temperatures above 540 K, the material behaves as a simple metal, but when cooled down below that temperature it undergoes a phase transition into an incommensurate (IC) CDW due to a combination of Coulomb repulsion [12] and Fermi surface nesting [13]. At this point the charge density inside the crystal is modulated and the crystal lattice is displaced, but the two of them are not aligned. Because of the frustration between the IC CDW and the underlying lattice, the state transforms into a nearly commensurate (NC) CDW at a temperature around 340 K. Electrical resistance of the material in NC state is several times higher than in the metallic state but it is still well conducting [11]. Steady state electrical resistance of the material is shown in Fig. 1a, where

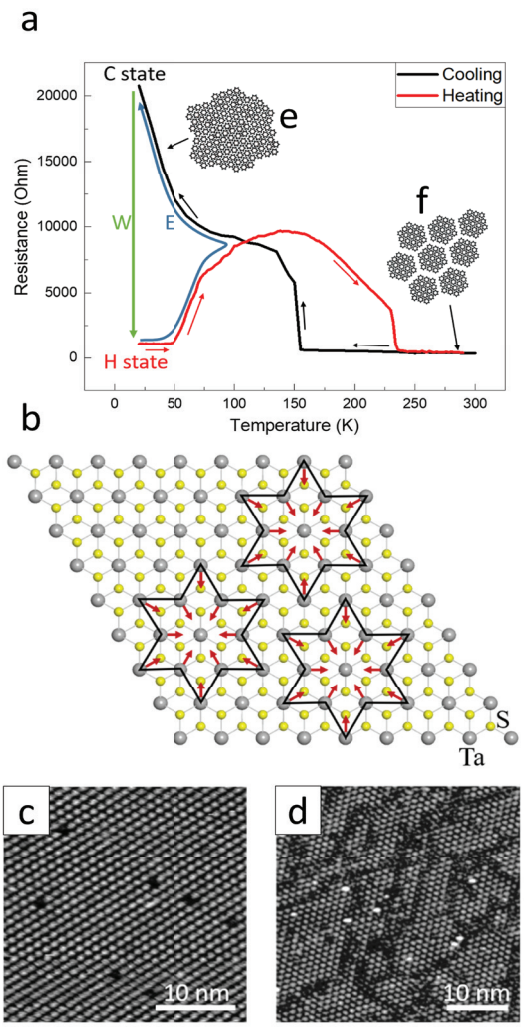

Figure 1: Phase diagram of 1T-TaS_2. a) Plot of resistance versus temperature. Black curve represents cooling of the CCM device and red curve represents heating after switching to the H state. Write (W) process is denoted with a green arrow, erase (E) process is denoted with a blue arrow. b) Formation of a polaron. 12 surrounding Ta atoms are slightly displaced toward the middle one. c) An STM image of the C state with an ordered polaronic structure. d) An STM image of the H state with patches of polarons seperated with domain walls. e) Sketch of the C state. f) Sketch of the NC state.

the black curve represents resistance upon cooling from room temperature. NC CDW state is made from a hexagonal array of polaron clusters, separated with domain walls, as is sketched in Fig. 1f (inset to Fig. 1a). A polaron consists of a central electron localised on a Ta atom with 12 surrounding Ta atoms displaced toward the centre [14], [15], which forms a star formation (Fig. 1b). Upon slow cooling below 160–180 K, domain walls between polaron clusters disappear and a fully commensurate (C) CDW polaronic lattice forms. Fig. 1e (inset to Fig. 1a) shows a sketch of the C state and Fig. 1c shows an image of the C state using a scanning tunnelling microscope (STM). Each bright spot represents an individual polaron and the dark spots are impurities in the lattice. C CDW state is a Mott insulator with a gap of 0.1 eV [13]. This leads to a jump in electrical resistance of the sample at ~160–180 K, which further increases as the temperature is decreased to ~20 K, as can be seen on Fig. 1a (black curve). 20 K or lower is a typical working temperature for CCM devices. If the C state is heated up from 20 K to room temperature, the resistance curve backtracks to ~100 K but then follows the red curve and draws a hysteresis until ~220 K. The material then transitions into a so-called stripped ordered triclinic (T) phase [14] before returning to the NC state at ~280 K.

If the C state is excited by either an optical [8] or an electrical [16] pulse, the material switches to a metastable hidden (H) state, which is stable at low temperatures (<20 K). When this transition occurs, the electrical resistance of the sample drops sharply because the H state is metallic. Transition from the C to the H state is called a Write (W) process, which is denoted with a green arrow in Fig. 1a. The contrast in resistance between the two states is dependent on the sample and on the geometries of the CCM device and can be up to three orders of magnitude big [8].

Upon heating the H state (red curve), the resistance remains approximately constant up to 50 K, at which point it starts to increase and merges with the virgin resistance curve (black) at ~100 K. If the sample is cooled down at that point, the resistance follows the virgin curve, meaning the H state is completely reversed into the C state. The transition from the H to the C state is called an Erase (E) process and is denoted in Fig. 1a with a blue curve. The H state can also be erased via Joule's heating of the material using a train of optical pulses [8] or a longer electrical pulse [16], [17].

Examining the H state microscopically using an STM, a distinct patchy pattern can be observed with domains of polarons and domain walls separating them [18], as seen in Fig. 1d. Domain walls arise because the extra injected charge introduced by the external excitation (optical or electrical) is accommodated in the C CDW structure. The charge periodicity of the metastable state (which determines the domain size) originates from a free energy minimum which arises from the competition of Coulomb interaction between domain walls and the energy of the domain wall crossings in the CDW state [8]. The conduction mechanism of the metallic H state is not yet completely understood, but scanning tunnelling spectroscopy (STS) reveals that both polarons and domain walls are conducting [19]. This means that the conduction is not percolative as in typical memristors [20], but is collective in nature. By analysing the junctions between domain walls in the STM image (Fig. 1d) it is discovered that some of them act as non-trivial topological defects (NTTDs), which means they can only be annihilated by an antidefect with equal and opposite winding number. These NTTDs contribute to the non-volatility of the LO state [17], [18] at low temperatures. The pattern of domain walls in the H state is also always different when switching between the C and the H state. This is important for reproducibility and endurance of the devices, because it means that pinning by lattice defects or impurities does not play a significant role in the switching process. Endurance measurement shows that the devices are very durable and can survive well over 10^6 cycles of W and E with remarkable stability throughout [17].

During the transition from the C to the H state (W process) only the charges are reconfigured. This switching is therefore purely electronic and predicted to occur on an electronic timescale (~300 fs). The transition time of the W process was measured using coherent time-resolved femtosecond spectroscopy by Ravnik *et al* [21] in a pump-probe experiment at 160 K. At this temperature the lifetime of the H state is ~0.1 ms [22]. This allows for a stroboscopic measurement with 1 kHz repetition rate laser, which means that before each next laser pulse, the H state has completely relaxed back to the C state. It was determined that the transition time of the W process is ~400 fs, which confirms the assumption. This shows that the W process is inherently extremely fast and is not the limiting factor when it comes to the speed of the CCM device. The E process on the other hand is predominantly thermal and slower and requires more effort and planning to reach optimal operation.

3 Operational properties of the CCM device

3.1 Current-voltage characteristics

A typical CCM device is shown in Fig. 2a with a 1T-TaS_2 flake on Si/SiO_2 substrate and metal electrodes

fabricated on top using electron-beam lithography. Current-voltage (I-V) characteristics of such a CCM device is shown in Fig. 2b and c for both the Write and Erase process respectively, measured at 20 K. Since the C state is the insulating state, it is denoted as the high resistance state (HI) and H state is metallic, so it is called the low resistance state (LO). For a W process, CCM is originally in the HI state. As the current incrementally increases, the voltage follows the HI curve (black) in Fig. 2b. It is linear at first but becomes non-linear at higher currents. Non-linearity is fitted as

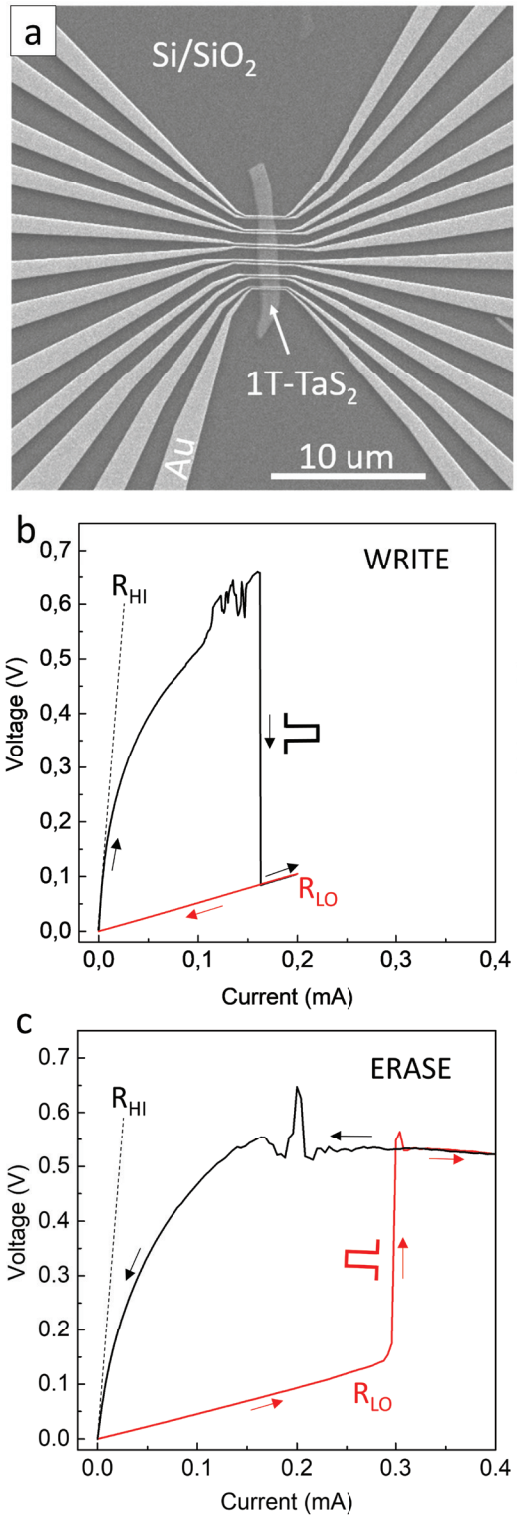

Figure 2: a) Typical CCM device. 1T-TaS_2 crystal on Si/SiO_2 substrate with golden electrodes fabricated on top. b and c) I-V characteristics of the W and E process respectively.

$$\frac{I}{I_0} = exp\left(\frac{V}{V_0}\right) \tag{1}$$

Voltage increases until a certain threshold of current is reached, at which point a switch to the LO state occurs, and the voltage drops. As the current is decreased back to zero, voltage follows a linear LO curve (red). E process is done similarly, only that the device starts from the LO state (Fig. 2c). As the current incrementally increases, the voltage follows a linear LO curve (red) until a certain threshold is reached, at which point a switch to the HI state occurs and the voltage jumps. As the current is decreased the voltage follows the non-linear HI curve back (black). The threshold values for W and E processes can vary slightly between devices but can be controlled with proper planning. Read operation (R) is straightforward, any read current can be used as long as it's low enough to not trigger the W or E operation.

The HI state shows clear non-linear behaviour which cannot be fitted with a tunnelling diode equation or attributed to CDW sliding behaviour [16], [23]. Steps or jumps in voltage in the HI state are case dependant and are attributed to complex tunnelling dynamics between polarons and slight rearrangements of the polaronic structure [16], [24] with similar resistance. However, the CCM device is not meant to be driven in this manner, but rather by using a single W and E pulse above the threshold value to switch between the HI and LO state. In devices that are well characterized, the potentially unknown region of the I-V characteristics can be easily avoided.

3.2 Writing process

W process can be observed in real time with the use of an oscilloscope connected in parallel to a CCM element as shown on a scheme in Fig. 3a. The 1T-TaS_2 flake used was 65 nm thick and 0.9 um wide, with Au electrodes fabricated over the flake and the gap between the electrodes ~280 nm. In Fig. 3b we see the time evolution of voltage across the CCM device when 50 ns long W pulses of varying amplitude are applied on the electrodes at 100 K. At low amplitudes the voltage remains constant over the entire duration of the pulse with the rise time τ_R~7.4 ns defined by the RC constant of

the circuit. At a certain threshold (~0.55 V) the voltage across the CCM drops, which is a result of a W process from HI to LO state and remains there till the end of the pulse. If the area under the voltage curves (coloured in Fig. 3b) is integrated and the W energies are calculated using the equation $E_W = \int_{t1}^{t2} (U^2 / R) dt$, where t_1 is the beginning of the pulse, t_2 is the time where the voltage drops and R is the resistance of the sample, it turns out that the energies for different amplitudes are not the same, meaning the switching does not occur due to cumulative heating. This is also confirmed in Fig. 3c where there is a clear decrease in W energy as the switching pulses are shortened from 400 ns to 9 ns. If switching was only due to heating, the W energy would be constant across all the pulse widths. The mechanism for W switching is not yet completely understood but it seems to be a combination of applied electric field and charge injection into the sample [8], [16], however heating might play a role to a certain degree.

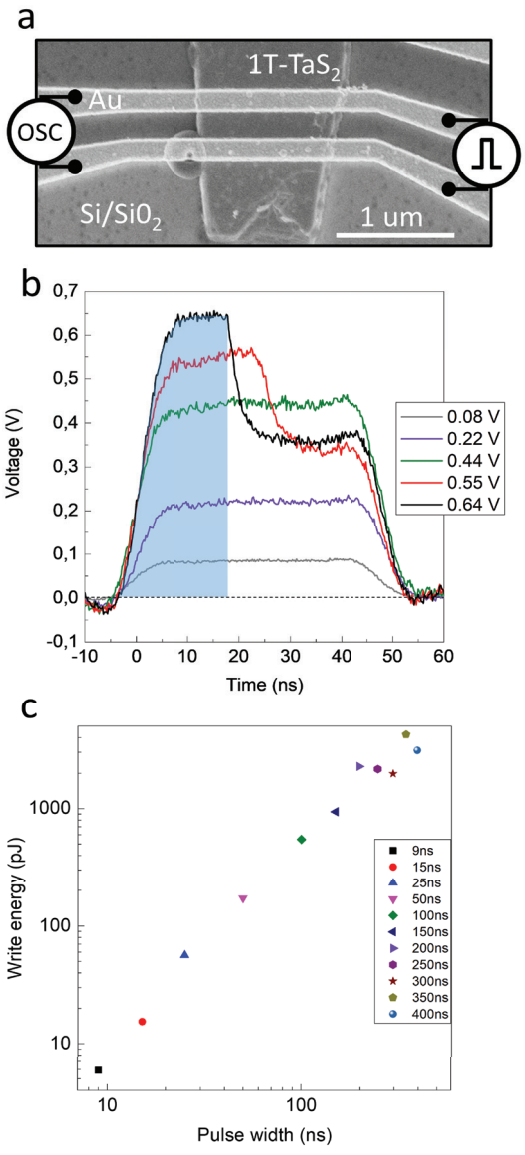

Figure 3: a) Schematic of the experiment with a pulse generator on one side of the CCM device and an osciloscope in parallel. b) Voltage across the CCM device observed during electrical pulsing. The drop in voltage occurs because the CCM device switches from HI to LO state. Shaded area was used in the W energy calculation. c) Scaling of the W energy as a function of applied pulse width.

The same kind of switching dynamics as in Fig. 3b was also observed using longer W pulses [16]. It was shown that the range of possible W pulse width is very wide, from 100 ms down to 16 ps [16], [17]. For ultrafast pulses the electrodes were fabricated in a transmission line configuration to ensure good transmission. W energy calculated with a 16 ps FWHM (rise time ~11 ps) pulse was E_W = 2.2 fJ/bit [17], where the W voltage was 1 V and entire pulse width was used in the equation.

One way to decrease the W energy is scaling of the CCM device. Scaling of dimensions directly affects the voltage needed to switch the state of the CCM device. If the dimensions of the device are smaller, there's physically less polarons or domain walls that are required to reconfigure, meaning less injected charge is needed plus the applied electric field is increased, assuming both are vital. W voltage scales linearly with the gap between the electrodes fabricated on devices on a range of 4 µm – 60 nm, with the smallest W voltage achieved being 0.3 V [17].

3.3 Erase process

When considering a non-volatile memory device, the information stored has to remain unchanged for a long period of time, ideally indefinitely. HI state of the CCM device is not problematic since it is the ground state. The LO state however is a metastable state which occurs under non-equilibrium conditions, but it can still be extremely long lasting under right conditions. The switching of the LO state back into the HI state is presumed to occur due to thermally activated domain reconfiguration, meaning the lower the ambient temperature, the more stable the LO state is, or in other terms, the longer the lifetime of the LO state τ_{LO} is. LO state is completely stable or non-volatile at temperatures below 20 K, so E process is induced by applying an E pulse, which can be on a time scale of µs-ms with an amplitude <0.5 V [16], [17]. E pulse effectively heats up the CCM element, which than switches back into to the HI state. The E process can be greatly optimized with proper thermal management by including an extra heating element as was demonstrated in phase change memory (PCM) devices, where high heating is crucial for operation [25]. It is also presumed that in a bigger

scale CCM device, E process would be done in blocks, meaning that slower E process would not pose such a disadvantage.

At temperatures above 20 K, the LO state slowly relaxes back into the HI state by itself with a certain relaxation rate ($r = 1/\tau_{LO}$) [22]. The relaxation dynamic was investigated by switching a CCM device from HI to LO state and observing the time evolution of the electrical resistance at a fixed temperature, which is shown in Fig. 4a (experiment - dotted line, exponential fit – dashed line). Speed of relaxation increases quickly with increasing temperature and becomes comparable to the measurement time at temperatures above 60 K. At 150 K the relaxation rate is a few µs, which can be observed on the oscilloscope by adjusting the period of W pulse train and observing the voltage across the CCM (similarly to Fig. 3b). This means that the CCM device can be written to the LO state at any temperature bellow the NC-C transition (~160–180 K), however the stability of the LO state is heavily influenced by the temperature. At 150 K it takes only a few µs for the LO state to completely relax back to the HI state after which the CCM device is ready to be written again. CCM device can thus also be used in the volatile regime (above 20 K), but have to be refreshed accordingly, much like dynamic random-access memory (DRAM).

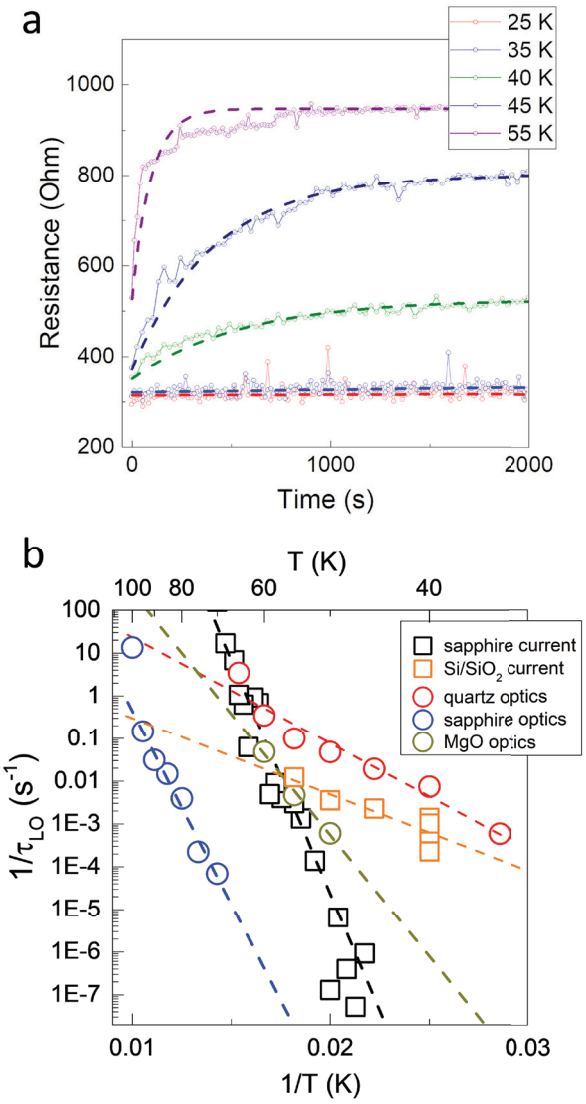

Figure 4: a) Plot of resistance versus time, showing relaxation of the LO state at different temperatures, from which the lifetimes are extracted. The relaxation time at 40 K is ~10 minutes, while at 55 K it's ~2 minutes. Dotted line is the experimental data, dashed line is the exponential fit. b) Arrhenius plot of relaxation rate for different substrates and different excitation methods (optical or electrical).

To obtain relaxation dynamics in Fig. 4a electrical pulses were used. When using laser pulses to write the CCM's state, the relaxation dynamic of the LO state looks similar, however the comparison of the relaxation rate *r* between the two cases shows quite a big difference. This can be seen when comparing the relaxation rate for optical (blue circles) and current (black squares) switching of a CCM device on a sapphire substrate in an Arrhenius plot in Fig. 4b. The *r* of the optical switching is much lower than the *r* of the current switching at a certain temperature. This is most likely attributed to extra heating provided by the current pulse used for switching, which is 5 µs long, compared to a 35 fs laser pulse. This means that the effective temperature is higher in the current switching compared to the optical switching.

Choice of sample substrate also affects the relaxation rate due to different expansion coefficients and consequential strain on the 1T-TaS_2 sample [22] (Fig. 4b). The tested substrates were sapphire, MgO, quartz and Si/SiO_2 with the imposed tensile strain $\Delta\varepsilon$ being 0.19 %, 0.13 % for sapphire and MgO respectively and 0.03 % for quartz and Si/SiO_2 at 50 K. Even though $\Delta\varepsilon$ is quite small, the effect seems to be rather large when comparing the relaxation rate for the case of sapphire and quartz. When the lattice expands because of the tensile strain of the substrate, the CDW has to rearrange to maintain commensurability and that can lead to extra domain walls being introduced. And since the relaxation from the H to the C state involves annihilation of domain walls, a higher tensile strain leads to higher activation energies E_A and consequentially to a lower relaxation rate. Extracting the activation energy E_A from fitting an Arrhenius law $1/\tau_H = e^{-E_A/k_BT}$ in Fig. 4b, the values are between E_A = 280–2300 K, where the highest activation energy belongs to the substrate with the highest $\Delta\varepsilon$ (sapphire). But it appears that the E_A also varies between different samples, implying that some other parameters such as nanofabricated electrodes, local defects and impurities

affect the stability of the H state. By using a proper substrate, one could manipulate and tune the stability of the H state while ensuring a fast E process in an ultrafast non-volatile memory device.

Different substrate strains may have an effect on the way multiple layers of 1T-TaS_2 crystal stack inside a CCM device. It is not yet clear how or to what extent the stacking of layers affects the switching dynamics. The measurements done on a device in a vertical/crossbar (out-of-plane) configuration show qualitatively similar behaviour to a more typical planar (in-plane) device [26]. There is a big discrepancy in the resistivity and the switching threshold for electric field between the two cases, where the vertical device has ~1000 times higher resistivity and ~100 times higher electric field threshold. However, the threshold electrical current is almost the same for both configurations as well as the relaxation rate of the LO state with the extracted activation energy $E_A = 650 \pm 100$ K [26] that matches with previous values for planar devices [22]. This points to the fact that switching between different electronic configurations inside the 1T-TaS_2 crystal combines the effect of in-plane polaronic order reconfiguration as well as re-stacking between individual layers. In the case of typical planar devices [16], [17], [22] (Fig. 2a, 3b) the current is probably not being confined only to the top layer anyway, especially since the electrodes are fabricated over the edge of the crystal and make contact on the side as well. Therefore, both the in-plane and out-of-plane physics contribute to the electrical behaviour of the devices.

Still, the CCM devices in crossbar configuration are very promising for larger scale integration since they allow for bigger density than the planar version. They are also easier to be scaled to lower dimensions, because the gap between the electrodes is determined only by the thickness of the 1T-TaS_2 flake and is therefore not limited by the complicated lithographic procedure. However, very thin flakes (< 10 nm) do not necessarily exhibit the NC CDW – C CDW transition, which means they don't develop the insulating behaviour at low temperatures (Fig. 1a, black curve) and cannot be used as a memory device. Instead their resistance follows a straight line into a so called supercooled NC CDW state as they are cooled down [27]. This problem can be mitigated by ensuring a very slow cooling rate [27] or with capping of the device to prevent oxidation, which could be responsible for pining of the CDW [28] and consequential suppression of the NC-C transition.

4 Conclusions and Outlook

In summary, CCM devices show ultrafast (16 ps FWHM) [17], energy efficient operation (2.2 fJ/bit) [17], non-volatility at cryogenic temperatures [22] and very good endurance (>10^6 cycles) [17], which is very important for electronic applications. The basic memory operation is provided through electronic switching between two distinct resistance states (HI and LO), but intermediate states are also available, potentially allowing one CCM element to be used as a multibit device [16], [26]. The overall structure of the device is also very simple, and it can be fabricated in a planar or vertical configuration to allow for easier integration into bigger systems. Erase process is currently the limiting factor when it comes to speed and energy consumption of the device, however with proper thermal management it can be improved significantly as demonstrated in PCM devices [25]. Role of heating in the switching operation is also not yet understood completely.

Among conventional CMOS memory technologies the most widely spread are the SRAM and DRAM technologies with write times on the nanosecond timescale and write energies from 100 fJ/bit to 1 pj/bit respectively [29]. They have very good endurance and very high level of integration, however their memory operation is still volatile, which makes them inherently more dissipative and less economical. Among non-volatile memory devices, the most popular are the solid state drives (SSD), which usually rely on NAND Flash technology for memory operation, but at this point they are not fast nor durable enough to replace SRAM or DRAM yet [30]. CCM devices are able to achieve faster write times (16 ps) and more energy efficient operation (2.2 fJ/bit)[17] compared to the SRAM or DRAM devices, while also having the advantage of non-volatility. However, CCM devices are currently still in the prototype stage and the level of integration and device density is still much lower compared to conventional CMOS devices.

There are many alternative non-volatile memory technologies besides the CCM, such as Magnetoelectric RAM (MeRAM), Spin-Transfer Torque RAM (STT-RAM) and Phase Change Memory (PCM) devices, among which the lowest energy per bit is reported in electric-field-controlled switching in magnetic tunnel junctions (MeRAM) with $E_W = 30 – 40$ fj/bit [31], followed closely by the spin-tranfer torque switching in CoFeB free layers (STT-RAM) with $E_W = 44$ fJ/bit [32]. PCM devices have higher switching energies (>2.5 pJ) and also slower operational speed (~500 ps) [25], because they rely on relatively slow ionic recrystallization of their active material. Thus, compared to others, CCM seems to be well under way for such a young technology.

Since CCM devices operate extremely well at cryogenic temperatures, they are very attractive to be used in cryocomputer systems such as superconducting Rapid Single-Flux-Quantum (RSFQ) [33], [34] systems and

quantum processors, which are lacking an ultrafast and energy-efficient cryogenic memory device [35]. Integration of CCM into RSFQ logic is possible using a superconducting element called a nanocryotron (nTron) [36] that is sensitive enough to be triggered by extremely small SFQ pulses (~2 mVps) yet can still produce up to 8 V of output voltage in only ~100 ps [36], [37], which is more than sufficient to drive a CCM device. Integrating SRAM or DRAM into superconducting circuits was also reported, but in order to drive CMOS logic, multiple Josephson junction stacks and amplification stages have to be used, which increases power dissipation and can negatively affect cryocomputer's operation [38], [39]. By replacing the typical voltage amplifiers in such hybrid Josephson-CMOS circuits with nTron drivers, the power consumption can be reduced by an order of magnitude [40], however the non-volatility of the memory is still not realized with this approach, while on the other hand it could be solved using CCM devices. Superconducting computer systems are considered as the solution to the power consumption problem current computers are facing and CCM devices could present a boost in their development.

5 Methods

5.1 Synthesis of 1T-TaS_2

Chemical vapour transport (CVT) method [41] is mostly used to grow high quality bulk 1T-TaS_2 and other TMD crystals. This is done in an evacuated and sealed quartz ampule which is inserted into a furnace with a temperature gradient from T_2~850 K to T_1~750 K (Fig 5a) [41]. For 1T-TaS_2, a mixture of solid sulphur, tantalum and iodine is inserted into the ampule. Iodine serves as a transport agent that forms complexes with the evaporated materials and transports them to the colder side of the ampule, where the crystal grows. The ampule is quenched after the growth in order to freeze the 1T polytype of TaS_2 which otherwise isn't stable at room temperature. The result of CVT growth are millimetre big high-quality crystals (Fig. 5b) which have to be mechanically exfoliated in order to acquire thin films used in CCM devices. After that, laser or electron beam (e-beam) lithography is performed to fabricate metallic contacts.

A more scalable and integrable approach to growing TaS_2 for device applications is by the Molecular Beam Epitaxy (MBE) method, which is schematically presented in Fig. 5c [42]. MBE method is used for epitaxial thin-film deposition and is widely used in the fabrication process of semiconductor devices. In the case of 1T-TaS_2, Ta and S source is needed in an ultrahigh vacuum chamber. The LSAT substrate is preheated to ~1000 K to ensure the growth of 1T polytype and the thickness is monitored *in situ*. After the growth of the

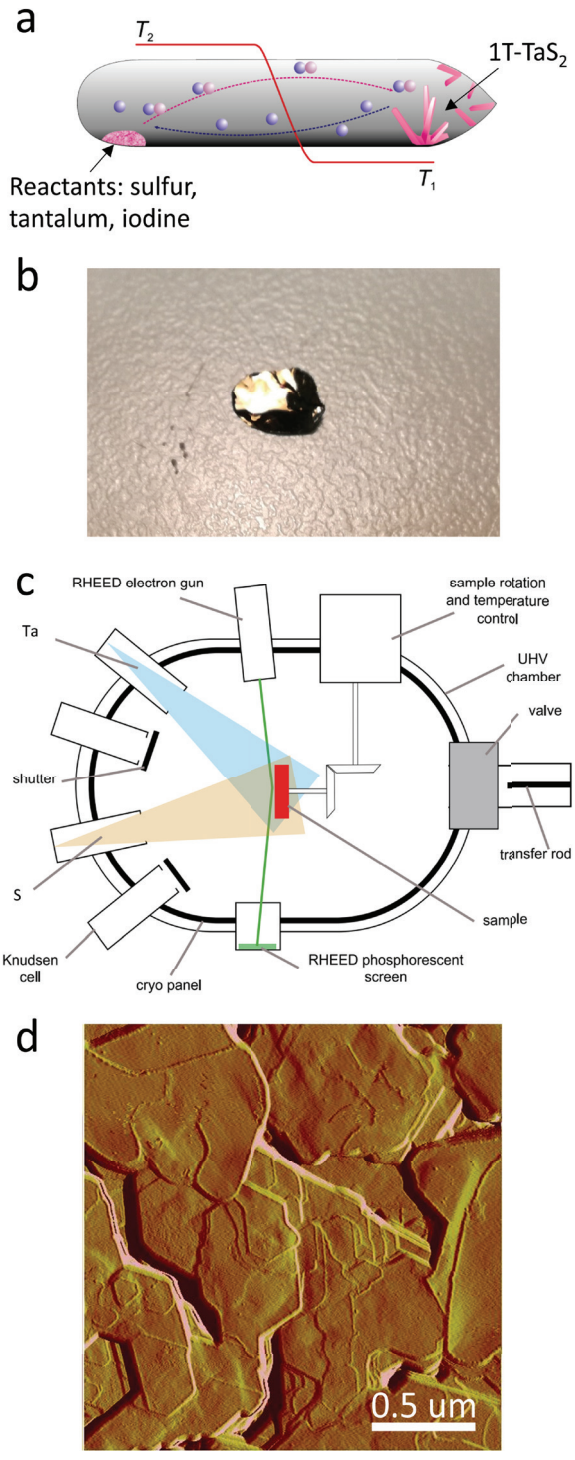

Figure 5: Growth of TaS_2. a) Chemical vapour transport (CVT) reaction in an ampule. Adopted from ref.[41] b) Image of a milimetre big TaS_2 crystal grown by CVT. c) Molecular beam epitaxy reaction in a vacuum chamber. Adopted from ref.[42] d) Atomic force microscope image of TaS_2 surface, grown in an MBE machine.

sample is complete, the sample is quenched to freeze the 1T polytype.

Result of the growth is a thin 1T-TaS_2 film (10–30 nm) fairly uniform over the entire substrate. Atomic force microscope (AFM) image of the MBE grown film is shown in Fig. 5d. To produce CCM devices, the MBE grown films would have to be patterned accordingly using etching and metal contacts would have to be fabricated using laser or e-beam lithography.

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7 Conflicts of interest.

The authors declare no conflict of interest.

8 References

1. H. Radamson *et al.*, 'The Challenges of Advanced CMOS Process from 2D to 3D', *Applied Sciences*, vol. 7, no. 10, p. 1047, Oct. 2017, https://doi.org/10.3390/app7101047.
2. N. Z. Haron and S. Hamdioui, 'Why is CMOS scaling coming to an END?', in *2008 3rd International Design and Test Workshop*, Monastir, Tunisia, Dec. 2008, pp. 98–103. https://doi.org/10.1109/IDT.2008.4802475.
3. D. Akinwande *et al.*, 'Graphene and two-dimensional materials for silicon technology', *Nature* 573, 507–518 (2019) https://doi.org/10.1038/s41586-019-1573-9
4. M. A. Zidan, J. P. Strachan, and W. D. Lu, 'The future of electronics based on memristive systems', *Nature Electronics*, vol. 1, no. 1, Art. no. 1, Jan. 2018, https://doi.org/10.1038/s41928-017-0006-8.
5. H. Choi, D. Hong, J. Lee, and S. Yoo, 'Reducing DRAM refresh power consumption by runtime profiling of retention time and dual-row activation', *Microprocessors and Microsystems*, vol. 72, p. 102942, Feb. 2020, https://doi.org/10.1016/j.micpro.2019.102942.
6. T. Tripathi, D. Chauhan, and S. Singh, 'A Novel Approach to Design SRAM Cells for Low Leakage and Improved Stability', *JLPEA*, vol. 8, no. 4, p. 41, Oct. 2018, https://doi.org/10.3390/jlpea8040041.
7. V. Sverdlov, J. Weinbub, and S. Selberherr, "Spintronics as a Non-Volatile Complement to Modern Microelectronics," *Inf. MIDEM*, vol. 47, no. 4, pp. 195–210, 2017.
8. L. Stojchevska *et al.*, 'Ultrafast Switching to a Stable Hidden Quantum State in an Electronic Crystal', *Science*, vol. 344, no. 6180, Art. no. 6180, Apr. 2014, https://doi.org/10.1126/science.1241591.
9. S. Manzeli, D. Ovchinnikov, D. Pasquier, O. V. Yazyev, and A. Kis, '2D transition metal dichalcogenides', *Nat Rev Mater*, vol. 2, no. 8, p. 17033, Aug. 2017, https://doi.org/10.1038/natrevmats.2017.33.
10. J. Ravnik *et al.*, 'A time-domain phase diagram of metastable states in a charge ordered quantum material', *Nat Commun*, vol. 12, no. 1, p. 2323, Dec. 2021, https://doi.org/10.1038/s41467-021-22646-7.
11. B. Sipos, A. F. Kusmartseva, A. Akrap, H. Berger, L. Forró, and E. Tutiš, 'From Mott state to superconductivity in 1T-TaS2', *Nature Mater*, vol. 7, no. 12, pp. 960–965, Dec. 2008, https://doi.org/10.1038/nmat2318.
12. E. Tosatti and P. Fazekas, 'ON THE NATURE OF THE LOW-TEMPERATURE PHASE OF 1T-TaS_2', *J. Phys. Colloques*, vol. 37, no. C4, pp. C4-165-C4-168, Oct. 1976, https://doi.org/10.1051/jphyscol:1976426.
13. K. Rossnagel, 'On the origin of charge-density waves in select layered transition-metal dichalcogenides', *J. Phys.: Condens. Matter*, vol. 23, no. 21, p. 213001, Jun. 2011, https://doi.org/10.1088/0953-8984/23/21/213001.
14. R. E. Thomson, B. Burk, A. Zettl, and J. Clarke, 'Scanning tunneling microscopy of the charge-density-wave structure in 1 *T* - TaS 2', *Phys. Rev. B*, vol. 49, no. 24, pp. 16899–16916, Jun. 1994, https://doi.org/10.1103/PhysRevB.49.16899.
15. B. Burk, R. E. Thomson, J. Clarke, and A. Zettl, 'Surface and Bulk Charge Density Wave Structure in 1 T-TaS2', *Science*, vol. 257, no. 5068, pp. 362–364, Jul. 1992, https://doi.org/10.1126/science.257.5068.362.
16. I. Vaskivskyi *et al.*, 'Fast electronic resistance switching involving hidden charge density wave states', *Nat Commun*, vol. 7, no. 1, p. 11442, Sep. 2016, https://doi.org/10.1038/ncomms11442.

17. A. Mraz *et al.*, 'Energy efficient manipulation of topologically protected states in non-volatile ultrafast charge configuration memory devices', arXiv:2103.04622
18. Y. A. Gerasimenko, P. Karpov, I. Vaskivskyi, S. Brazovskii, and D. Mihailovic, 'Intertwined chiral charge orders and topological stabilization of the light-induced state of a prototypical transition metal dichalcogenide', *npj Quantum Mater.*, vol. 4, no. 1, p. 32, Dec. 2019, https://doi.org/10.1038/s41535-019-0172-1.
19. D. Cho *et al.*, 'Nanoscale manipulation of the Mott insulating state coupled to charge order in 1T-TaS2', *Nat Commun*, vol. 7, no. 1, p. 10453, Apr. 2016, https://doi.org/10.1038/ncomms10453.
20. M. W. Shihong, T. Prodromakis, I. Salaoru, and C. Toumazou, 'Modelling of Current Percolation Channels in Emerging Resistive Switching Elements', arXiv:1206.2746.
21. J. Ravnik, I. Vaskivskyi, T. Mertelj, and D. Mihailovic, 'Real-time observation of the coherent transition to a metastable emergent state in 1 T – Ta S 2', *Phys. Rev. B*, vol. 97, no. 7, Art. no. 7, Feb. 2018, https://doi.org/10.1103/PhysRevB.97.075304.
22. I. Vaskivskyi *et al.*, 'Controlling the metal-to-insulator relaxation of the metastable hidden quantum state in 1T-TaS_2', *Science Advances*, vol. 1, no. 6, Art. no. 6, Jul. 2015, https://doi.org/10.1126/sciadv.1500168.
23. P. Monceau, 'Electronic crystals: an experimental overview', *Advances in Physics*, vol. 61, no. 4, pp. 325–581, Aug. 2012, https://doi.org/10.1080/00018732.2012.719674.
24. J. Bardeen, 'Classical versus quantum models of charge-density-wave depinning in quasi-one-dimensional metals', *Phys. Rev. B*, vol. 39, no. 6, pp. 3528–3532, Feb. 1989, https://doi.org/10.1103/PhysRevB.39.3528.
25. D. Loke *et al.*, 'Breaking the Speed Limits of Phase-Change Memory', *Science*, vol. 336, no. 6088, Art. no. 6088, Jun. 2012, https://doi.org/10.1126/science.1221561.
26. D. Svetin, I. Vaskivskyi, S. Brazovskii, and D. Mihailovic, 'Three-dimensional resistivity and switching between correlated electronic states in 1T-TaS2', *Scientific Reports*, vol. 7, no. 1, Art. no. 1, Dec. 2017, https://doi.org/10.1038/srep46048.
27. M. Yoshida, R. Suzuki, Y. Zhang, M. Nakano, and Y. Iwasa, 'Memristive phase switching in two-dimensional 1T-TaS_2 crystals', *Sci. Adv.*, vol. 1, no. 9, Art. no. 9, Oct. 2015, https://doi.org/10.1126/sciadv.1500606.
28. A. W. Tsen *et al.*, 'Structure and control of charge density waves in two-dimensional 1T-TaS_2', *Proc Natl Acad Sci USA*, vol. 112, no. 49, pp. 15054–15059, Dec. 2015, https://doi.org/10.1073/pnas.1512092112.
29. K. L. Wang, J. G. Alzate, and P. Khalili Amiri, 'Low-power non-volatile spintronic memory: STT-RAM and beyond', *J. Phys. D: Appl. Phys.*, vol. 46, no. 7, Art. no. 7, Feb. 2013, https://doi.org/10.1088/0022-3727/46/7/074003.
30. R. Micheloni, 'Solid-State Drive (SSD): A Nonvolatile Storage System', *Proc. IEEE*, vol. 105, no. 4, pp. 583–588, Apr. 2017, https://doi.org/10.1109/JPROC.2017.2678018.
31. P. Khalili Amiri *et al.*, 'Electric-Field-Controlled Magnetoelectric RAM: Progress, Challenges, and Scaling', *IEEE Transactions on Magnetics*, vol. 51, no. 11, Art. no. 11, Nov. 2015, https://doi.org/10.1109/TMAG.2015.2443124.
32. J. M. Iwata-Harms *et al.*, 'Ultrathin perpendicular magnetic anisotropy CoFeB free layers for highly efficient, high speed writing in spin-transfer-torque magnetic random access memory', *Sci Rep*, vol. 9, no. 1, p. 19407, Dec. 2019, https://doi.org/10.1038/s41598-019-54466-7.
33. O. A. Mukhanov, 'Energy-Efficient Single Flux Quantum Technology', *IEEE Trans. Appl. Supercond.*, vol. 21, no. 3, pp. 760–769, Jun. 2011, https://doi.org/10.1109/TASC.2010.2096792.
34. K. K. Likharev and V. K. Semenov, 'RSFQ logic/memory family: a new Josephson-junction technology for sub-terahertz-clock-frequency digital systems', *IEEE Trans. Appl. Supercond.*, vol. 1, no. 1, pp. 3–28, Mar. 1991, https://doi.org/10.1109/77.80745.
35. D. S. Holmes, A. L. Ripple, and M. A. Manheimer, 'Energy-Efficient Superconducting Computing—Power Budgets and Requirements', *IEEE Trans. Appl. Supercond.*, vol. 23, no. 3, pp. 1701610–1701610, Jun. 2013, https://doi.org/10.1109/TASC.2013.2244634.
36. A. N. McCaughan and K. K. Berggren, 'A Superconducting-Nanowire Three-Terminal Electrothermal Device', *Nano Letters*, vol. 14, no. 10, Art. no. 10, Oct. 2014, https://doi.org/10.1021/nl502629x.
37 Q.-Y. Zhao, A. N. McCaughan, A. E. Dane, K. K. Berggren, and T. Ortlepp, 'A nanocryotron comparator can connect single-flux-quantum circuits to conventional electronics', *Superconductor Science and Technology*, vol. 30, no. 4, Art. no. 4, Apr. 2017, https://doi.org/10.1088/1361-6668/aa5f33.
38. G. Konno, Y. Yamanashi, and N. Yoshikawa, 'Fully Functional Operation of Low-Power 64-kb Josephson-CMOS Hybrid Memories', *IEEE Trans. Appl. Supercond.*, vol. 27, no. 4, pp. 1–7, Jun. 2017, https://doi.org/10.1109/TASC.2016.2646911.

39. T. Van Duzer *et al.*, '64-kb Hybrid Josephson-CMOS 4 Kelvin RAM With 400 ps Access Time and 12 mW Read Power', *IEEE Trans. Appl. Supercond.*, vol. 23, no. 3, pp. 1700504–1700504, Jun. 2013, https://doi.org/10.1109/TASC.2012.2230294.
40. M. Tanaka, M. Suzuki, G. Konno, Y. Ito, A. Fujimaki, and N. Yoshikawa, 'Josephson-CMOS Hybrid Memory With Nanocryotrons', *IEEE Trans. Appl. Supercond.*, vol. 27, no. 4, pp. 1–4, Jun. 2017, https://doi.org/10.1109/TASC.2016.2646929.
41. P. Schmidt, M. Binnewies, R. Glaum, and M. Schmidt, 'Chemical Vapor Transport Reactions–Methods, Materials, Modeling', in *Advanced Topics on Crystal Growth*, S. Ferreira, Ed. InTech, 2013. https://doi.org/10.5772/55547.
42. S. Tardif, 'Nanocolonnes de GeMn : propriétés magnétiques et structurales à la lumière du synchrotron', https://tel.archives-ouvertes.fr/tel-00585130/.

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