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Quantum-based serial-parallel multiplier circuit using an efficient nano-scale serial adder

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Abstract: Quantum dot cellular automata (QCA) is one of the newest nanotechnologies. The conventional complementary metal oxide semiconductor (CMOS) technology was superbly replaced by QCA technology. This method uses logic states to identify the positions of individual electrons rather than defining voltage levels. A wide range of optimization factors, including reduced power consumption, quick transitions, and an extraordinarily dense structure, are covered by QCA technology. On the other hand, the serial-parallel multiplier (SPM) circuit is an important circuit by itself, and it is also very important in the design of larger circuits. This paper defines an optimized circuit of SPM circuit using QCA. It can integrate serial and parallel processing benefits altogether to increase efficiency and decrease computation time. Thus, all these mentioned advantages make this multiplier framework a crucial element in numerous applications, including complex arithmetic computations and signal processing. This research presents a new QCA-based SPM circuit to optimize the multiplier circuit's performance and enhance the overall design. The proposed framework is an amalgamation of highly performance architecture with efficient path planning. Other than that, the proposed QCA-based SPM circuit is based on the majority gate and 1-bit serial adder (BSA). BCA circuit has 34 cells and a 0.04 μm2 area and uses 0.5 clock cycles. The outcomes showed the suggested QCA-based SPM circuit occupies a mere 0.28 μm² area, requires 222 QCA cells, and demonstrates a latency of 1.25 clock cycles. This work contributes to the existing literature on QCA technology, also emphasizing its capabilities in advancing VLSI circuit layout via optimized performance.

Keywords: Multiplier, Serial–Parallel, Binary multiplier operation, Nano, QCA-based communications

Kvantno vezje zaporedno-paralelnega množilnika z uporabo učinkovitega zaporednega seštevalnika v nano merilu

Izvleček: Kvantni točkovni celični avtomati (QCA) so ena od najnovejših nanotehnologij. Tradicionalno tehnologijo komplementarnih kovinsko oksidnih polprevodnikov (CMOS) je odlično nadomestila tehnologija QCA. Ta metoda uporablja logična stanja za določanje položajev posameznih elektronov in ne definira napetostnih nivojev. Tehnologija QCA pokriva številne optimizacijske dejavnike, vključno z manjšo porabo energije, hitrimi prehodi in izredno gosto strukturo. Po drugi strani pa je vezje serijsko-paralelnega množilnika (SPM) samo po sebi pomembno vezje, zelo pomembno pa je tudi pri načrtovanju večjih vezij. Članek opredeljuje optimizirano vezje SPM z uporabo QCA. V njem lahko združimo prednosti serijske in vzporedne obdelave ter tako povečamo učinkovitost in skrajšamo čas računanja. Zaradi vseh omenjenih prednosti je torej to seštevalno ogrodje ključni element v številnih aplikacijah, vključno s kompleksnimi aritmetičnimi izračuni in obdelavo signalov. V tej raziskavi je predstavljeno novo vezje SPM, ki temelji na QCA, za optimizacijo učinkovitosti vezja množitelja in izboljšanje celotne zasnove. Predlagani okvir je združitev visoko zmogljive arhitekture z učinkovitim načrtovanjem poti. Predlagano vezje SPM, ki temelji na QCA, temelji na večinskih vratih in 1-bitnem zaporednem seštevalniku (BSA). Vezje BCA ima 34 celic in površino 0,04 μm2 ter porabi 0,5 takta. Rezultati so pokazali, da predlagano vezje SPM, ki temelji na QCA, zavzema le 0,28 μm² površine, potrebuje 222 celic QCA in izkazuje zakasnitev 1,25 takta. To delo prispeva k obstoječi literaturi o tehnologiji QCA, pri čemer poudarja tudi njene zmožnosti pri napredku postavitve vezij VLSI prek optimizirane zmogljivosti.

Ključne besede: množilnik, serijsko-vzporendo, binaren množilnik, nano, komunikacije na osnovi QCA

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1 Introduction

Enduring empirical observation in semiconductor technology, exemplified by Moore's Law, outlines the contemporary challenges faced by Very Large-Scale Integration (*VLSI*). To address these troubling issues, a shift from conventional VLSI computing to molecular, DNA, and quantum computing as some viable alternative options might be helpful. The Quantum-dot Cellular Automata (*QCA*) is one of these intriguing realization technologies that has garnered greater attention recently (9–13) because of several advantageous qualities. These challenges prompted the solution introduced by *Lent* in *1997* involving QCA [1]. Moore's Law, established in *1965*, signifies the regular doubling of transistors per square inch on integrated circuits and microchips, underpinning the remarkable growth and cost-effectiveness of transistor-based semiconductor technologies such as Complementary Metal-Oxide-Semiconductor (*CMOS*) and *VLSI*.
There are examples of actualized quantum circuits that can function at room temperature and are built with semiconductor, magnetic, and molecular technologies. One particularly helpful aspect of QCA technology is that it uses electron interactions—rather than electron flow—to accomplish computation, making it an ultra-low-power implementation method. In comparison to CMOS, it also offers better device density and quicker switching speed. QCA technology is expected to operate in the terahertz frequency domain and attain a density of 10^{12} devices per cm^2. Because CMOS transistors have constraints in terms of power, area, and performance, QCA technology should be viewed as a promising alternative for implementing complex systems. This is because of all these qualitative qualities [2, 3].

The potential of QCA technology to transform computer usage is generating a lot of excitement. To put it simply, QCA circuits process information by using the power of attraction between electrons, the smallest particles. On the other hand, the Serial–Parallel Multiplier (*SPM*) is a unique circuit that may be used to solve a wide range of arithmetic problems. Moreover, the *SPM* takes advantage of QCA technology, which can do many things at once. This helps QCA manage big multiplication tasks really well. A *SPM* is an important part of QCA technology because it makes it possible to multiply binary numbers in a smart way using the special abilities of QCA cells. Multipliers, especially *SPM* circuits, are important and essential circuits in QCA technology due to their high speed and accuracy. Based on the issues mentioned, this paper introduces a unique SPM circuit based on QCA. In fact, the primary goal of the presented paper is to design a fast SPM circuit with fast computing capabilities. In fact, this circuit, with its inherent capability of QCA-based computing, tries to increase the speed, accuracy, and efficiency of the circuits implemented in this technology.

The remaining part of this paper is divided as follows: section 2 is the preliminaries of QCA and related works. Section 3 presents the proposed *1-bit* serial adder (*BSA*) and SPM circuit designs in detail. The simulation and evaluation of the circuits are illustrated in Section 4. Lastly, section 5 concludes the findings of the study and explains the direction of future research.

2 Background

A pair of electrons can be carried across any set of diagonal dots in a QCA cell consisting of four quantum dots. The electrons break into separate points because of the strong potential barrier that exists among every pair of quantum dots. However, the arrangement can be made simpler by using cells with four points; an extra quantum dot can be placed in the cell's center. Because of their high energy, electrons are known to push things. Consequently, the opposite electron is moved to the matching diagonal quantum dot by transferring over the tunneling barrier when one electron moves in the neighboring cells. By going over the tunneling barrier and onto its associated diagonal quantum dot, the other electron is moved to the surrounding cells. The binary numbers *0 and 1* can be assumed to correspond to the two conceivable instances discussed above. [4]. An array of QCA cells makes up the binary wire, which is the fundamental logic component of QCA. Transmitting binary data requires a linear arrangement of the cells. Also, the electrostatic repulsion causes information to flow from input to output. In addition, a diagonal QCA wire is a regular cell that has been rotated. Once it has been rotated, it can likewise be utilized to create a wire [5].

The fundamental components of a QCA are the majority gate, inverter, and QCA wire. The binary value is transferred through Coulombic interactions among cells from input to output. The wire created by cascading cells could be composed of cells orientated at *45 degrees* rather than *90 degrees*, or it could be arranged in a horizontal row. Furthermore, for QCA cells to properly convey binary signals, they do not need to be in an upright position. Also, the cells that are *90 degrees* oriented can be positioned close to cells that are off-centered. This implementation explains the integrated quantum behavior of QCA technology in information processing. QCA is considered a suitable alternative to traditional semiconductor devices [6].

The XOR gate is a fundamental unit in the logical element in QCA for bit-wise manipulation. Usually, it com-

prises a low output (*0*) if both inputs are low or both are high. On the other hand, if one, and only one, of the inputs to the gate is high, the output will be true (*1*). Employing coulombic interactions, the *XOR* logic functions are executed by the QCA XOR gate. Thus, it is of substantial importance in computational systems based on QCA [7].

The QCA-based clocking synchronization system is an important component of nano-scale technology. It determines the efficiency of all computational functions run by the QCA cells. The changes that occur in a clock control system during the clock phase are depicted in four distinct phases. The four phases of the clock—*Switch, Hold, Release, and Relax*—can be changed following how electrons are activated. Hold encodes values *0 and 1*, referring to the condition in which the barrier associated with the dot has been increased, inhibiting electron tunneling. The switch involves progressively increasing the barrier corresponding to a dot in an inactivated cell. The release is the state in which the dot barrier is progressively dropped, and Relax is the state in which the barrier decreases, and electron tunneling is made simpler [8].

The fundamental mathematical operations encompass addition, subtraction, division, and multiplication. Out of these, multiplication holds a distinct significance within the context of circuits and digital computing [9]. Multiplication operations find widespread applications in various computational tasks, making them particularly vital. Within processors, multipliers stand as integral components of the arithmetic unit, and their efficiency and speed profoundly impact overall processor performance [10]. The capacity to carry out effective multiplication operations dictates the complexity and speed of processors, so optimizing multipliers is essential to improving the capabilities and efficiency of contemporary processors and digital systems. The standard integer multiplication procedure and binary multiplication are quite similar. The first step is to multiply each binary number's digit by the digit of another binary number. Then, finally, total them all to obtain the outcome. The result is a binary number representing the product of the multiplicand and multiplier. Binary multipliers are integral in digital systems, particularly in microprocessors and digital signal processing, where they perform essential tasks such as integer and fixed-point multiplication, making them a fundamental component of binary arithmetic [11].

2.1 Related works

In this section, the previous designs presented for the SPM circuit have been reviewed.

Edrisi Arani and Rezai [12] proposed the design of aserial–parallel multiplier in quantum-dot cellular automata technology. A new serial-parallel QCA multiplier circuit based on an effective full-adder circuit design was presented and evaluated in this paper. The QCA full-adder circuit was constructed using *31* cells that had an area of *0.03 μm²* and a delay of *0.5 clock cycles*. It also featured a majority gate and a three-input XOR gate. The *4 × 4* QCA SPM was designed by *264* QCA cells that use *0.75 clock cycle latency* and a *0.27 μm²* of area. In this article, QCADesigner *2.0.3* was used to implement the circuits and test them, and the results showed the accuracy of the circuits.

Bahar and Wahid [9] presented and investigated an *SPM* circuit along with energy analysis. The authors have used a new XOR and a majority gate to design a *BSA* circuit. The presented XOR gate has used the Coulombic repulsion property of QCA technology. This gate was used in designing circuits of *4-, 8-, 16-, 32-, and 64-bit* multipliers. The circuits that were presented were designed and tested by QCADesigner and QCAPro simulators, and the results, according to the researchers, reduced the space consumption and the number of cells compared to previous designs. It is worth mentioning that the QCAPro simulator has been used to determine the energy dissipation of the implemented circuit.

Ahmadpour, et al. [13] presented the design of a multiplier for use in nano-scale *IoT* systems using atomic silicon. In fact, this article examined an *ASiQD-based* multiplier circuit for efficient power management in micro-IoT devices. The *4 × 4-bit multiplier* array was designed with the *SiQAD* simulation tool technology to reduce space consumption and energy consumption. This circuit and design have significantly reduced energy consumption and space consumption in IoT devices compared to most existing designs.

Also, Premananda, et al. [14] proposed a *4-bit SPM* based on QCA. Compared to multipliers that use more complex multiplication methods, *SPMs* have a simple and scalable architecture. The present paper has proposed a *4-bit SPM* circuit based on QCA, which was optimal in energy and area. Using the *4* multipliers, a *4-bit SPM* was designed and *QCADesigner-E* was used to design, analyze, and simulate proposed circuits. This tool used the number of cells, area, and energy that have been used to evaluate the designed circuits. The simulation results showed that compared to the reference architectures, the proposed 4-bit SPM minimizes the number of cells, area, and energy dissipation.

Finally, Sekar, et al. [15] proposed a high-speed SPM in QCA. In addition, in this paper, 4-bit SPM, shift registers, and adders were implemented based on QCA cells.

Shift registers were added to the circuit for parallel and serial computations, to store inputs and outputs, and to improve circuit output stability. The implementation of SPM with shift registers to store input and output in QCA was presented for the first time in this article. Compared to current designs, the proposed multiplier without a shift register was at least *66%* faster and more efficient. The *4-bit* shift register multiplier had had *2271* cells with a *7.74 μm²* size and a *25.25 clock cycle* latency.

3 Proposed design

An SPM is a digital circuit used to multiply two binary numbers. It combines both serial and parallel processing techniques to perform multiplication efficiently. This type of multiplier is essential in the context of QCA technology, which is an emerging nano-scale computing technology with potential applications in future high-performance and energy-efficient computing systems. In mode a serial-parallel processing is as follows:

Serial Processing: In a serial-parallel multiplier, the multiplication process begins with serial processing, where the bits of one of the operands (*usually the multiplier*) are processed one by one. The other operand (*the multiplicand*) remains fixed during this phase.

Parallel Processing: After serial processing, the multiplier is processed in parallel, meaning multiple bit-wise multiplications occur simultaneously. These parallel multiplication results are then added together to obtain the final product.

Given that, QCA is a novel computing paradigm that utilizes quantum phenomena at the nano-scale level to perform logic and computation. In QCA, information is represented and processed using the quantum properties of electron charge and Coulombic interactions between quantum dots. Unlike conventional *CMOS* technology, QCA exhibits potential as a technology that holds significant promise for realizing digital logic at the nano-scale. It is a kind of nanotechnology designed specifically for developing computational circuits. Also, some of its attributes, such as less occupied area and lower latency, render it a suitable alternative when compared to the nano-scale *CMOS* technology. The repulsion between QCA cells and how to communicate between them are fundamental challenges in the design of nanomultipliers for QCA technology. Older multipliers designed using CMOS technology cannot be used for QCA technology because they use Coulombic repulsion. It should be noted that SPMs are particularly important in QCA technology because they can exploit the inherent parallelism of QCA cells while the input data are serial and perform calculations.

In addition, the SPM circuit significantly performs complex binary multiplication operations, and this important feature makes this circuit a major element in nanocomputing. Thus, all these advantages make this multiplier framework a crucial element in numerous applications, including complex arithmetic computations and signal processing. Also, QCA-based systems often require scalability to handle larger data sizes and more complex computations. *SPM* can be designed with scalability, making them suitable for various QCA-based computing needs.

To implement the proposed *SPM* circuit presented in this article, we applied a *BSA*, which includes an *XOR* gate and a majority gate. We have made changes to connect one of its inputs to the carry output, as shown in Figure 1, and this connection goes through a *0.5-clock cycle*. This circuit has *34 cells* and a *0.04 μm²* area.

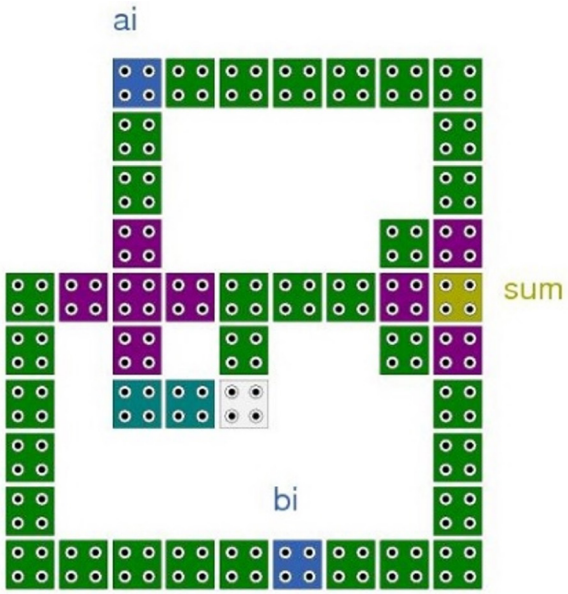

Figure 1: The proposed BSA.

In the pursuit of performance improvements, particularly in terms of reducing circuit area and minimizing cell count, an efficient architecture is utilized, incorporating one-layer crossovers as the selected design strategy. It's essential to note that in scenarios where minimizing signal delay is critical, the integration of one-layer crossovers proves effective for optimizing circuit efficiency. A high-speed BSA serves as the foundational component for creating a high-speed SPM circuit. Notably, the traditional BSA architecture has been enhanced, specifically involving the establishment of feedback connections that link the carry input and out-

put. This innovative design enables the carry output of the BSA to serve as an input for the same BSA, a feature instrumental in designing the QCA SPM circuit. A visual representation of the developed QCA SPM circuit can be found in Figure 2, while Figure 3 provides a detailed layout illustration of this circuit.

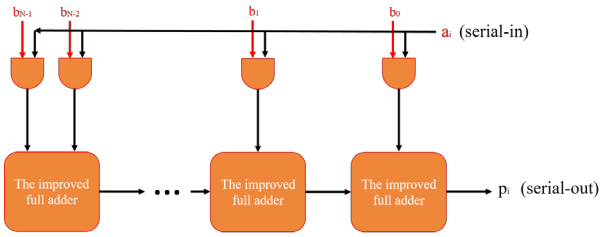

Figure 2: Block diagram of the developed SPM circuit

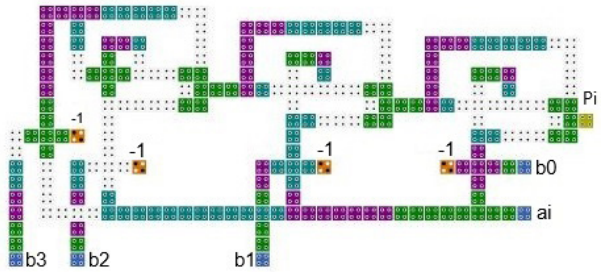

Figure 3: QCA design of the developed SPM circuit

Figure 3 shows the QCA-based design of the developed SPM circuit. It is demonstrated that this circuit is implemented in one layer, and the majority gates and *BSAs* are located in the main layer. In the provided circuit, access to inputs and outputs is very easy to use. With *1.25 clock cycles* and a *0.28 μm²* area, the proposed QCA *SPM* circuit comprises *222* cells.

4 Simulation tools and results

Utilizing QCA technology, *QCADesigner 2.0.3* is an all-inclusive and adaptable software application employed for the simulation and fabrication of digital circuits. This academic application is meticulously customized to address the particular demands and complexities of QCA-based circuit layouts, presenting scientists and developers with indispensable resources for investigating the futuristic possibilities of this emergent nanoelectronics paradigm. The QCA circuits are designed and simulated using the *QCADesinger* tool *version 2.0.3* using the *bistable approximation* default simulation engine. The area and clock analysis are carried out using the QCADesigner [16-18].

Figure 4 shows the simulation and test outcomes of the proposed *1-bit BSA* circuit in QCA, and these results confirm the correctness of the proposed circuit. In addition, a pair of inputs and the output is reached after *0.5 clock cycles*. Figure 5 also shows the simulation and test outcomes, and these results confirm the proposed *SPM* circuit is working well. In addition, a pair of inputs and the output is reached after *1.25 clock cycles*. All the output results are consistent with the results of the correctness table (Table 1), indicating the presented circuit's accuracy.

On the other hand, Table 2 summarizes the simulation results of the developed QCA *BSA* and SPM circuits compared to other QCA circuits. According to the comparison results, it is quite visible that the presented circuits have fewer consumption cells and less consumption space than the previous designs due to their one-layers.

Table 1: The truth table of the proposed *BSA*

ai	bi	Majority gate output	Sum
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	1
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	1

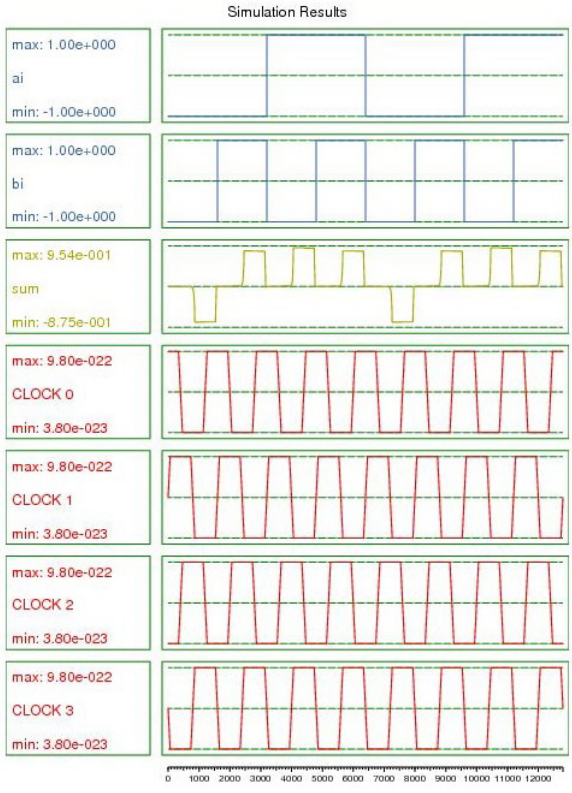

Figure 4: The proposed BSA circuit simulation results

Table 2: Comparisons of multiplier circuits

Designs	Area (μm²)	Cells	Latency
Cho and Swartzlander [19]	0.493	406	1
Zhang, et al. [20]	0.299	329	1
Zhang, et al. [20]	0.319	330	1.25
Edrisi Arani and Rezai [12]	0.27	264	1.75
Bahar and Wahid [9]	0.243	229	1.25
Proposed BSA design	0.04	34	0.5
Proposed SPM design	0.28	222	1.25

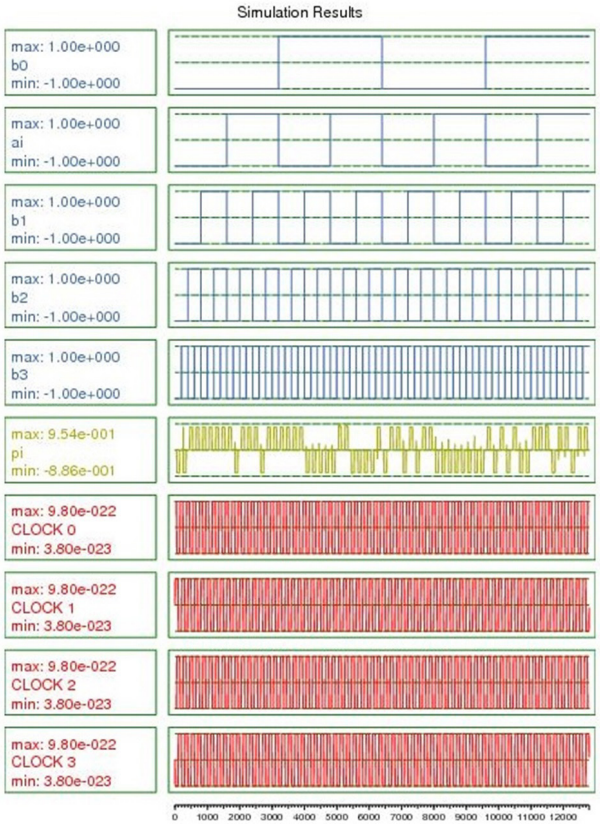

Figure 5: The proposed SPM circuit simulation results**.**

5 Conclusion and future works

The unique features of QCA, such as their low occupancy and ultralow power consumption, make them particularly attractive candidates for nano-scale technology. Also, BSA and SPM are widely used as building elements in arithmetic circuits. An essential part of digital computing is an SPM because it can efficiently perform complex binary multiplication operations. An efficient BSA gate and SPM circuit in QCA computational circuits can significantly improve efficiency. Therefore, this paper proposes one approach for designing the SPM circuit utilizing a BSA gate. The suggested SPM circuit was validated and simulated. We demonstrated the suggested SPM circuit's functioning. In addition, the number of cells, delay, and space consumption of the suggested SPM circuit are obtained using QCAdesigner. This SPM circuit is designed with *222* quantum cells. The outcomes show the suggested QCA-based SPM circuit occupies a mere *0.28 μm²* area. This circuit has *1.25 clock cycles* to create output. Based on the number of cells, occupied area, and latency, the findings showed that the suggested designs work as intended. The suggested SPM appears to offer a workable substitute for the current architecture and is scalable. This circuit may be utilized in larger circuits since it generates *n-bit* QCA SPM using the suggested QCA SPM.

6 Conflict of interest

The authors declare no conflict of interest.

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