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CMOS Low-Power, Fully-Programmable Gaussian/Trapezoidal Fuzzy Membership Function Generator

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Abstract: Design of a novel flexible structure for fuzzy Membership Function Generator (MFG) has been discussed in this article. The main advantage of the proposed circuits is the capability for the production of all Trapezoidal, Gaussian, S and Z shapes, simultaneously. This objective has been achieved at the first step by means of two interconnected differential pairs which generate Gaussian, S and Z shapes. Thereafter, with the help of an improved Min/Max circuit, the Trapezoidal shape with sharp edges has been constructed. The circuits are designed in a way to produce all shapes with the feature of full programmability for slope, core, and height. These features, along with small active area and low power consumption, qualify this work to be repeatedly used in Fuzzy Logic Controllers (FLCs). Post-layout simulation results for TSMC 0.18µm CMOS technology confirm the correct behavior of the designed circuits. Based on the results, the power consumption of the whole structure is 54µW from a 1.8V power supply.

Keywords: Fuzzy membership function; Fuzzy logic controller; Fuzzifier; Min/Max circuits

CMOS nizkoenergijski programabilni gausov/ trapezoidni fuzzy funkcijski generator

Izvleček: V tem članku je obravnavana zasnova nove prilagodljive strukture za fuzzy funkcijski generator (MFG). Glavna prednost predlaganih vezij je možnost hkratne izdelave vseh trapeznih, Gaussovih, S in Z oblik. Cilj je bil v prvi fazi dosežen z dvema povezanima diferencialnima paroma, ki ustvarjata Gaussovo, S in Z obliko. Nato je bila s pomočjo izboljšanega vezja Min/Max izdelana trapezoidna oblika z ostrimi robovi. Vezja so zasnovana tako, da omogočajo izdelavo vseh oblik z možnostjo popolnega programiranja naklona, jedra in višine. Te lastnosti, skupaj z majhno aktivno površino in majhno porabo energije, omogočajo, da se to delo uporabi v fuzzy logičnih krmilnikih (FLC). Rezultati simulacije po izdelavi za tehnologijo TSMC 0,18 µm CMOS potrjujejo pravilno obnašanje zasnovanih vezij. Na podlagi rezultatov je poraba energije celotne strukture 54 µW pri napajalni napetosti 1,8V.

Ključne besede: Fuzzy funkcija; Krmilnik Fuzzy logike; Min/Max tokokrogi

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1 Introduction

Analog nature of the environment around us necessitates the operation of human-made signal processing systems in the analog domain. The main reason for this purpose lies behind the fact that analog systems can capture the natural signals more suitably than their digital counterparts. Also, the digital circuits mostly need extra blocks for the digitization of those obtained signals. Hence, the analog systems are economically efficient due to their lower power consumption [1]. Moreover, based on the information obtained from the

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literature, hardware realization for most of the fuzzy systems and neural networks has been done in the analog domain.

On the other hand, there has been intense competition between fuzzy systems and neural networks over recent years for the emulation of human brain behavior. Started by McCulloch and Pitts in 1943 for the realization of the first neuron model [2, 3], the historical background of neural systems seems to be older than Fuzzy Logic Controllers (FLCs). But since the practical realization of fuzzy logic systems at the end of the 1970s, in less than half a century, they have justified their capabilities for industrial use. Their applications cover a wide range of commercial consumer products such as cameras, rice-cookers, washing machines, and so forth [4].

The critical fact behind the population of fuzzy systems comes from the human brain translation ability for incorrect and imperfect sensory information which comes from perceptive organs [5]. It is because that the fuzzy set theory prepares a systematic computation which deals with such details linguistically. Moreover, it carries out the numerical calculations through linguistic labels arranged by membership functions [6]. Although Lukasiewicz and Tarski perused fuzzy logic as multi-valued logic in the 1920s [7], it was Lotfi A. Zadeh who announced his fuzzy set theory in 1965. It was the starting point for fuzzy systems [8].

In contrast to the standard binary sets where the variables usually pick up true or false values, in fuzzy sets, they can obtain a truth value revolving in the interval of 0 and 1 [9]. Meanwhile, for the case of utilizing linguistic variables, the degrees can be modeled by specific functions [10]. By considering these points, the general concept of an FLC will be brought up using the structure of Figure 1. As it is evident, each fuzzy system is composed of three main stages:

1) Fuzzification (membership function generation)
2) Fuzzy inference or fuzzy rule evaluation
3) Defuzzification

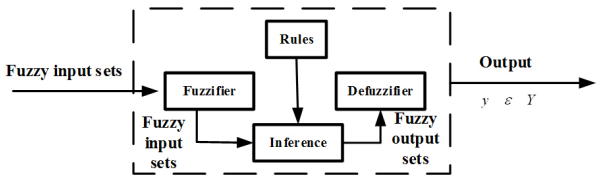


Figure 1: Structure of a Fuzzy Logic Model.

At the starting point, the fuzzification interface maps the inputs so that they can be interpreted and evaluated by the rules of the inference engine [11]. In hardware realization, the fuzzification is done by means of Membership Function Generator (MFG) circuits. The main objective of the fuzzification process is to transmute the analog input into a set of fuzzy variables. For higher accuracy, more fuzzy variables must be chosen where the outputs should be produced simultaneously [6, 12].

Because of their continuous nature and lower costs, analog Membership Function Circuits (MFCs) have drawn the attention of circuit designers over previous years. Many structures have been reported in the literature for hardware implementation of fuzzifiers in the analog domain. Depending on the purpose of the application, each structure contains different characteristics such as single or multi-variable outputs, specific waveforms, etc. In order to save power, most of the reported works can only generate one fuzzy variable at their outputs [13, 14, 15, 16, 17, 18]. The characteristic feature of these works is the function waveforms with smooth edges making them unsuitable for high-precision applications. One of the famous low-power exceptions has been introduced in [1], which has the capability of producing six fuzzy variables simultaneously. The drawback of such structure is the low resolution of the output waveforms as the drain-source voltages of the transistors are not equal in transients. Moreover, the circuit doesn't have the capability of programmability, which limits its usage in high-performance FLCs.

Piece-Wise Linear (PWL) membership functions are the waveforms with sharp edges which are used for special purpose applications. Despite higher precision, more power dissipation is expected for their generating circuits. Those circuits are designed mostly in current-mode because of the simplicity for current summation or subtraction at the connecting nodes [19, 20, 21, 22, 23]. The reported works in this criterion only produce the triangular or trapezoidal functions. The thorough analysis depicts that the problems concerning power and active area consumption have rarely been considered in most of these architectures.

One of the notable works has been presented in [21] in which by means of a simple mathematical idea an MFC has been designed using Min/Max operations. Since the circuit has been implemented in current-mode, it contains two advantages. Providing the Max and Min operations is the first privilege of this structure, while the flexibility to be configured as an MFG constitutes its second benefit. This idea can further be expanded to obtain multi-waveform membership functions.

As a conclusion, the main emphasis in this paper is to achieve the unique ability to generate all functional waveforms in a single scheme. Along with this, the programmability feature, along with low power and active area consumption, must be taken into account.

This work introduces a novel Min/Max architecture based MFG, which is implemented in current-mode using TSMC 0.18µm CMOS technology. Input voltages are used to control the slope, height, and location of waveforms. The main idea is based on the expansion of the scheme introduced in [21]. Figure 2 illustrates the initial concept, which is adapted to the differential pair based MFG so that all of the waveforms can be produced in one single architecture.

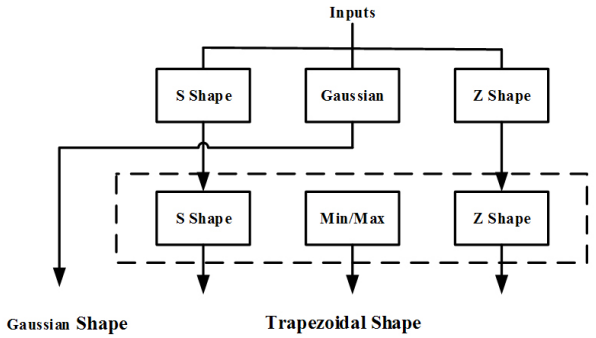


Figure 2: Structure of a Fuzzy Logic Model.

The designed circuit is composed of two parts. The first lock which is composed of a differential pair configuration generates the Gaussian, S and Z shapes simultaneously. Then, with the help of the optimized Min/Max circuit, which was initially reported in [24], the Trapezoidal/Triangular shapes with sharpened edges have been produced. It must be mentioned that the optimized Min/Max circuit can calculate the minimum of three input signals.

In Section 2, the main idea for the fuzzifier circuit is discussed, and the architecture has been demonstrated with a complete analysis. Section 3 is about the optimized Min/Max structure and its usage for customization of the output waveforms. Section 4 contains the simulation results and comparison of the designed work with previous ones. Finally, the conclusions have been summarized in Section 5.

2 Materials and methods

Fuzzification is well described by the procedure which generates a fuzzy value from an analog value of the real world. For this purpose, different classes of fuzzifiers can be employed [25]. The most important groups, utilized for the fuzzification process are:

1) Single-tone fuzzifiers
2) Gaussian fuzzifiers
3) Trapezoidal/Triangular fuzzifiers

It must be considered that the base set determines the class of representation for the membership function. For multi-valued or continuous fuzzy sets the *parametric representation* is usually suitable, and to do this, the modification of some parameters is often enough for the adjustment of the membership function. On the other hand, PWL membership functions are the most employed ones because of their computational efficiency. Trapezoidal and triangular functions constitute the central part of PWL waveforms and are distinguished by four and three parameters, respectively [5, 19, 23].

The normalized Gaussian function (which is the difference of two sigmoid waves), and the generalized bell function are also used for modeling of fuzzy sets in some special cases. In such functions, continuously differentiable curves with smooth transitions are needed where those features cannot be fulfilled by trapezoids [1, 16, 17, 26].

In General, for hardware realization of a fuzzy membership function, the following four features must be remarked [7]:

a) The *height*, as the highest membership value achieved by any element in the set.
b) The *support*, as the crisp set including all the elements of *X* with non-zero membership values.
c) The *core,* as the crisp set consisting of all the elements of *X* with the membership values of one.
d) The *boundary,* as the crisp set having all the elements of *X* with the membership values of $0 < \mu_A(x) < 1$.

The main emphasis in this work is to design a flexible architecture for achieving all of the mentioned waveforms simultaneously. Therefore, the initial idea comes from the generation of S, Z, and Gaussian functions in the first step. After that, with the help of an auxiliary circuit, the trapezoidal waves will be produced.

Therefore, the first part of the MFC will produce Gaussian, S, and Z shapes, where the initial idea has been illustrated in Figure 3. This circuit is composed of two differential pairs: the first pair consisting of M_1 and M_2 transistors, and the second pair in the right side which is constructed of M_3 and M_4 transistors. These pairs generate both S and Z shapes at their output loads.

The input voltage V_{in} is applied to M_1 and M_3 transistors at the same time. These transistors are initially in the cut-off region. Along with the increment of V_{in}, the gate-source voltages of M_1 and M_3 will grow, and they become ON. Therefore, they will produce S shape waveform at their drains while M_2 and M_4 transistors have the responsibility of generating Z shape.

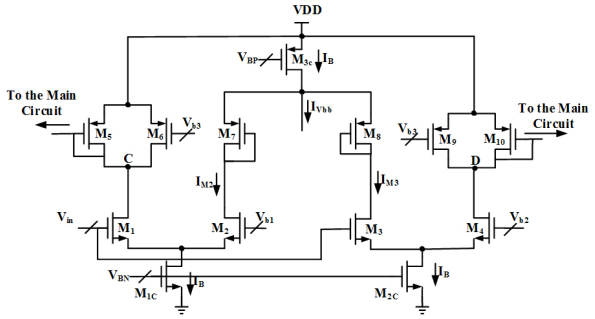


Figure 3: Initial idea for realization of the MFG.

To generate the Gaussian shape waveform, the currents of M_2 and M_3 are summed together, and the result will be subtracted from a normalized $10\mu A$ current. The current is specified as I_{Vbb} in Figure 3. These three currents will constitute three fuzzy variables.

Equations (1) and (2) illustrate the currents of M_2 and M_3, respectively [27]:

$$I_{M2} = \frac{1}{2}\left(I_B - V_1\sqrt{2kI_{ss} - k^2V_1^2} \right) \quad (1)$$

$$I_{M3} = \frac{1}{2}\left(I_B + V_2\sqrt{2kI_{ss} - k^2V_2^2} \right) \quad (2)$$

where $k = \frac{1}{2}\mu C_{ox}\frac{W}{L}$, $V_1 = V_{in} - V_{b1}$, and $V_2 = V_{in} - V_{b2}$. Moreover, I_B is the bias current which has a normalized value of $10\mu A$. Table 1 illustrates the values for I_{M2}, I_{M3}, and I_{Vbb} for different intervals of the input voltage. It is assumed that $V_{b1} < V_{b2}$.

The subtraction of V_{b1} from V_{b2} determines the width for the Gaussian shape. To explain the slope changes, let's consider the current of MOS transistor in the saturation region [27]:

$$I_d = \frac{1}{2}\mu C_{ox}\frac{W}{L}\left(V_{gs} - V_{th} \right)^2 \quad (3)$$

In (3), V_{gs} and V_{th} are the gate-source and the threshold voltage of the MOS transistor, respectively. μ and C_{0x} demonstrate the process coefficients, while W and L represent the dimensions of the MOS transistor. In order to change the slop, the sizes of M_1, M_2, M_3 and M_4 must be changed to achieve the desired values. It can be done by parallel transistors of differential pair inputs in Figure 3.

Table 1: Different values of three fuzzy variables.

	IM2	IVbb	IM3
$V_{in} < V_{b1} - \sqrt{2}\Delta V$	I_B	0	0
$V_{in} = V_{b1}$	$I_B/2$	$I_B/2$	0
$Vin = (V_{b1} + V_{b2})/2)$	0	I_B	0
$Vin = _{b2}$	0	$I_B/2$	$I_B/2$

M_6 and M_9 are current sources with constant values. Their role is to sharpen the lower part of the current for M_5 and M_{10}, which is illustrated in (4):

$$I_{M5,10} = \begin{cases} I_{M1,4} - I_{M6,9} & if \quad I_{M1,4} > I_{M6,9} \\ 0 & if \quad I_{M1,4} \le I_{M6,9} \end{cases} \quad (4)$$

The current waveforms of M_5 and M_{10} are S and Z shape, respectively which are expected to have sharpened edges. These currents will be transferred to the Min/Max circuit to produce the Trapezoidal/Triangular shape. Practically, the architecture of Figure 3 has two major problems:

1) The currents of M_2 and M_3 cannot be replicated easily as their loads are not directly connected to V_{dd}.
2) The currents of M_5 and *10* M_{10} transistors are not sharp enough to generate a Trapezoid waveform with sharp edges because of the poor linear operating range of differential pairs.

In order to solve these problems, the configuration of Figure 4 has been proposed and used as the final version of Gaussian, S, and Z shape MFG. M_{7a} and M_{8a} transistors are used to replicate currents of M_2 and M_3, respectively. For equalizing all of the currents, the bias current must be doubled for upside M_{3c} transistor. So I_{Vbb} will be doubled, too and it must be considered for current mirroring.

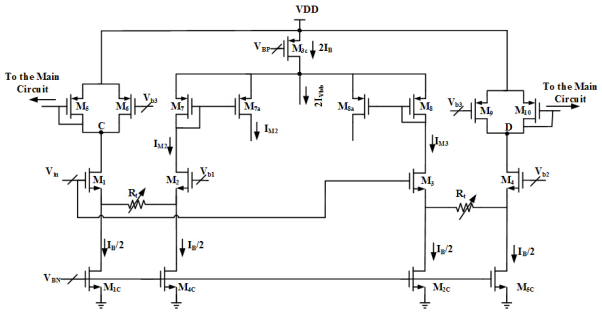


Figure 4: The proposed MFG.

The variable resistance R_t is used to increase the linearity range of differential pairs. It is implemented by means of a single transistor biased in the triode region. The current of the transistor in the triode region can be expressed as follows [27]:

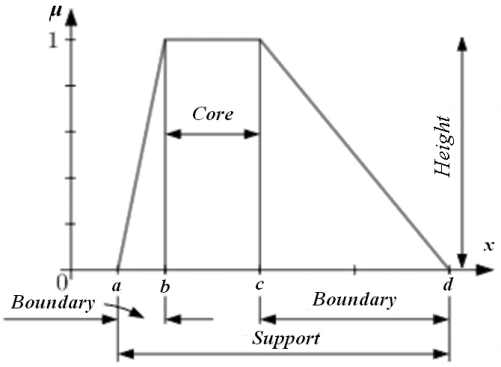
$$I_d = \mu C_{ox} \frac{W}{L}\left[\left(V_{gs} - V_{th}\right)V_{ds} - \frac{1}{2}{V_{ds}}^2\right] \quad (5)$$

V_{gs}, V_{th} and V_{ds} are the gate-source, threshold, and drain-source voltages of the MOS transistor, respectively. μ and C_{0x} represent the process coefficients while W and L denote the dimensions of the MOS transistor. If $V_{ds} \ll V_{gs} - V_{th}$, the resistance can be calculated as follows:

$$R = \frac{V_{ds}}{I_d} = \frac{L}{\mu C_{ox} W\left(V_{gs} - V_{th}\right)} \quad (6)$$

The resistance sharpens the edges of output currents I_{M5} and I_{M10}, which will be transferred to the Min/Max circuit.

(a)



(b)

$$\text{trapezoid}(x;a,b,c,d) = \begin{cases} 0 & x \le a \\ \frac{x-a}{b-a} & a \le x \le b \\ 1, & b \le x \le c \\ \frac{d-x}{d-c} & c \le x \le d \\ 0 & d \le x \end{cases}$$

Figure 5: Trapezoidal membership function (a) general waveform (b) mathematical expressions.

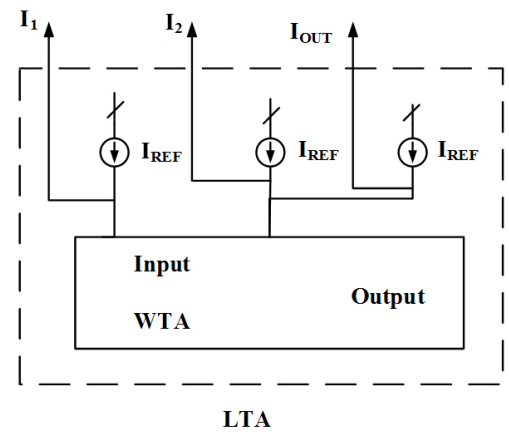
As mentioned before, the circuit of Figure 4 can only produce Gaussian, S, and Z shapes. By means of the current replicas (which perform the operations of summation and subtraction), the Trapezoid shape can be generated. However, the feature of full programmability along with good accuracy can be achieved using an additional circuit. Figure 5 demonstrates the general figure of a Trapezoidal membership function where in Figure 5(a), its four main characteristics are emphasized. Moreover, the mathematical expressions of this function are illustrated in Figure 5(b). For $b = c$, the trapezoidal shape will migrate to a triangular membership function.

In order to construct a programmable circuit, the height, core, boundary, and support must be adjustable. With a two input Min/Max circuit, at most only three of four features would be controlled. For achieving full programmability feature, a three-input Min/Max circuit is needed.

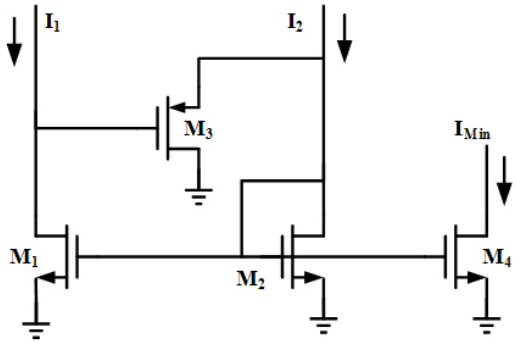
3 The optimized min/max circuit

In hardware design, the most popular fuzzy logic functions which implement logical 'AND' and 'OR' functions, are MIN and MAX operators, respectively. Therefore, they will play an essential role in the fuzzy inference engine implementation, and most of the reported works in the literature have put their basis on them.

(a)



(b)



(c)

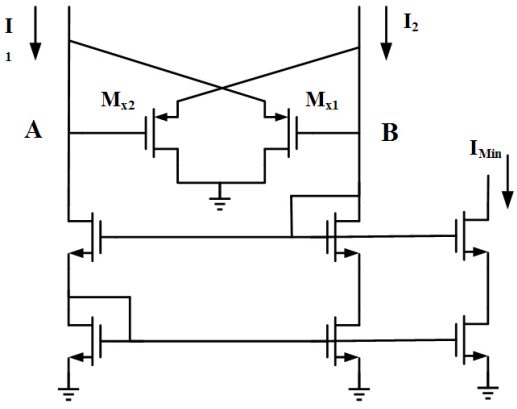


Figure 6: LTA network design by means of WTA network (a) general concept (b) Initial idea of Min circuit, (c) Structure of Min circuit proposed in [24].

One of the notable advantages of current-mode MIN and MAX circuits is that they do not necessarily need resistors in their architectures. On the other hand, the summation and subtraction of currents can simply be achieved just by wire connections. This leads to discriminating and straightforward configurations, which represent high speed and great functional density [24].

Because single fan-out is one of the drawbacks of current-mode based MIN/MAX circuits, then the current repeatability is considered as of prime importance for these structures. Also, the distribution of signals necessitates the utilization of multiple-output current mirrors. To design the MIN/MAX structure, current-mode is chosen because of the mentioned benefits, while the disadvantages are also taken into account.

After Lazzaro's work which was a novel report on Winner-Takes-All (WTA) structures (released in 1988) [28], a lot of WTA and closely related Loser-Takes-All (LTA) circuits have been proposed to realize Min/Max circuits [29, 30] (Figure 6). In some of the reported structures, the LTA function is obtained by means of WTA function. This fact is illustrated in Figure 6(a) whereby subtraction of the input values from a fixed reference current, the LTA function has been obtained. In order to explain the procedure, one can say that at the first step, one circuit performs the subtraction from a fixed current. Then, the maximum current selector behaves as the minimum current selector function. By considering the structure of Figure 6(b) as the initial idea, a newly designed structure has been reported in [24] (Figure 6(c)).

Wilson current mirror transistors are used to increase the output resistance. Also, the subtraction of currents at the input nodes enhances the accuracy of the output current.

According to Figure 6(c), If $I_1 > I_2$, then the voltage of node A rises to a high level while the voltage of node B drops down. Therefore, the gate-source voltage of M_{x1} will be increased, and this transistor will become on. On the other side, M_{x2} goes to cut off region. The extra current $I_1 - I_2$ passes through M_{x1} to the ground, which results in the reflected current in output as minimum current ($I_{min} = I_2$). The same reason holds for I_1 as the minimum current when $I_1 < I_2$.

The improved version in [31] has the extra feature of generating both maximum and minimum of input signals simultaneously. But the major problem associated with both of [24] and [31] is that they can only accept two signals as the inputs. As discussed in the previous section, for achieving the full control feature over four common characteristics of a Trapezoid waveform, at least the minimum of three input signals should be calculated. The optimized circuit with three inputs is shown in Figure 7.

The circuit is composed of two cascaded Min circuits of Figure 6(c). M_{11} and M_{12} are the input transistors. I_{M5} and I_{M10} are applied from the circuit of Figure 4 to M_{11} and M_{12}. In order to miniaturize the configuration and avoid more wiring, the second Min part is designed as the complement of the first part. The first part is the same as the circuit of Figure 6(c). At the second part, PMOS transistors are employed as the active loads (M_{19}, M_{20}, M_{21} and M_{22}). M_{25} and M_{26} are the input transistors of this part. M_{23} and M_{24} have the same role as their counterparts (M_{13} and M_{14}) in the first part of the Min circuit.

If $I_{M25} > I_{M26}$, then the gate voltage of M_{24} grows high and the gate voltage of M_{23} drops down. The extra current $I_{M25} - I_{M26}$ passes through M_{24} to V_{dd}. The result, which is the reflected current in output, gives the minimum current (I_{M26}).

The current of M_{25} can also represent the Trapezoidal/Triangular waveform. But it only controls *core*, *boundary*, and *support* of the membership function. Transistor M_{26}, which is the third input of Min circuit, is biased with a constant current to control the *height* of the Trapezoid function. Its maximum value which represents the fuzzy value of one is $10\mu A$.

The final waveform which has been obtained from cascode transistors (M_{27} and M_{28}) is the output of the fuzzifier to produce the Trapezoidal membership function. It must be mentioned that in the circuit of Figure 7 if the location of $M_{23} - M_{24}$ configuration is replaced with its counterpart $M_{13} - M_{14}$ pair, the three input Max circuit can also be obtained.

4 Simulations and comparison

4.1 Behavioral simulation

Post-Layout simulations are performed based on the TSMC 0.18µm standard process and 1.8V supply voltage by HSPICE to evaluate the correct behavior of designed fuzzifier architecture.

For the circuit of Figure 4, the simulation results of three fuzzy variables (I_{M2}, I_{Vbb}, and I_{M23}) constituting Z, Gaussian, and S shapes, respectively, are shown in Figure 8. The normalized $10\mu A$ current represents the fuzzy value of 1. For the overlapping areas, the summation of *heights* won't pass the normalized value.

To show programmability feature of the designed MFG, simulation results for different values of the sec-

ond bias voltage of differential pair V_{b2} (applied to the gate of M_4) are shown in Figure 9. The result indicates that the increment of V_{b2} stretches the *core* of Gaussian shape and turns it into Bell shape membership function, whilst the position of S shape will be relocated, too.

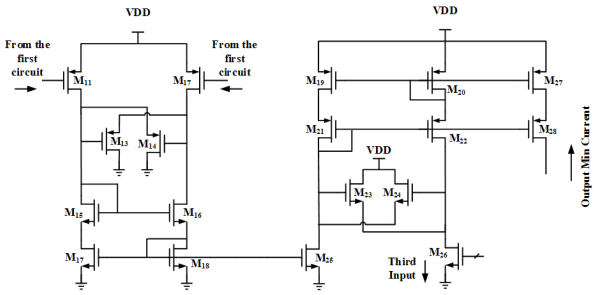


Figure 7: The optimized Min circuit.

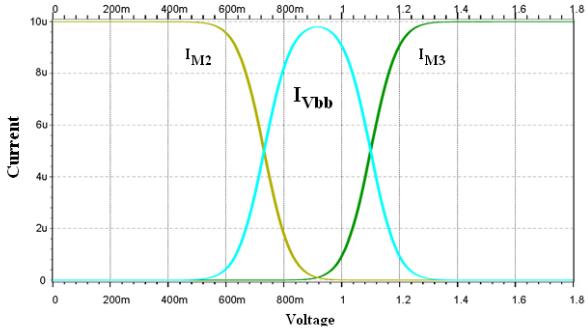


Figure 8: Simulation results for the architecture of Figure 4.

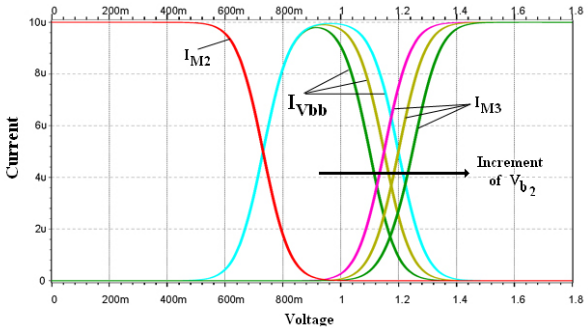


Figure 9: Core changes in the proposed MFG.

In order to investigate effect of input transistors dimensional variations on the slope changes of S, Z and Bell shapes, simulations have been done for three different values of $\frac{W}{L}$. The result which is illustrated in Figure 10 depicts that along with *core* and *support* changes, the *slope* can be regulated, too.

In order to adjust the height, the four bias currents ($\frac{I_B}{2}$) can be modified. As discussed in sections 2 and 3, I_{M5} and I_{M10} are the outputs of the first part, which constitute the inputs of Min circuit. Figure 11 shows the waveforms for these currents.

As illustrated in Figure 2, these waveforms are fed to the Min/Max circuit to produce the trapezoidal output with sharp edges.

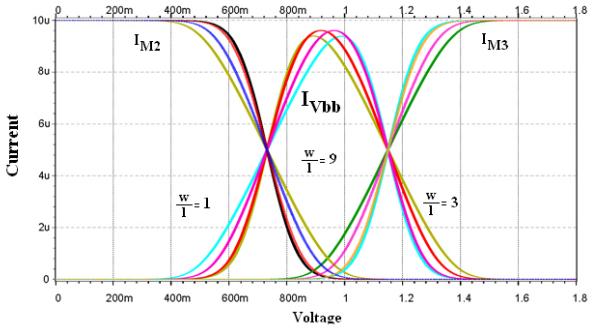


Figure 10: Slope changes of the proposed MFG for all three shapes.

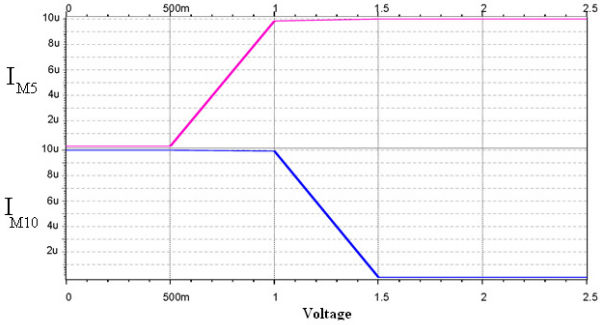
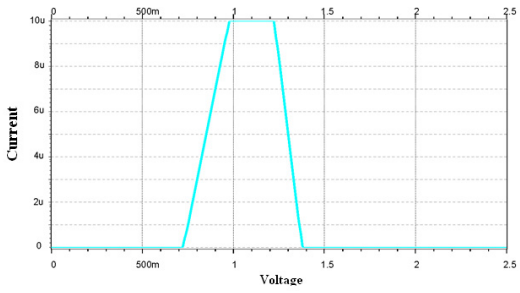


Figure 11: Waveforms of I_{M5} and I_{M10}.

(a)



(b)

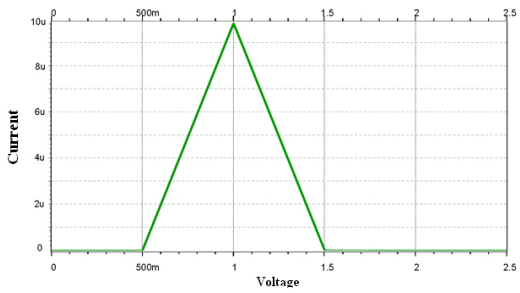


Figure 12: Simulation results for optimized Min Circuit (a) Trapezoidal shape (b) Triangular shape.

Also, Figure 12 shows the output of Min circuit, which produces the desired shapes. In Figure 12(a), the Trapezoidal waveform is illustrated, whilst by some modifications in bias voltages, the Triangular membership function can be achieved easily (Figure 12(b)).

In Figure 13, the programmability feature of Trapezoidal shape has been shown according to changes of V_{b1} and R_t. The increment of V_{b1} shifts the left side of the waveform to the higher voltages, while the changes of R_t adjusts the slope.

As the simulation results depict, full programmability of the designed structure (either for Gaussian and Trapezoid shapes) has been achieved successfully. This is a unique feature which is not reported in previous works.

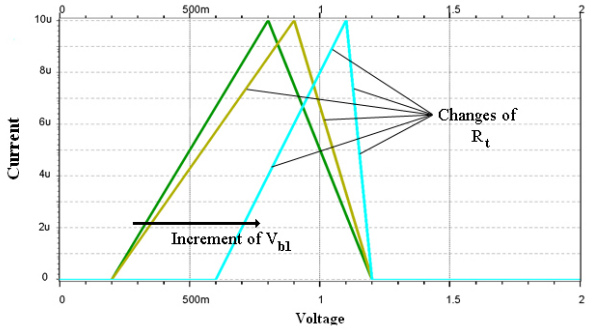


Figure 13: Simulation results for programmability of optimized Min Circuit considering Triangular shape.

The layout of the proposed work is illustrated in Figure 14, which consumes a small area of $500\mu m^2$ on-chip. In order to minimize the active area consumption, we have merged the transistors of membership function and Min/Max circuits together. Finally, Table 2 shows a comparison of this work with previous designs.

As the comparison results illustrate, the power consumption of the proposed architecture is less than the reported works. Moreover, the transistor count with the consideration of the fact the designed architecture produces all four classes of waveforms needed for fuzzy inference engine remains in a reasonable range.

It must be noted that only [1] and [15] have measurement results, and the other works have relied on simulation results. For the architecture of [18], the feature of full programmability has not been mentioned as the Trapezoidal shape has smooth edges for this work.

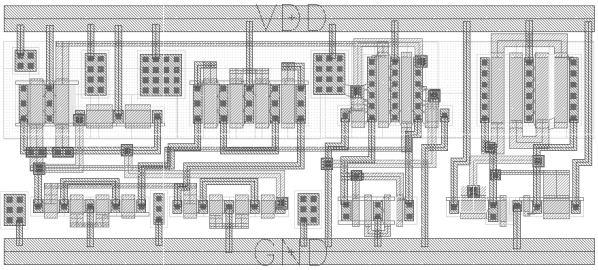


Figure 14: Layout of the proposed work.

4.2 Monte carlo simulation

At the final stage of the design performance evaluation, the Monte Carlo simulation results are provided to show the effect of process variations on the proposed structure. To achieve this, random values with Gaussian distribution were assigned to the device parameters

Table 2: Comparison of this work with previous designs.

Work	[1]	[15]	[16]	[17]	[18]	[21]	[22]	[23]	This Work
Technology (µm)	2	0.5	0.35	0.35	0.18	0.35	0.35	0.5	0.18
Supply (V)	10	3	3.3	3.3	1.8	3.3	3.3	1.5	1.8
S and Z Waves	√	×	√	×	√	×	×	×	√
Gaussian Wave	√	×	√	√	√	×	×	×	√
Trapezoid Wave	×	√	×	×	×	√	√	√	√
Slope Programmability	×	√	√	√	√	√	√	√	√
Height Programmability	×	√	√	√	√	√	√	√	√
Core Programmability	√	√	√	√	√	√	√	√	√
Transistor Count	17	28	43	23	16	48	24	61	33
Power (µW)	500	300	260	105	108	--	426	200	54
Input signal	Voltage	Voltage	Voltage	Voltage	V/I	Current	Current	Current	Voltage
Output Signal	Current	Current	Current	Current	Current	Current	Current	Current	Current
Implementation	Fab.	Fab.	Sim.	Sim.	Sim.	Sim.	Sim.	Sim.	Sim.

such as threshold voltage and size of transistors for each sample of Monte Carlo simulation.

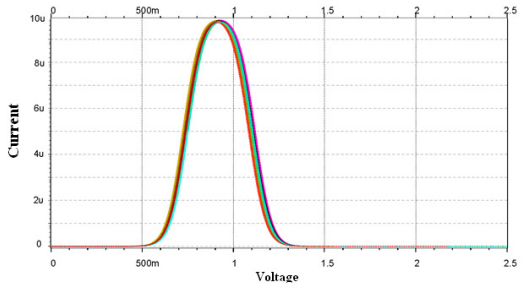
Then by running a complete simulation, a series of measurement results have been obtained. The designed circuit has been examined for 50 iterations, and the results for Gaussian and Triangular simulations are shown in Figure 15. In Figure 15(a) the results Gaussian waveform have been demonstrated while Figure 15 (b) illustrates the results for Trapezoidal shape. As the results indicate, the negative effect of process variations such as device mismatches and threshold voltage do not significantly affect the performance of the circuit.

Along with Monte Carlo analysis, the effect of temperature variations has also been considered on the current variations of the MOS transistors for performance evaluation of the designed circuits. As Figure 16 illustrates, temperature changes from 0 to 60°C do not cause any concern for the Gaussian waveform. It is because that in the configuration of Figure 4, the variable resistance behaves like a local feedback configuration and compensates the current changes related to temperature variations.

For the total power consumption of the designed architecture, one can say that the power dissipation can be calculated using the following relation:

$$P_{total} = V_{dd} \times \left(I_F + I_M \right) \tag{7}$$

(a)



(b)

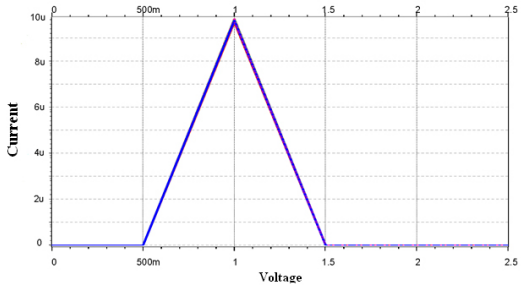


Figure 15: Monte Carlo simulation results (a) for Gaussian waveform (b) for Triangular shape.

in which I_F is the bias current-driven from M_{3c} transistor in Figure 4 and I_M is the summation of currents in

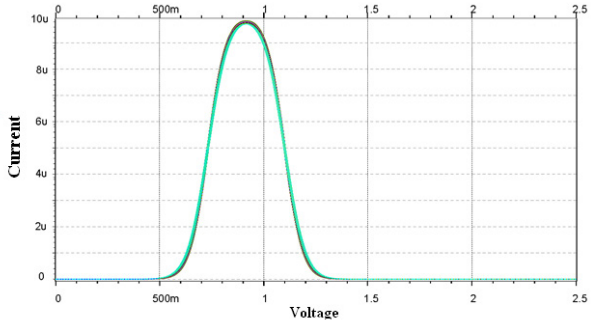


Figure 16: Temperature simulation results for Gaussian waveform.

the Min circuit of Figure 7 (driven from voltage source). Therefore, with the consideration of 1.8V as the supply voltage, $I_F = 10\mu A$, and $I_M = 20\mu A$ in the design process, the total power consumption will be equal to 54µW while the HSPICE simulation results have confirmed this value.

5 Conclusions

In this paper, a novel architecture for a fully programmable MFC is presented which produces Gaussian shape along with the Trapezoidal waveform. The improved Min/Max circuit enables us to obtain full programmability feature for Trapezoidal function, too. None of the previously published works could get both of the mentioned waveforms in a single scheme, and this is the main advantage of the designed architecture. Low power consumption and small active area are the other advantages of the designed architecture. These features, along with careful design considerations and reasonable transistor count, qualify the proposed work to be widely used in high-speed Fuzzy Logic Controllers.

Post-Layout simulation results confirm the correct behavior of the designed structure while the Monte Carlo and temperature simulation results demonstrate the low sensitivity feature of this work for process variations. The power consumption of the whole structure is 54µW from a 1.8V power supply using TSMC 0.18µm CMOS technology.

6 Conflict of Interest

The authors declare no conflict of interest. The authors also declare that there is no funding support for this work.

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