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Analysis and Mitigation of Negative Differential Resistance Effects with Hetero-gate Dielectric Layer in Negative-capacitance Field-effect Transistors

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Abstract: Negative-capacitance field-effect transistors (NCFETs) show promise as low-power devices for the next-generation. However, the negative differential resistance (NDR) effects are inherent in NCFET and adversely affect the design of integrated devices and circuits. In this study, a hetero-gate dielectric NCFET (HGD-NCFET) is proposed and investigated. The HGD-NCFET is formed by partially replacing the ferroelectric layer of NCFET with a high-dielectric constant (high-κ) material on the drain side to inhibit its NDR effects. The Sentaurus technology computer-aided design simulations demonstrate that the out conductance (G_{DS}), which is used to quantify the NDR effects, increases monotonically as a function of the length of high-κ material (L_{HK}), and G_{DS} eventually tends to zero in HGD-NCFET. In addition, the other electrical parameters of the HGD-NCFET remained almost unchanged compared to those of the original NCFET.

Keywords: negative differential resistance; negative-capacitance field-effect transistor; high-dielectric constant; hetero-gate dielectric

Analiza in ublažitev učinkov negativne diferencialne upornosti s hetero-vratno dielektrično plastjo v poljskih tranzistorjih z negativno kapacitivnostjo

Izvleček: Tranzistorji z negativno kapacitivnostjo (NCFET) so obetavni kot naprave z nizko porabo energije za naslednjo generacijo. Vendar so učinki negativne diferencialne upornosti (NDR) značilni za NCFET in negativno vplivajo na načrtovanje integriranih naprav in vezij. V tej študiji je predlagan in raziskan dielektrični hetero-vratni NCFET (HGD-NCFET). HGD-NCFET je oblikovan z delno zamenjavo feroelektrične plasti NCFET z materialom z visoko dielektrično konstanto (high-κ) na ponorni strani, da se zavirajo učinki NDR. Simulacije računalniško podprtega načrtovanja s tehnologijo Sentaurus kažejo, da se izhodna prevodnost (G_{DS}), ki se uporablja za količinsko opredelitev učinkov NDR, monotono povečuje v odvisnosti od dolžine materiala z visokim κ (L_{HK}), G_{DS} pa se v HGD-NCFET sčasoma približuje ničli. Poleg tega so ostali električni parametri HGD-NCFET skoraj nespremenjeni v primerjavi s prvotnim NCFET.

Ključne besede: negativna diferencialna upornost; poljski tranzistor z negativno kapacitivnostjo; visoka dielektrična konstanta; hetero-vratni dielektrik

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1 Introduction

Reducing the power consumption density has become one of the main research hotspots following the continuous miniaturization of silicon-based integrated circuits. However, the subthreshold swing (SS) of traditional metal-oxide-semiconductor field-effect transistors (MOSFETs) is difficult to break through 60 mV/decade at room temperature owing to basic thermodynamic limitations; thus, the scaling of the power supply voltage is limited [1,2]. Owing to the negative capacitance effects of the ferroelectric materials, negative-capacitance field-effect transistors (NCFETs) can amplify the internal gate voltage (V_{IN}). This successfully overcomes Boltzmann's SS limitation at 60 mV/decade, thus resulting in reduced power consumption [3–7]. Therefore, NCFETs are regarded as promising candidates for next-generation low-power devices due to their exceptional performance, including steep SS, high- switching current ratio (I_{ON}/I_{OFF}), and compatibility with standard the complementary metal-oxide-semiconductor (CMOS) manufacturing processes. Nevertheless, NCFETs exhibit negative differential resistance (NDR) effects at lower gate voltages.

The NDR effects in NCFET originate from the coupling of the drain voltage (V_{DS}) to V_{IN} via the gate–drain capacitance (C_{GD}), which results in current loss [8,9]. Although the NDR effects are advantageous in oscillator circuits [10,11], their presence may result hysteresis in the voltage transfer characteristics of logical gates, thus leading to larger noise margins [12,13]. This is due to the fact that the transfer characteristic curves of NMOS and PMOS intersect three times resulting in two steady states of the inverters at the same input voltage, with one value for each of the forward and reverse voltage sweeps, leading to hysteresis. Meanwhile, due to the unstable saturation current of the analogue amplifier[14], the application of NCFET to an analogue circuit may result in a change in the circuit's operating point. This alteration may lead to changes in the amplification characteristics, frequency response, and linear range of the circuit, resulting in non-linear distortion. This distortion may cause additional energy conversion between different components in the circuits, leading to increased power consumption. Therefore, suppression of the NDR effects is a necessary and urgent task. Several methods have been proposed to address this issue, such as the use of oxide-layer-trapped charge through electron injection [15], adjustment of the coupling capacitance between the gate and drain [16], and the use of local Gaussian heavy doping on the drain side [17]. However, these solutions require hot-carrier injection or complex manufacturing processes.

In this study, we propose an approach to suppress the NDR effects by partly replacing the ferroelectric layer of the traditional NCFET with a high-dielectric constant (high-κ) material (HfO_2) on the drain side. It is shown that with an increase in the HfO_2 length (L_{HK}), the electrostatic potential of the channel increased at low-gate voltages, and the NDR effects are obviously reduced.

2 Structure and modeling of hetero-gate dielectric NCFET (HGD-NCFET)

In this study, the NCFET used fully depleted silicon-on-insulator (FDSOI) technology. The process parameters for the device are listed in Table 1. The ferroelectric layer of the NCFET was replaced with a high-κ material (HfO_2) on the drain side, forming the HGD-NCFET. The structure of a typical HGD-NCFET device is shown in Fig. 1(a). Fig. 1(b) depicts the calibrated transfer characteristic curve (I_{DS}-V_{GS}) for the baseline FDSOI device with the experimental data at the 14 nm node [18]. The fabrication process flow of the HGD-NCFET is shown in Fig. 2. The manufacturing process for HGD-NCFET is essentially the same as that for conventional NCFET with few additional process step or cost. To demonstrate the physical characteristics of NCFET more accurately, the high-field saturation, Fermi, Shockley Read Hall model, Slotboom model of band gap narrowing, eQuantum Potential, doping dependence, and Landau-Khalatnikov model were included in the Sentautus technology computer-aided design (TCAD) simulations [19]. Although TCAD models aim to accurately represent physical processes, they are still based on approximations and simplifications. This can result in discrepancies between simulated and actual device behavior, particularly under extreme conditions or for new materials and structures. Ferroelectric materials have a non-centrosymmetric crystal structure in which spontaneous displacement of atoms leads to non-zero spontaneous polarisation. The relationship between electric field and polarisation (P) in ferroelectrics can be expressed as $E_{FE}=2\alpha P+4\beta P^3+6\gamma P^5+\rho(dP/dt)$, where α, β, and γ are parameters of the ferroelectric material. Then we can establish the correlation between the voltage V_{FE} at the ferroelectric terminals and the thickness of the attached point as $V_{FE}=T_{FE}\times(2\alpha P+4\beta P^3+6\gamma P^5+\rho(dP/dt))$. Then $Q=P+\varepsilon E\approx P$, and the ferroelectric capacitance (C_{FE}) can be expressed as follows [20]:

$$C_{FE}=\frac{dQ}{dV_{FE}}\approx\frac{1}{2\alpha\times T_{FE}}=\frac{2}{3\sqrt{3}}\times\frac{P_r}{E_C.T_{FE}} \quad (1)$$

where P_r and E_c are the remanent polarization and coercive fields of the ferroelectric materials, respectively. Since α is negative, the C_{FE} is negative.

Fig. 1(c) displays the equivalent capacitance circuit of the NCFET. Herein, C_{FE} and C_{MOS} represent the capacitances of the ferroelectric layer and the underlying FD-SOI, respectively. C_{MOS} is equivalent to the source capacitance (C_S), drain capacitance (C_D), oxide capacitance (C_{OX}), and hafnium dioxide capacitance (C_{HfO2}). Similar to the gate voltage, the drain voltage is coupled to the internal node through the gate-drain capacitance (C_{GD}). Equivalent circuits controlled by the gate and drain are shown in Fig. 1(d). The NDR effects in the NCFET are closely related to the capacitance matching between C_{FE} and C_{MOS}, as well as C_{GD}. The differential gain (A_V) and drain coupling factor (ξ_D) of the NCFET are given as follows [10]

$$A_V = \frac{dV_{IN}}{dV_{GS}} = \frac{C_{FE}}{C_{FE} + C_{GS} + C_{GD}} = \frac{C_{FE}}{C_{FE} + C_{MOS}} \tag{2}$$

$$\xi_D = \frac{dV_{IN}}{dV_{DS}} = \frac{C_{GD}}{C_{FE} + C_{GS} + C_{GD}} = \frac{C_{GD}}{C_{FE} + C_{MOS}} \tag{3}$$

To ensure the stable operation of NCFET without hysteresis, the absolute value of C_{FE} must be greater than C_{MOS}, that is, $C_{FE} + C_{MOS} < 0$ [21,22]. As NCFET stabilizes in the negative capacitance region ($C_{FE} < 0$), this results in $A_V \geq 1$ and $\xi_D < 0$.

Table 1: Structural parameter of the NCFET device.

Baseline structure	Value
Burrier oxide thickness (T_{BOX})	10 nm
Gate length (L_G)	12 nm
Insulator thickness (T_{OX})	Oxide/HfO2 0.5 /1.2 nm
Channel thickness (T_{CH})	5 nm
Source/Drain doping	2×10^{20} cm^{-3}
Channel doping	1×10^{15} cm^{-3}
Coercive field (E_C)	1×10^6 V/cm
Remanent polarization (P_r)	5×10^{-6} C/cm^2

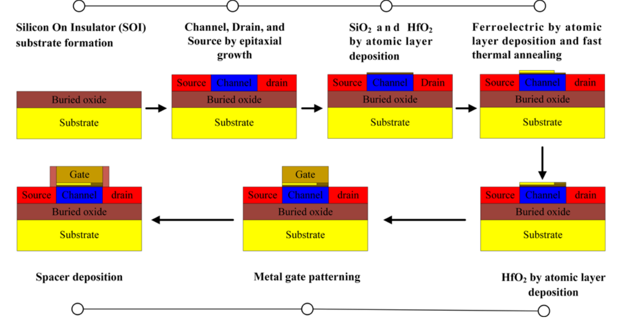

Figure 2: Fabrication process flow of hetero-gate dielectric negative-capacitance field-effect transistors.

3 Results and analysis

3.1 Analysis of NDR effects

The NDR effects occurred in the saturated region, and the drain current (I_{DS}) decreased when V_{DS} increased. This resulted in a negative output conductance (G_{DS}) in the NCFET. By taking the derivative of the output current $I_{DS} = f(V_{IN}, V_{DS})$ using the chain derivative rules, the G_{DS} of the NCFET can be obtained as follows [10],

$$\frac{dI_{DS}}{dV_{DS}} = \frac{\partial I_{DS}}{\partial V_{IN}} \frac{dV_{IN}}{dV_{DS}} + \frac{\partial I_{DS}}{\partial V_{DS}} \tag{3}$$

$$G_{DS} = g_{m,i} \cdot \xi_D + G_{DS,i} \tag{4}$$

where $g_{m,i}$ and $G_{DS,i}$ respectively denote the transconductance and output conductance of the underlying FDSOI. In Equation (5), $g_{m,i}$ and $G_{DS,i}$ are positive; therefore, ξ_D is the only factor that causes the G_{DS} to be negative. In Equation (3), ξ_D is determined by the coupling capacitance C_{GD} and by the capacitance matching between C_{FE} and C_{MOS}. Thus, it is possible to increase ξ_D by increasing $|C_{FE}|$ or decreasing C_{GD} so that G_{DS} tends to zero and the NDR effects are suppressed. As shown in Fig. 3(a), the NDR effects become more pronounced

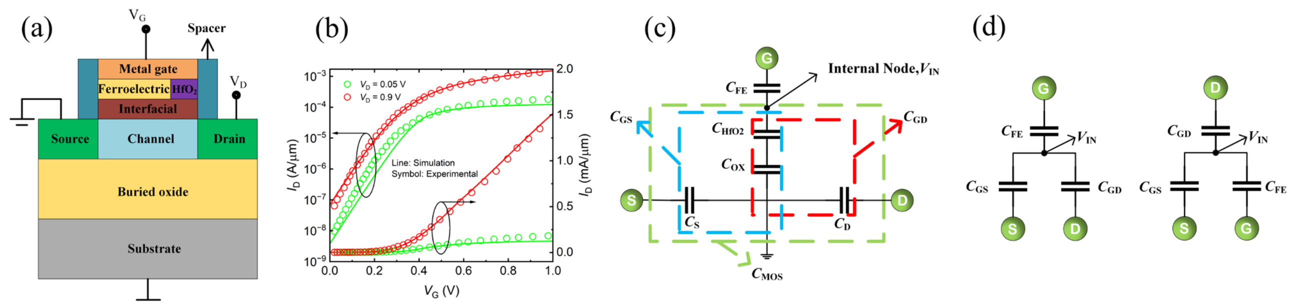

Figure 1: (a) Structure of the hetero-gate dielectric negative-capacitance field-effect transistor device. (b) I_{DS}–V_{GS} calibration plot of 14 nm FDSOI comparisons between technology computer-aided design (TCAD) simulation results (solid line)and experimental data (circles)[18]. (c) Equivalent capacitance circuit for negative-capacitance field-effect transistor. (d) Gate and drain control circuits.

as the ferroelectric thickness (T_{FE}) increases. This is because $|C_{FE}|$ decreases as T_{FE} increases. Equation (3) verifies that the decreases of $|C_{FE}|$ will lead to the decrease of ξ_D; thus, the NDR effects will become more obvious.

As V_{DS} increases in the linear region, two competing effects occur. The first is the reduction in V_{IN}, which reduces I_{DS} according to Equation (3). The other is the increase in the lateral electric field, which increases I_{DS}. As shown in Fig. 3(a), the second effect dominates and I_{DS} increases as a function of V_{DS} in the linear region. However, after the output characteristic enters the saturated region, $G_{DS,i}$ becomes very small. Therefore, a small $|\xi_D|$ will also lead to a negative G_{DS}. Fig. 3(b) shows that the G_{DS} is less than zero, and the NDR effects become more obvious as T_{FE} increases.

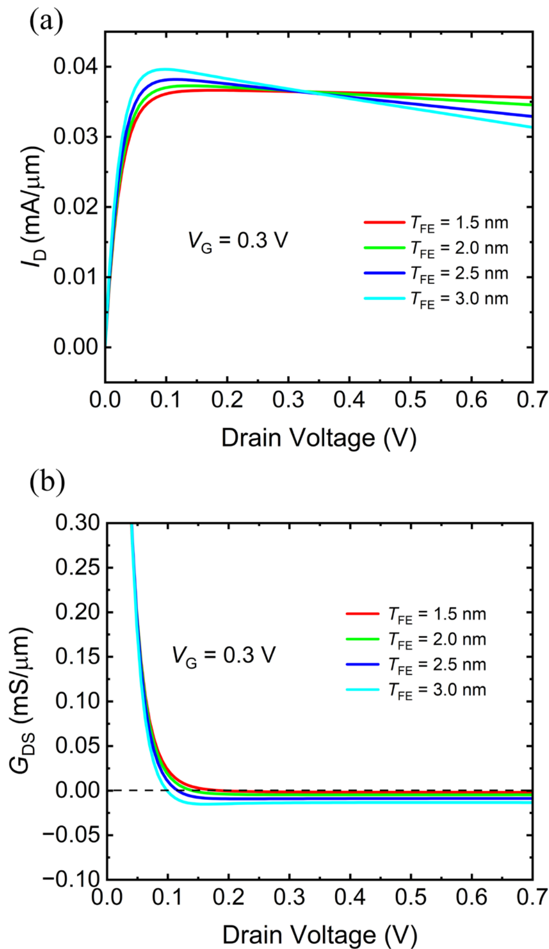

Figure 3: (a) Output characteristic curves (I_{DS}–V_{DS}) at different T_{FE} values. (b) Output conductance plots as a function of V_{DS} at different T_{FE} values.

After the addition of a ferroelectric layer to the dielectric layer of a traditional MOSFET, the amplification of V_{IN} can be demonstrated using Equation (2). Furthermore, V_{IN} increased as a function of T_{FE} in the NCFET. As shown in Fig. 4(a), at V_G = 0.3 V, the channel electrostatic

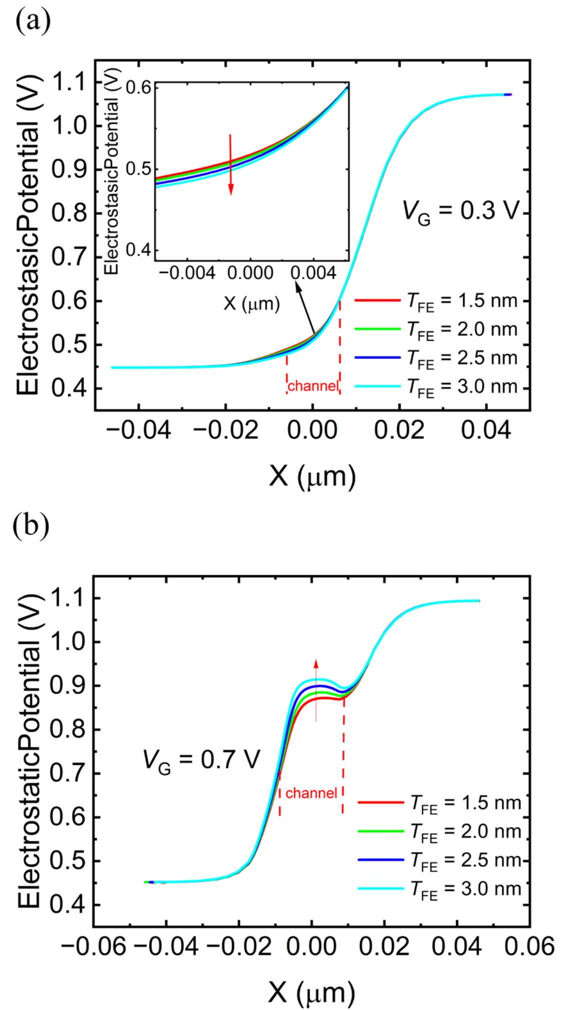

Figure 4: (a) Electrostatic potentials of different T_{FE} values at V_{GS} = 0.3 V. (b) Electrostatic potentials of different T_{FE} values at V_{GS} = 0.7 V.

potential decreases as T_{FE} increases. This is because the amplification of V_{IN} is small when V_G is exceptionally low. Moreover, Equation (3) shows that when T_{FE} increases, ξ_D decreases, and the channel's electrostatic potential decreases. Conversely, as shown in Fig. 4(b), at V_G = 0.7 V, the channel's electrostatic potential increases as T_{FE} increases. This is because the addition of a ferroelectric layer can enhance the electrostatic potential of the channel. As a result, the NDR effects occur at a low V_{GS}.

3.2 Inhibition of NDR effects in HDG-NCFET

The NDR effects were suppressed in the HGD-NCFET. As shown in Fig. 5(a), the suppression of the NDR effects became more pronounced as L_{HK} increased. Moreover, Fig. 5(b) shows that when L_{HK} increases to almost half of the gate length (5 nm), the G_{DS} value tends to zero, indicating the disappearance of the NDR effects. An increase in L_{HK} was accompanied by a decrease in the length of the ferroelectric layer, which led to a decrease in C_{FE}. Fig. 5(c)

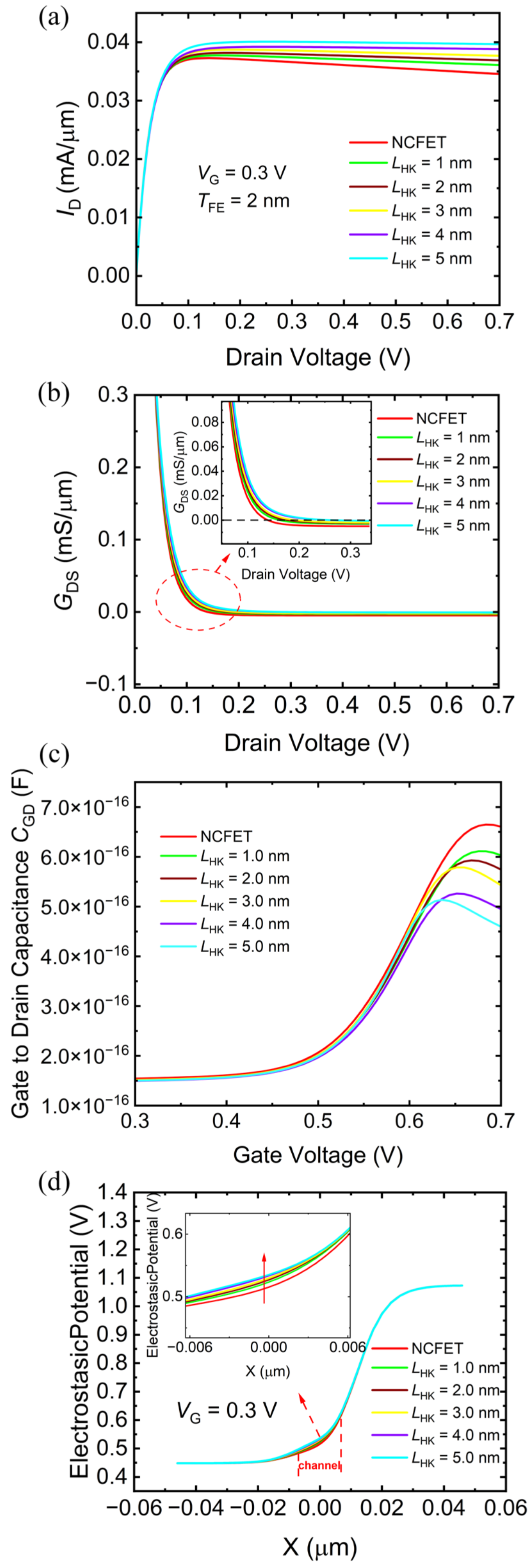

Figure 5: (a) Output characteristic curves as a function of the drain voltage at different L_{HK} values. (b) Output conductance curves as a function of the drain voltage at different L_{HK} values. (c) gate-drain capacitance (C_{GD}) curves as a function of the gate voltage at different L_{HK} values. (d) Electrostatic potentials of different L_{HK} at V_{GS} = 0.3 V.

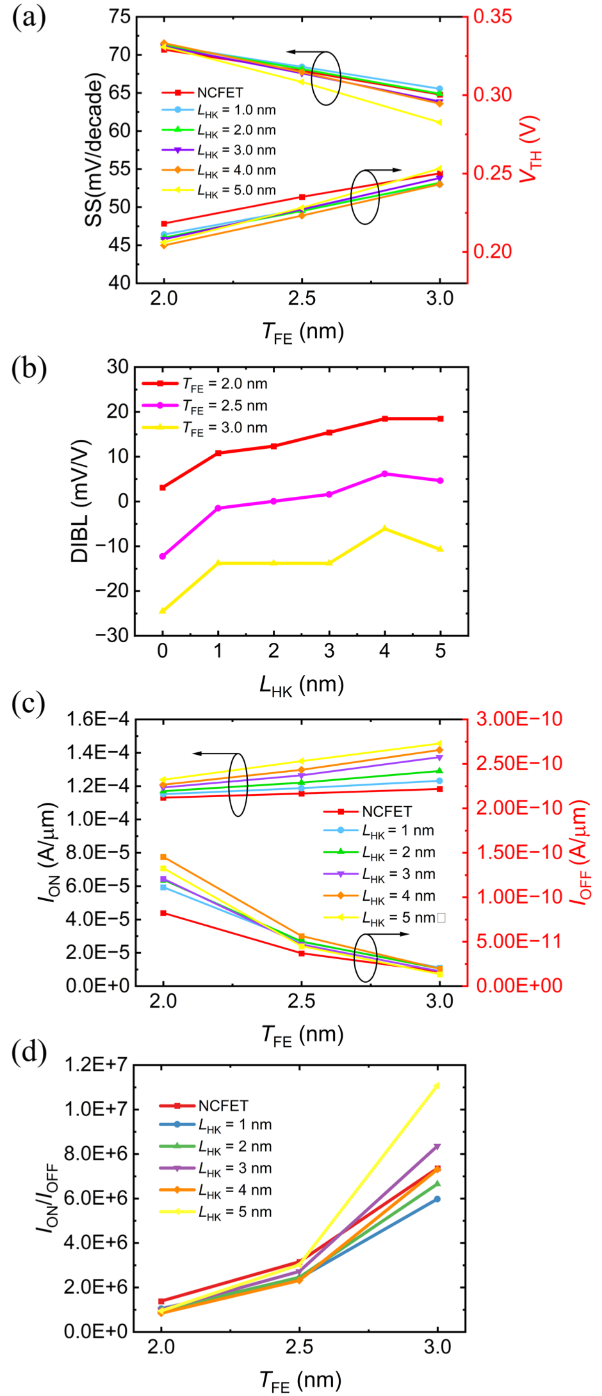

Figure 6: (a) Subthreshold swing (SS) and V_{TH} of HGD-NCFET at different L_{HK} settings. (b) Drain-induced barrier lowering (DIBL) effect of HGD-NCFET at different T_{FE} settings. (c) I_{ON} and I_{OFF} responses of HGD-NCFET at different L_{HK} settings. (d) I_{ON}/I_{OFF} responses of HGD-NCFET at different L_{HK} settings.

illustrates that C_{GD} decreases as L_{HK} increases. Equation (3) indicates that reducing C_{FE} and C_{GD} will increase ξ_D. This results in a larger V_{IN} as L_{HK} increases at the same V_{DS}. Therefore, as shown in Fig. 5(d), the NDR effects are sup-

pressed because the channel electrostatic potential increases with increasing L_{HK}. It was proposed in paper [11] that the NDR effect could be suppressed by increasing the extension length of the drain region, but the NDR effect did not completely disappear with the extension of the drain. And from the transfer characteristic curve, it can be seen that the drain current is decreasing with the increase of the drain length. In the scheme proposed in this paper, the NDR effect is basically completely reduced and the drain current is increased.

To comprehensively compare the performance of the HDG-NCFET with that of the conventional NCFET, the drain-induced barrier lowering (DIBL), SS, threshold voltage (V_{TH}), on-state current (I_{ON}), off-state current (I_{OFF}), and I_{ON}/I_{OFF} were examined. As shown in Fig. 6(a), as T_{FE} increases, SS gradually decreases. When L_{HK} equals to 3 nm, 4 nm, and 5 nm, the SS is lower than that of the NCFET. This is because an increase in T_{FE} leads to a decrease in $|C_{FE}|$, thus resulting in better capacitance matching between C_{FE} and C_{MOS}. Similarly, in Fig. 6(a), the V_{TH} values of NCFET and HGD-NCFET are almost the same. As shown in Fig. 6(b), compared to the conventional NCFET without L_{HK}, the DIBL effect of the HGD-NCFET is slightly worse. This is because the DIBL effect yields larger I_{DS} outcomes as V_{DS} increases. However, the NDR effects cause I_{DS} to decrease when V_{DS} increases. Therefore, the DIBL effect is apparent when the NDR effects are inhibited. However, the DIBL effect can be mitigated by increasing T_{FE}. This is because the increase in T_{FE} causes the channel barrier becoming higher. As illustrated in Fig. 6(c), when T_{FE} = 2 nm, the I_{OFF} results of the HGD-NCFET are larger than that of the NCFET. This is because the electrostatic potential of the NCFET being lower than those of the HGD-NCFET at a low V_{GS}. Meanwhile, I_{OFF} decreases as T_{FE} increases. Furthermore, I_{ON} increases as a function of T_{FE}. This is because the SS decreases rapidly as T_{FE} increases. As shown in Fig. 6(d), when T_{FE} is equal to 2 nm and 2.5 nm, the I_{ON}/I_{OFF} values are close to those of NCFET at different L_{HK} settings. However, at T_{FE} = 3 nm and L_{HK} = 5 nm, the I_{ON}/I_{OFF} values of the HGD-NCFET are larger than those of the NCFET.

The analogue/RF characteristics of the HGD-NCFET were analyzed by studying its small signal. Fig. 7(a) illustrates the total capacitance (C_{GG}) of HGD-NCFET

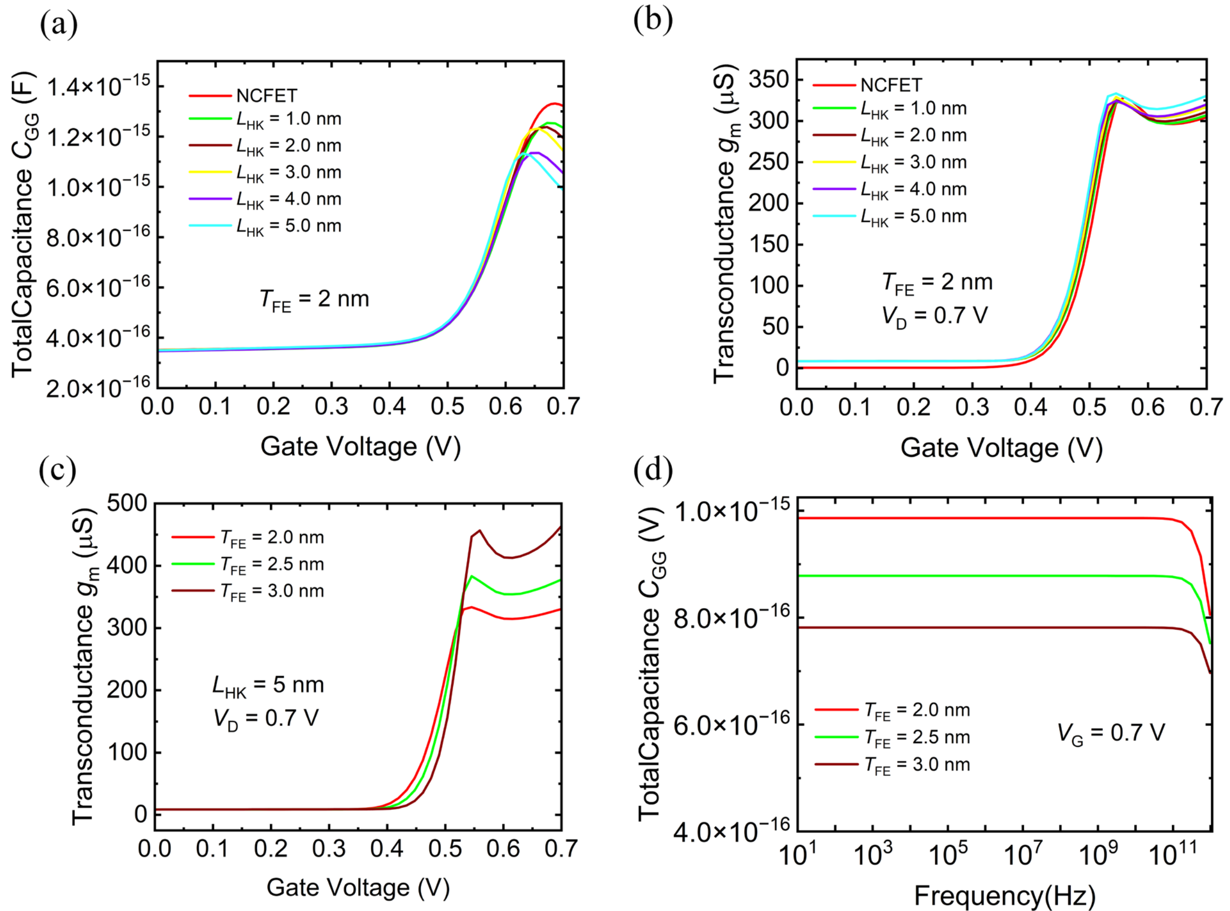

Figure 7: (a) total capacitance (C_{GG}) curves as a function of the gate voltage at different L_{HK} values. (b) transconductance (g_m) curves as a function of the gate voltage at different L_{HK} values. (c) g_m curves as a function of the gate voltage at different T_{FE} values. (d) C_{GG} curves as a function of the frequency at different T_{FE} values.

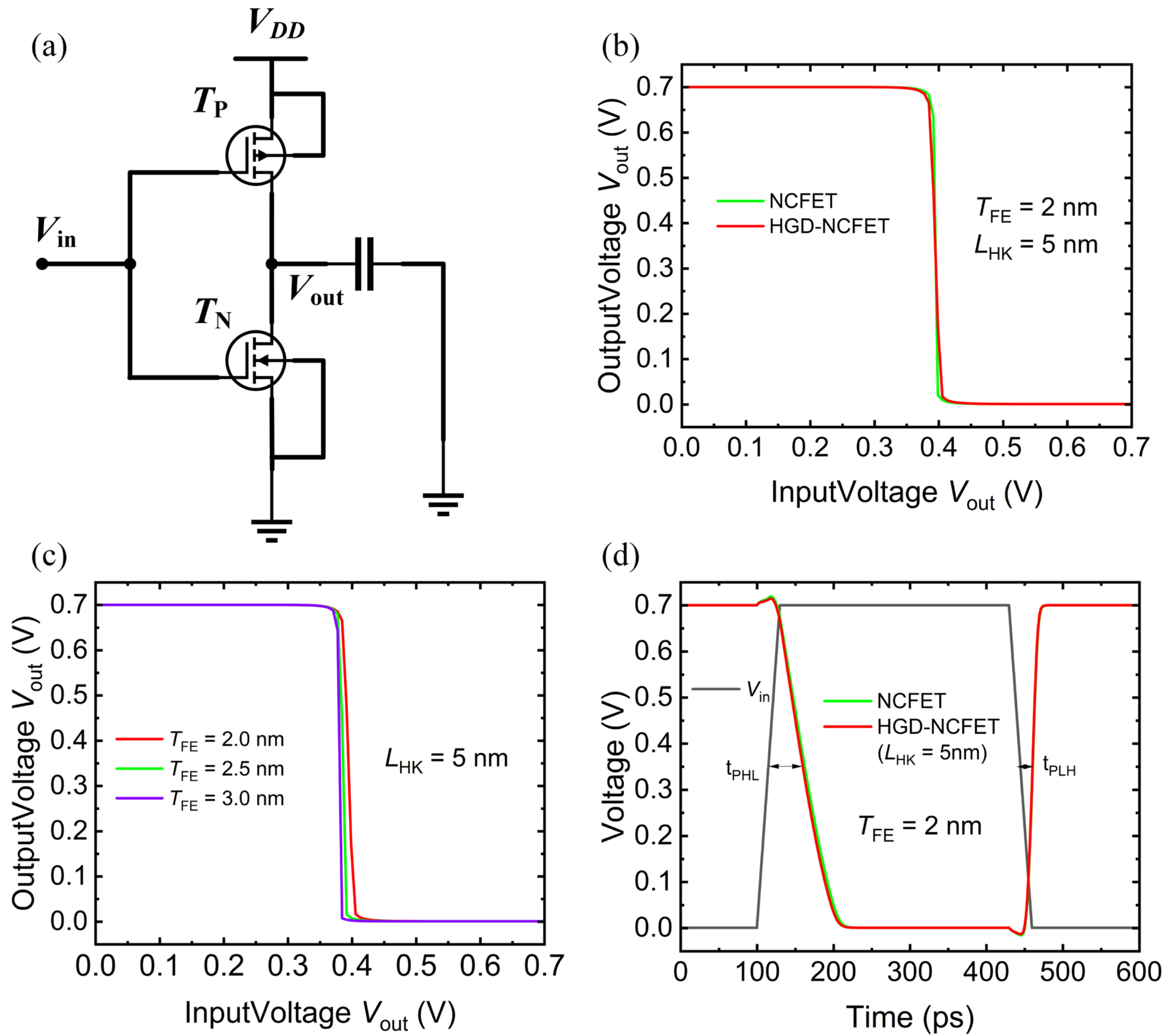

Figure 8: (a) implementation of CMOS inverter employing HGD-NCFET. (b) voltage transfer characteristic curves of inverter composed of NCFET and HGD-NCFET. (c) voltage transfer characteristic curves of inverter composed of HGD-NCFET at different T_{FE} values. (d) input-output waveform of inverter composed of NCFET and HGD-NCFET.

under different L_{HK} values at T_{FE} = 2 nm. It can be seen that C_{GG} decreases with the increase of L_{HK}. This is because replacing ferroelectricity on the drain side with a high-κ material leads to a reduction in C_{GD}, as shown in Fig. 5(c). Therefore, as the L_{HK} increases, the C_{GG} will decrease. Enhancing the transconductance (g_m) of transistors can significantly impact analogue circuitry. This improves amplifier performance, enhances linearity, reduces distortion, increases interference immunity, and lowers power consumption. Therefore, studying the g_m of HGD-NCFET is necessary. Fig 7.(b) shows the g_m of HGD-NCFET under different L_{HK} values at T_{FE} = 2 nm. The results indicate that g_m slightly increases with an increase in L_{HK} and surpasses that of NCFET. Meanwhile, as shown in Fig 7.(c), increasing T_{FE} significantly enhances the value of g_m. This is because an increase in T_{FE} results in a higher effective gate electric field of the HGD-NCFET. Fig 7.(d) shows the curve of C_{GG} as a function of frequency. It is evident that C_{GG} remains stable within the range of 10Hz to 100GHz, indicating the device's stable operation in the low, high, and ultra-high frequency.

To expand the study of HGD-NCFET to circuits, we designed a CMOS inverter comprising of n-type and p-type HGD-NCFET, as shown in Fig. 8(a). The simulation results of the voltage transfer characteristics of the inverter are shown in Fig. 8(b). It is evident that the voltage transfer curves of the NCFET and HGD-NCFET are similar in steepness. Furthermore, Fig. 8(c) illustrates that the voltage transfer curve of the HGD-NCFET becomes steeper as the T_{FE} value increases at L_{HK} = 5 nm. This is because the inner gate voltage of the HGD-NCFET is amplified more strongly as T_{FE} increases. Fig.

8(d) shows the variation in transient response of the inverter, where t_{PHL} and t_{PLH} represent the transition delay from high to low and from low to high voltage, respectively. The t_{PHL} of the HGD-NCFET is slightly smaller than that of the NCFET, while the t_{PLH} remains almost constant for both. This indicates that the transfer speed of the HGD-NCFET is faster compared to the NCFET.

4 Conclusion

In this study, an HGD-NCFET was proposed to suppress the NDR effects in NCFET by partly replacing the ferroelectric layer with a high-κ material on the drain side. The results showed that this structural device can improve the coupling factor between the gate and the drain to increase the electrostatic potential of the channel. The suppression of the NDR effects became more prominent when the length of high-κ material increased. In addition, compared with the traditional NCFET, HGD-NCFET had a steeper subthreshold swing when the length of the high-κ material was almost half of the channel length. Simultaneously, the DIBL effect was mitigated with an increase in the ferroelectric thickness. Finally, the switching current ratio of the HGD-NCFET was essentially the same or even higher than that of the traditional NCFET. Therefore, compared with traditional NCFET, HGD-NCFET not only has similar electrical performances but also suppresses the NDR effects. HGD-NCFET has a higher transconductance than NCFET. Additionally, the inverter composed of HGD-NCFET exhibits a shorter transmission delay. In future investigations, we will examine the DIBL effect of HGD-NCFET as its suppression deteriorates with the increase of L_{HK}. The preliminary idea is to better suppress the DIBL in HGD-NCFET by modifying the parameters of the spacer. In addition, we will look for effective ways to further reduce the transmission delay of the HGD-NCFET.

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