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A Placement and Routing Method for Layout Generation of CMOS Operational Amplifiers Using Multi-Objective Evolutionary Algorithm Based on Decomposition

Mehran Nohtanipour[1], Mohammad Hossein Maghami[,2], Mehdi Radmehr[1]*

[1]Department of Electrical Engineering, Sari Branch, Islamic Azad University, Sari, Iran
[2]Faculty of Electrical Engineering, Shahid Rajaee Teacher Training University, Tehran, Iran

Abstract: This paper presents a new placement and routing method for layout generation of CMOS operational amplifiers (op-amps). Both circuit sizing and layout generation stages are performed automatically. In the proposed method, layout effects are considered during the layout generation. Layout parasitics and geometry information are extracted from a new automated layout generator. In this method, the multi-objective evolutionary algorithm based on decomposition (MOEA/D) is used as an optimization algorithm. In order to verify the performance of the proposed method, the design of three-stage operational amplifier (op-amp) and two-stage class-AB operational trans-conductance amplifier (OTA) in a 0.18µm process CMOS technology with 1.8 V supply voltage are presented. The simulation results indicate the efficiency of the proposed analog layout generation method.

Keywords: Analog layout generation; Circuit sizing; Automated placement and routing; MOEA/D; Three-stage operational amplifier

Metoda umeščanja in usmerjanja za generiranje postavitve operacijskih ojačevalnikov CMOS z uporabo večciljnega evolucijskega algoritma na osnovi dekompozicije

Izvleček: Članek predstavlja novo metodo umeščanja in usmerjanja za izdelavo postavitve operacijskih ojačevalnikov CMOS (op-amperov). Fazi določanja velikosti vezja in generiranja postavitve se izvajata samodejno. Pri predlagani metodi se med generiranjem postavitve upoštevajo učinki postavitve. Parazitske lastnosti postavitve in informacije o geometriji se pridobijo iz novega samodejnega generatorja postavitve. V tej metodi se kot optimizacijski algoritem uporablja večobjektni evolucijski algoritem, ki temelji na dekompoziciji (MOEA/D). Da bi preverili učinkovitost predlagane metode, sta predstavljeni zasnova tristopenjskega operacijskega ojačevalnika (op-amp) in dvostopenjskega operacijskega ojačevalnika razreda AB (OTA) v tehnologiji CMOS z 0,18 µm procesom in napajalno napetostjo 1,8 V. Rezultati simulacije kažejo učinkovitost predlagane metode generiranja analogne postavitve.

Ključne besede: Generiranje analogne postavitve; Določanje velikosti vezja; Avtomatizirano umeščanje in usmerjanje; MOEA/D; Tristopenjski operacijski ojačevalnik

** Corresponding Author's e-mail: mhmaghami@sru.ac.ir*

1 Introduction

Analog circuit design includes three main steps as follows [1], [2], [3], [4]: topology synthesis / selection, circuit sizing and layout design. In the first step, a proper circuit topology is selected by a designer. The second step is sizing devices with the aim of finding proper width and length of the transistors, passive components values,

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bias voltages and currents. Finally, the layout should be generated from the previous step. In the analog integrated circuit (IC) design, it is often required to optimize different specifications simultaneously. Designing the circuit can be performed manually which is a difficult task and takes lots of time. There are large number of circuit sizing methods in the literature [5], [6], [7], [8], [9]. In the knowledge-based approach, sizes of circuit devices are determined based on some pre-defined design flows and databases. However, this method is time-consuming and there is no guarantee to convergence to the global optimum solution. Optimization-based methods can be divided into three categories as follows: "equation-based", "simulation-based" and "equation and simulation-based" methods [10], [11]. In the equation-based method, mathematical solvers are used to solve the circuit equations and satisfy the target specifications. In the simulation-based method, a circuit simulator is used to evaluate the target specifications for a set of design variables. Finally, to have a compromise between speed and accuracy of the two mentioned methods, equation and simulation-based method was utilized in some designs [12].

Automatic analog layout generation has been considered by analog circuits designers [13]. In the literature, several Computer-Aided Design (CAD) tool [14], [15]. shave been introduced for analog circuits layouts. However, circuit sizing and layout generation steps are not regarded simultaneously. Since circuit performance can be influenced by layout parasitics, the circuit specifications may not be satisfied after post-layout simulation. The behavior of analog integrated circuits is sensitive to layout-induced parasitics. To achieve desired specifications, time-consuming and non-systematic iterations between these circuit sizing and layout synthesis are required [16]. If these issues are not taken into account, circuit overdesign may occur which results in wasting power and area. On the other hand, circuit underestimation may lead to a worsening of post-layout performance. It is useful to perform circuit sizing and layout generation steps automatically.

Some approaches have been proposed in the analog circuit domain to assist the designers. But some procedures should be performed manually. Optimization-based sizing approaches are employed for analog IC design automation using the circuit simulators as evaluation engines [17], [18]. The quality of a design is evaluated by the degree to which constraints are satisfied and also desired specifications are achieved. In order to achieve the better sizing results, the layout effects should be considered. The layout-aware sizing method consists of parasitic-aware sizing and geometry-aware sizing [19], [20]. In parasitic-aware sizing method, parasitics of the layout are extracted continuously and then they are utilized in the sizing process. In the geometry-aware sizing method, the value of geometrical parameters such as width, length, and the number of fingers of MOS transistors are chosen such that the layout area and shape to be optimized. Several analog layout-aware sizing methods have been introduced in the literature.

Parametric generators are used that code the whole layout of the circuit to increase execution speed. However, their definition is time-consuming and the solutions for devices' sizes may differ from the ones intended in the definition step [21], [22], [23]. In Ref [24], a predefined floorplan template supported by a slicing tree is used. To obtain the desired geometric features, the number of fingers of MOS transistors should be adjusted. A similar idea is suggested by minimizing the placement area using convex optimization [25]. However, placement solutions are not compact. In Ref [26], parasitics estimation are performed without actual layout generation. However, these methods suffer from the fixed layout template used for layout generation or parasitic model construction. A method to model the parasitics associated with inductors during RF circuit synthesis is suggested [27]. The post-layout results may not be acceptable since other parasitics are not considered. A method is proposed to estimate parasitics from earlier placement information and includes this during the circuit resizing stage. Since the parasitic information is related to a single design, it does not take the parasitic variation and it may not be sufficient to use in resizing stage [28].

Layout with templates and commercial extractors is used in Ref [29], In this method, symbolic analysis is employed to combine the parasitics with the performance models. But, geometrical information is not taken into account. A parasitic-aware sizing method is suggested in Ref [30], This method is only applicable to a pre-defined floorplan. A placement and routing method for analog layout generation based on a modified cuckoo optimization algorithm (MCOA) is introduced in Ref [31] In this method, layout parasitics are considered to avoid performance deterioration. But, the placement and routing stages have some shortcomings as it will be discussed in this paper. In Ref [32], an automatic method to generate chip floorplans is proposed. The obtained results are superior or comparable to the solutions produced by designers in terms of power consumption, performance and chip area. In order to achieve this aim, chip floorplanning is considered as a reinforcement learning problem. An edge-based graph convolutional neural network architecture is introduced which has the characteristics of learning rich and transferable representations of the chip.

This paper presents a new technique for placement and routing in analog layout generation using the MOEA/D.

Circuit performance and layout effects are considered in the proposed method. In addition, geometrical information is regarded in the proposed method. The rest of the paper is organized as follows: Multi-objective evolutionary algorithm based on decomposition is introduced in Section 2. The proposed automatic analog layout generation method is described in Section 3. Simulation results are provided in Section 4. Finally, the conclusion is given in Section 5.

2 Multi-objective evolutionary algorithm based on decomposition (MOEA/D)

At present, engineering designs are not usually a simple optimization problem. Multiple objectives are usually desired especially when conflicting operations exist between the optimization searching for different design specifications. During the past decades, evolutionary multi-objective optimization (EMO) has been used by many researchers in the area of intelligent computing [33], [34]. EMO algorithms have advantages in exploring a set of Pareto-optimal solutions compared to traditional methods. Many EMO algorithms utilize Pareto dominance for fitness assignment. In these algorithms, the fitness value of each individual is achieved by comparing it with other individuals in terms of Pareto dominance. therefore, all non-dominated solutions in the population should have the best fitness value.

In this paper, multi-objective optimization problems can be considered as follows:

$$\begin{aligned} &\text{Minimize}\,(f_1(x), f_2(x), \ldots, f_M(x)) \\ &\text{Subject to}\, g(x) \geq 0, X_L < x < X_H \end{aligned} \tag{1}$$

where $f_i(x)$, $i = 1 \ldots M$ is the objective function, M is the number of objectives, x includes design variables, and X_L and X_H are their lower and upper bounds, respectively. The vector $g(x) \geq 0$ represents the design constraints.

A multi-objective evolutionary algorithm based on decomposition (MOEA/D) has been proposed for multiobjective optimization problem (MOP) [35]. In MOEA/D, a MOP is decomposed into several scalar subproblems in which the optimization is performed simultaneously. Using the information on solutions of neighborhood subproblems, this method has less computational cost, which has been proved by several numerical tests.

The motivation of MOEA/D is to decompose a multi-objective optimization problem into several scalar optimization sub-problems using a scalar function. In this method, optimization is performed simultaneously by the evolutionary algorithm. In MOEA/D, each non dominated solution of the multi-objective optimization problem is related to an optimal solution of the single objective optimization problem and it is computed using a specific weight vector. MOEA/D uses a set of weight vectors to set up different search directions, and different weight vectors will direct to search the different regions of the objective space. The Tchebycheff method can be used to decompose a multi-objective optimization problem into N sub-problems. In this method, the objective function of the *jth (j=1, 2, ..., N)* sub-problem is as follows:

$$g^{te}(x \mid \lambda^j, z^*) = \max_{1 \leq i \leq m} \left\{ {\lambda_i}^j \mid f_i(x) - z_i^* \mid \right\} \tag{2}$$

where $\lambda^j = \left({\lambda_1}^j, \ldots, {\lambda_m}^j\right)^T$ demonstrates a weight vector, $z^* = \left(z_1^*, \ldots, z_m^*\right)^T$ represents the vector of reference points. For each Pareto optimal point x^* there exists a weight vector so that x^* is the optimal solution of (2). The methods to determine the weight vector can be found in the related references such as Ref [36]. It should be mentioned that each optimal solution of Eq. (2) is a Pareto optimal solution of the problem of Eq. (1).

3 Proposed Placement and Routing Method

In this Section, the proposed placement and routing stages based on the MOEA/D are described.

3.1 Placement

In the placement stage, the area of floorplan is optimized by simultaneous consideration of symmetry and proximity constraints. It is necessary to place the devices by considering symmetry and proximity constraints to alleviate the parasitic coupling effects and also to improve circuit performance. Therefore, they are briefly reviewed here [37]. A set of m symmetry groups can be shown by $S = \{S_1, S_2, \ldots, S_m\}$. The coordinates of the symmetry axes are indicated by $(\hat{x}_i, \hat{y}_i)$. A member of the groups is described as follows:

$$\begin{aligned} S_i = \{&(\mathrm{M}_1, \mathrm{M}_1'), (\mathrm{M}_2, \mathrm{M}_2'), \ldots, (\mathrm{M}_u, \mathrm{M}_u') \\ &, \mathrm{M}_1^s, \mathrm{M}_2^s, \ldots, \mathrm{M}_v^s\} \end{aligned} \tag{3}$$

This group includes u symmetry pairs $(\mathrm{M}_j, \mathrm{M}_j')$ with coordinates centers (x_j, y_j) and (x_j', y_j') and v self-symmetric modules M_k^s with coordinate center (x_s^k, y_s^k). The conditions for symmetry group with vertical symmetric axis are indicated by (4) - (6), and

equations set (7) - (9) are used for those with horizontal axis.

$$x_j + x'_j = 2 \times \hat{x_i}, \ \forall i = 1, 2, ..., u. \quad (4)$$

$$y_j = y'_j, \ \forall i = 1, 2, ..., u. \quad (5)$$

$$x_s^k = \hat{x_i}, \ \forall k = 1, 2, ..., v. \quad (6)$$

$$x_j = x'_j, \ \forall i = 1, 2, ..., u. \quad (7)$$

$$y_j + y'_j = 2 \times \hat{y_i}, \ \forall i = 1, 2, ..., u. \quad (8)$$

$$y_s^k = \hat{y_i}, \ \forall k = 1, 2, ..., v. \quad (9)$$

The proximity condition is described as follows:

$$\sigma^2(\Delta P) = \frac{A_P^2}{WL} + S_P^2 D_x^2 \quad (10)$$

where Δ*P* is the difference of an electrical parameter *P*, A_p is the area proportionality constant for *P*, *W* and *L* are the respective width and length of the device, and S_p is the variation of *P* under the device spacing D_x. As can be seen from the above equation, it is necessary to place the symmetry group together as close as possible.

For two groups of modules such as A and B, a common centroid constraint is defined as below:

$$\sum_{a \in A} \left(x_a + \frac{\omega_a}{2} \right) = \sum_{b \in B} \left(x_b + \frac{\omega_b}{2} \right) \quad (11)$$

$$\sum_{a \in A} \left(y_a + \frac{h_a}{2} \right) = \sum_{b \in B} \left(y_b + \frac{h_b}{2} \right) \quad (12)$$

In the above equations, (x, y) and (ω*h*) show the lower left coordinates and the width and height of the modules, respectively.

In addition, design rules should be satisfied at this stage. A method for handling constraints would be to consider them as new objective functions. If g(x) ≥ 0 must hold, for instance, we can transform this to a new objective function $f_{new}(x) = \min\{-g(x), 0\}$ subject to minimization.

The devices to be placed on the floorplan are represented by *k* modules $M_1, \ldots, M_k$. The objective functions are defined for the placement stage as follows:

$$f_P(x) = (f_{oP1}(x), -f_{oP2}(x)) \quad (13)$$

$$f_{oP1}(x) = Width_{floorplan} \times Height_{floorplan} \quad (14)$$

$$f_{oP2}(x) = \frac{Total\ Blocks\ Area}{Width_{floorplan} \times Height_{floorplan}} \quad (15)$$

In the above equation, $x = \{(x_1, y_1), ..., (x_k, y_k)\}$ indicates the coordinates of the left-bottom corners of the modules, $f_{oP1}(x)$ is the area of the floorplan. $Width_{floorplan}$ and $Height_{floorplan}$ represent the floorplan width and height, respectively. The term area utilization is defined by $f_{oP2}(x)$ and it is no greater than 1. It is worth to mention that the $f_p(x)$ is formulated to deal with a minimization optimization problem. In the placement stage, optimization is performed using the MOEA/D.

3.2 Routing

The routing stage aims to electrically connect the terminals of the layout devices such as transistors, capacitors, differential pairs. In this proposed method, each wire is divided into d segments. Each segment is represented by segment direction, segment layer. Segment direction can be defined as up, down, left, and right. Segment is located in the layers from 1 to n, where n is the number of the layers.

Positions of the segments are adjusted automatically so that the wire length between terminal pairs to be minimized. The objective functions for the routing stage are proposed as follows:

$$f_R = (f_{oR1}(x), f_{oR2}(x), f_{oR3}(x)) \quad (16)$$

$$f_{oR1}(x) = \sum_{i=1}^{d} Length_{Segment_i} \quad (17)$$

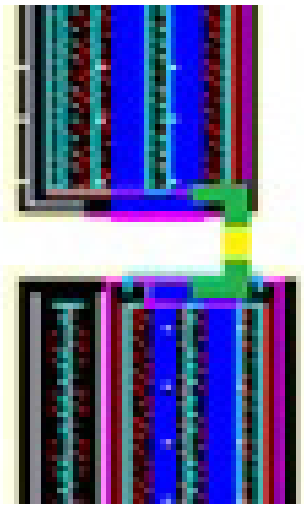
$$f_{oR2}(x) = Number\ of\ Vias \quad (18)$$

$$f_{oR3}(x) = Number\ of\ bends \quad (19)$$

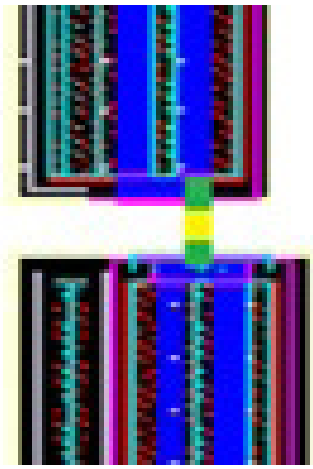
Where $f_{oR1}(x)$ is the sum of the segment lengths from the starting terminal (T_S) to the target terminal (T_E) (See Figure1). $(x_{T_S}, y_{T_S}, z_{T_S})$ and $(x_{T_E}, y_{T_E}, z_{T_E})$ are the coordinates of the starting terminal and the target terminal, respectively. $f_{oR2}(x)$ is the number of vias in the wire. $f_{oR3}(x)$ is the number of bends in the wire and it is defined to avoid unnecessary change of direction between adjacent segments. It is worth to mention that it is not considered in the Ref [31]. Current-density to determine the segment width and design rules are the constraints in the routing stage. An example of wiring progress using the proposed method is demonstrated in Figure 2. In this Figure, different segment colors indicate transition between layers.

Figure 1: Wire segmentation in the proposed method.

(a)



(b)



(c)

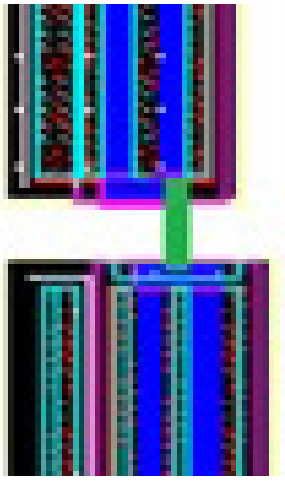


Figure 2: Example of routing stage progress using the proposed method: **(a)** Wiring between two terminals after 1 generation, **(b)** Wiring between two terminals after 10 generations, **(c)** Wiring between two terminals after 100 generations.

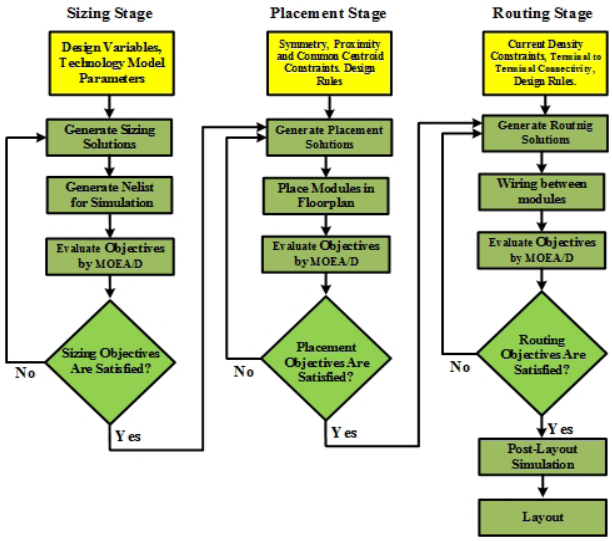


Figure 3: Flowchart of the proposed analog layout generation method.

3.3 Proposesd layout generation method

The flowchart of the proposed analog layout generation method is shown in Figure3. The proposed method details are as follows:

Sizing Stage
Inputs: Design variables such as width, length, and the number of fingers of the MOS transistors, bias voltages, the values of the passive components, and technology models parameters.

Sizing Procedure:
Step 1: Solutions are provided using the optimization algorithm. It this paper, it is performed by the MOEA/D.
Step 2: After providing the solutions by the MOEA/D, a netlist is created. Schematic simulation should be performed to evaluate the circuit specifications. In this paper, simulation is performed using HSPICE software.
Step 3: Specifications of the circuit such as DC-gain, phase margin (PM), power dissipation (P_{diss}), settling time (ST), slew rate (SR) and unity-gain-bandwidth (UGBW), are evaluated from the schematic simulation results.
Step 4: If the specifications are satisfied, the solutions are given to the placement stage. Otherwise, new solutions should be found by the MOEA/D.

Placement Stage
Inputs: Symmetry, proximity and common centroid constraints, design rules, device sizes from the sizing stage.
Placement Procedure:
Step 5: The coordinates of the left-bottom corners of the modules are chosen by the MOEA/D.
Step 6: The modules are placed in the floorplan using the solutions obtained from the previous step.

Step 7: In this step, the placement objectives are evaluated. A compact floorplan should be produced in the placement stage by simultaneous consideration of design rules and the other constraints.
Step 8: If the placement objectives are satisfied, the solutions are given to the routing stage. Otherwise, new solutions should be provided by the EMO.

Routing Stage
Inputs: Current-density constraints, terminal to terminal connectivity, design rules, floorplan from the placement stage.

Routing Procedure:
Step 9: In this step, the obtained floorplan from the placement stage is given to the router. The solutions are generated by the router.
Step 10: Based on the segment positions, wiring between terminals are performed.
Step 11: The routing objectives according to the Section 3.2 are evaluated.
Step 12: If the routing objectives are satisfied, the solutions are given to the next stage. Otherwise, MOEA/D is looking for new solutions.
Step 13: After extracting the parasitics of the obtained layout, post-layout simulation is performed. Parasitics extraction are done using a resistance-capacitance (RC) π model that is suggested in Ref [38]. If post-simulation on routing stage somehow fails, to find new solutions the routing stage should be repeated. It usually takes a few repetitions to get the answer.
Step 14: The final layout of the proposed method is drawn.

4 Performance Evaluation

The proposed analog layout generation method is performed in a 0.18µm 1.8V CMOS technology. An automatic MATLAB toolbox is provided which is connected to HSPICE. MOEA/D is implemented in MATLAB R2016b version and is tested on Intel corei5-4460 CPU @ 3.2 GHz with 16 GB RAM. Operational amplifiers (op-amps) can be considered as an essential block in many mixed-mode systems [39-42].The proposed method is applied to three-stage amplifier and two-stage class-AB operational trans-conductance amplifier (OTA).

4.1 Three-stage amplifier

In Ref [42], optimization of the settling performance of a three-stage amplifier shown in Figure 4 is studied. In the following, designing the three-stage op-amp shown in Figure 4 is presented.

$$f(x) = (f_1(x), f_2(x), f_3(x), f_4(x), f_5(x), f_6(x)) \quad (20)$$

In the above equation , $f_1(x)$=-1xDC-gain, $f_2(x)$=-1xPM, $f_3(x)$=-1xUGBW, $f_4(x)$=-1xSR, $f_5(x)$=-P_{diss}, and $f_6(x)$=ST.x represents the design variables. Designing is performed using minimum channel length transistor (0.18µm), and the widths of the MOS transistors are chosen as 2µm≤ Wj ≤150µm. MOEA/D is executed with a population of 100 individuals with 250 iterations. It should be noted that in each iteration, the z^* in selected as the minimum of the z^* and the cost function. One solution to the sizing result is shown in Table 1. The placement and routing results are done by the layout generator and the result is depicted in Figure 5. The area of the layout is 34µm×32µm. The total number of wires is 23. In this Figure, metal 1 and metal 2 are shown by green and yellow colors, respectively.

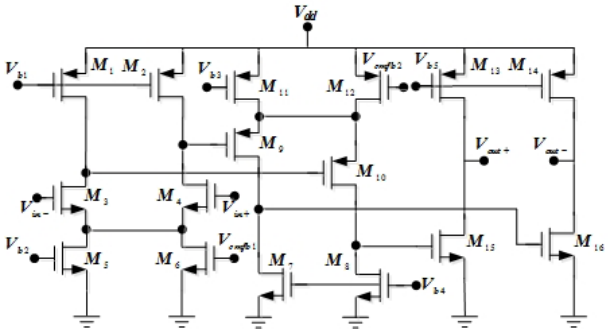


Figure 4: CMOS Three-Stage op-amp [42].

Table 1: Size of transistors for the three-stage op-amps.

Parameter	Value
$(W/L)_{1,2}$	10x10µm/0.18 µm
$(W/L)_{3,4}$	8x6.25µm/0.18 µm
$(W/L)_{5,6}$	10x5µm/0.18 µm
$(W/L)_{7,8}$	16x3.125µm/0.18 µm
$(W/L)_{9,10}$	16x6.25µm/0.18 µm
$(W/L)_{11,12}$	16x12.5µm/0.18 µm
$(W/L)_{13,14}$	10x20µm/0.18 µm
$(W/L)_{15,16}$	10x4µm/0.18 µm

The open-loop frequency responses of the designed op-amp in demonstrated in Figure 6. The results show that the DC-gain is 72 dB after post-layout simulation. UGBW and PM of the Op-Amp are 720 MHz and 82°, respectively. A 0.4 V step voltage is applied to the op-amp and the 1% ST is calculated. The obtained step response is shown in Figure 7. The results shown in the Figures 6 and 7 are also obtained by the Cadence software. It should be mentioned that the proposed method results are consistent with the Cadence software.

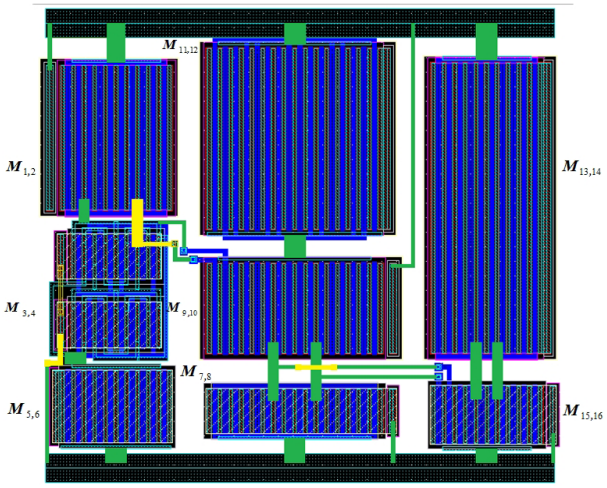


Figure 5: The three-stage amplifier layout generated by the proposed method.

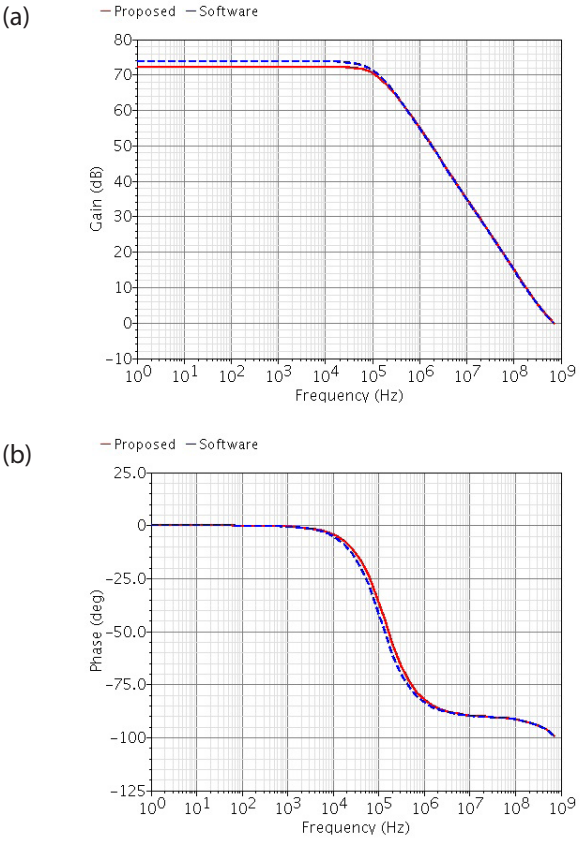


Figure 6: Three-stage op-amp frequency response: **(a)** magnitude, **(b)** phase.

The Pareto optimal fronts (POFs) of the three-stage op-amp including ST versus P_{diss}, DC-Gain versus P_{diss}, SR versus P_{diss} and UGBW versus PM are shown in Figure 8. As can be seen from the Figure 8.a, the proposed method can achieve better ST compared to the existing methods [14], [31]. Table 2 reports the comparisons of post-layout simulation results of the proposed method with the existing methods. The main advantage of the proposed method compared with the existing methods is that the sizing stage is not considered in the existing methods. In addition, a set of solutions are provided by MOEA/D in the proposed method compared to the single solution in the [31]. In the [31], area utilization and number of bends are not included for the placement and routing stages, respectively. It is essential to define initial wires and some operators for the routing stage in the [14]. The ST, layout area and also area utilization of the proposed method is better than the existing methods with the cost of a little increase in the runtime. Therefore, the proposed method is more suitable for automatic analog layout generation.

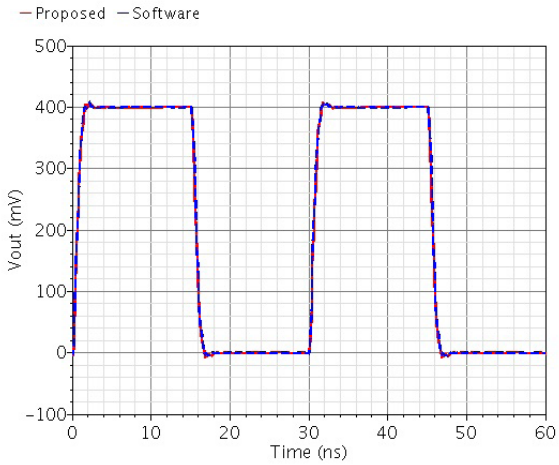


Figure 7: Three-stage op-amp step response.

Table 2: Comparisons of the post-layout simulation results for three-stage amplifier.

No.	Specifications	Post-layout performance		
		This work	[31]	[14]
1	1% Settling time (ns)	<4.4	4.9	5.2
2	Total runtime (s)	1531	1266	1134
3	Layout Area (mm2)	0.0011	0.0013	0.0014
4	Area Utilization (%)	88	82	76

4.2 Two-stage class-AB OTA

In Ref [41], a two-stage class-AB OTA is suggested. By increasing the trans-conductance of the first stage, DC-gain is enhanced. Non-linear current mirror boosts the current of the second stage. As a result, the SR is improved. The OTA is shown in Figure 9. Analytical equations are provided in the Ref. 41. The placement and routing results are obtained from the proposed method and the result is shown in Figure 10. The area of the layout is 130μm×195μm. The POFs of the two-stage class-

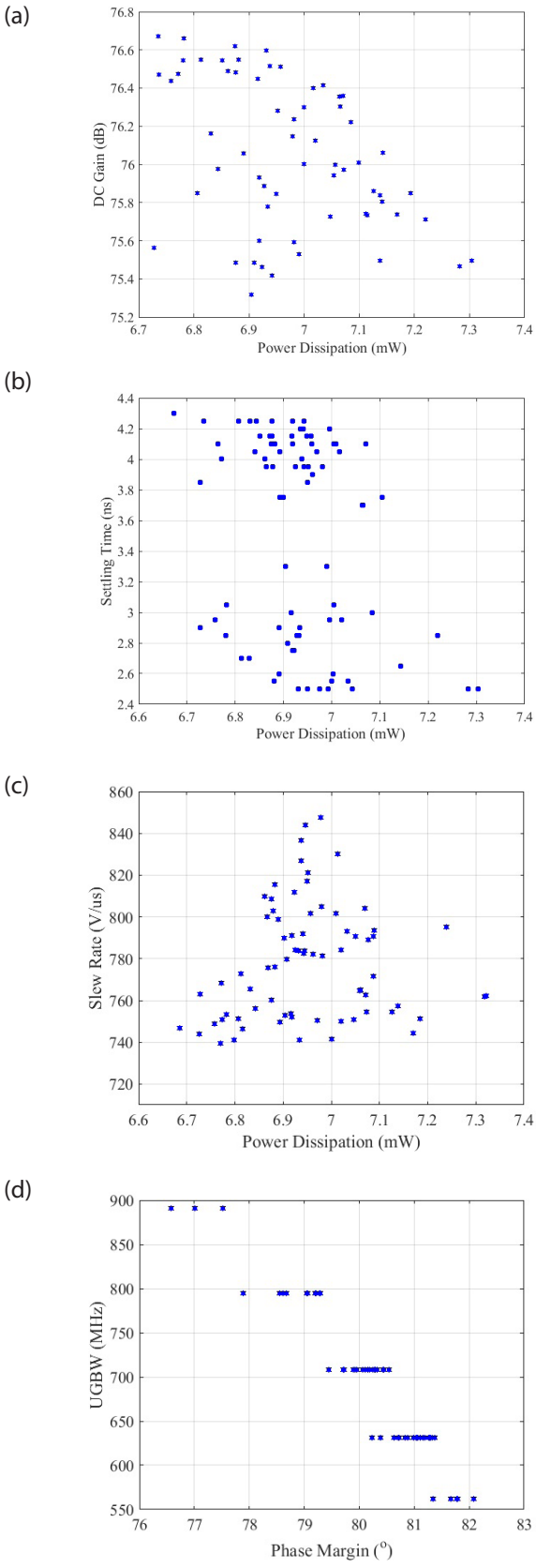


Figure 8: POFs of the three-stage: **(a)** ST versus P_{diss}, **(b)** DC-gain versus P_{diss}, **(c)** SR versus P_{diss}, **(d)** UGBW versus PM.

AB OTA including DC-Gain versus P_{diss}, SR versus P_{diss} and UGBW versus PM are shown in Figure 11. The results show that DC-Gain and UGBW reach 84 dB and 68 MHz, respectively. In addition, according to the PM values, the system is stable. Table 3 indicates the comparisons of post-layout simulation results of the proposed method with the existing methods for the two-stage class-AB OTA. Simulation results indicate that the proposed method outperforms the existing methods in terms of DC-gain, SR, layout area and area utilization.

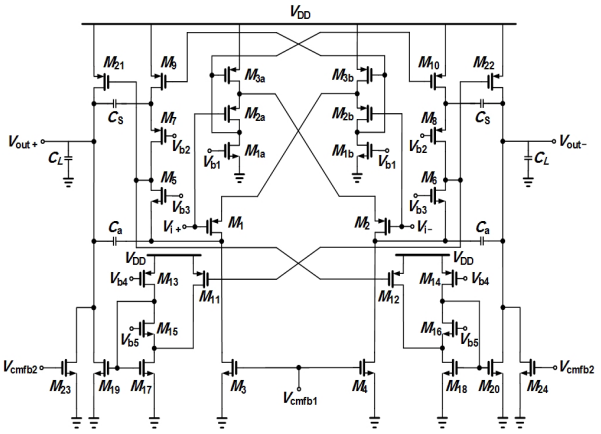


Figure 9: CMOS two-stage class-AB OTA [41].

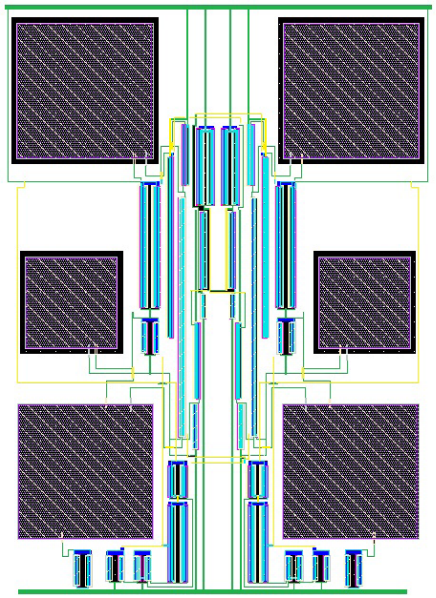


Figure 10: The two-stage class-AB OTA layout generated by the proposed method.

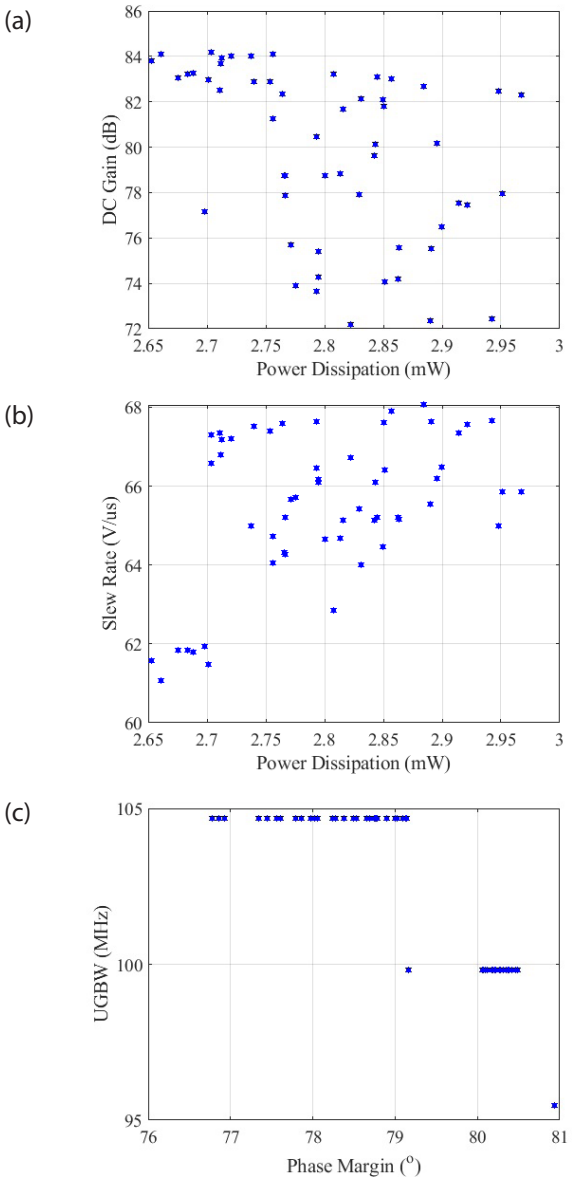


Figure 11: POFs of the two-stage class-AB OTA: (a) DC-gain versus P_{diss}, (b) SR versus P_{diss}, (c) UGBW versus PM.

Table 3: Comparisons of the post-layout simulation results for the two-stage class-AB OTA.

No.	Specifications	Post-layout performance		
		This work	[31]	[14]
1	DC-gain (dB)	84	80	76
2	Slew Rate V/µs	68	65	61
3	Total runtime (s)	2143	1785	1610
4	Layout Area (mm2)	0.025	0.027	0.028
5	Area Utilization (%)	89	84	78

5 Conclusions

A new automatic placement and routing method for layout generation of op-amps has been presented in this paper. In addition, the sizing has been performed automatically. Layout effects including parasitics and geometry effects have been considered. A compact floorplan has been generated in the placement stage by considering a set of constraints. A router has been suggested to generate wires automatically. MOEA/D has been utilized for optimization which is suitable for multi-objective optimization problems. In order to evaluate the performance of the proposed method, some simulations have been carried out and the results indicated the efficiency of the automatic analog layout generation method.

6 Conflicts of Interest

The authors declare no conflict of interest.

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