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Low Power CMOS Full Adder Cells based on Alternative Logic for High-Speed Arithmetic Applications

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Abstract: As the demand for computational capabilities continues to grow, the design and optimization of arithmetic circuits have more crucial in modern digital systems. The efficient operations of these arithmetic circuits heavily depend on the performance of fundamental modules such as Full Adders (FA). In addition to addressing typical challenges, designing full adder circuits using alternative logic offers unique advantages that are vital for the developing landscape of digital system. This paper presents two FAs based an alternative structures using modified Double Pass-Transistor Logic (DPL) for fast computing. The proposed Multiplexer based alternative structure differs from other conventional structures by concurrently generating both the carry signal and the sum signal, significantly reducing the overall propagation time. In addition to that multiplexers are controlled by external signals, the proposed structures provide full swing outputs. Also the modified DPL improves the signal integrity and noise immunity. The proposed circuits' performances were compared with other conventional logic and few hybrid adders. In comparison with other logics, various type of simulation results indicate that the proposed FA-2 exhibits improved performance in terms of average power, average delay, and average power-delay product (PDP). Our proposed FA-2 shows performance improvement over conventional CMOS for Power, Delay, and PDP, with values of 3.304%, 69.017%, and 74.602%, respectively. Full adders were simulated under different supply voltages and process corners to measure the reliability and robustness. Noise tolerances of full adder circuits were calculated using Average Noise Threshold Energy (ANTE) methodology.

Keywords: Full Adder, Alternative Logic, Multiplexer, Double Pass Transistor, Low Power

Celice CMOS z nizko porabo energije na osnovi alternativne logike za hitre aritmetične aplikacije

Izvleček: Ker povpraševanje po računskih zmogljivostih še naprej narašča, sta načrtovanje in optimizacija aritmetičnih vezij v sodobnih digitalnih sistemih vedno bolj pomembna. Učinkovito delovanje teh aritmetičnih vezij je močno odvisno od delovanja temeljnih modulov, kot so popolni seštevalniki (FA). Oblikovanje vezij polnih seštevalnikov z uporabo alternativne logike poleg reševanja tipičnih izzivov ponuja tudi edinstvene prednosti, ki so ključne za razvijajočo se okolje digitalnih sistemov. V tem članku sta predstavljena dva FA, ki temeljita na alternativnih strukturah z uporabo modificirane logike dvojnega prehoda in tranzistorja (DPL) za hitro računanje. Predlagana alternativna struktura, ki temelji na multipleksorju, se od drugih običajnih struktur razlikuje po tem, da hkrati generira tako prenosni signal kot celotni signal, kar znatno skrajša skupni čas širjenja. Poleg tega multiplekserje nadzorujejo zunanji signali, predlagane strukture pa zagotavljajo polne nihajne izhode. Prav tako spremenjeni DPL izboljša celovitost signala in odpornost proti šumu. Delovanje predlaganih vezij smo primerjali z drugimi konvencionalnimi logičnimi in hibridnimi seštevalniki. V primerjavi z drugimi logikami rezultati kažejo, da predlagani FA-2 izkazuje izboljšano zmogljivost v smislu povprečne moči, povprečne zakasnitve in povprečnega produkta moči in zakasnitve (PDP). Naš predlagani FA-2 kaže izboljšanje zmogljivosti v primerjavi s konvencionalnim CMOS za moč, zakasnitev in PDP z vrednostmi 3,304 %, 69,017 % in 74,602 %. Popolni seštevalniki so bili simulirani pod različnimi napajalnimi napetostmi in procesnimi koti, da bi izmerili zanesljivost in robustnost. Šumne tolerance polnih seštevalnikov so bile izračunane z uporabo metodologije ANTE (Average Noise Threshold Energy).

Ključne besede: popolni seštevalnik; alternativna logika; multiplekser; dvojni prehodni tranzistor; nizka poraba energije

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1 Introduction

The widespread usage of portable battery-operated electronic devices has made the adoption of VLSI circuits more important [1]. Present electronic hardware is designed for high performance operation. Energy efficiency and operating speed are considered as the important parameters for portability of any system. The increasing semiconductor market for portable devices demands for low-power building components to enable long-lasting battery-powered systems. Furthermore, the trend towards increasing circuit complexity and operating frequencies in high-performance applications necessitates the designing of high-speed circuit components [2]. Power dissipation in conventional CMOS (C-MOS) circuits is classified as Dynamic power dissipation ($P_{dynamic}$) and Static power dissipation (P_{static}). The main sources of power consumption are due to short circuit path, increased switching and various leakage currents. Short circuit power ($P_{short\text{-}dynamic}$) due to both p-channel and n-channel MOS transistors are active at the same time during transitions, Switching power $P_{switch\text{-}dynamic}$ is associated with charging/discharging at node/load capacitance and leakage power due reverse leakage current and sub-threshold currents. The total power dissipation (P_{Tot}) [3] can be expressed using equations 1 and 2.

$$P_{Tot} = P_{short\text{-}dynamic} + P_{switch\text{-}dynamic} + P_{static} \quad (1)$$

$$P_{Tot} = I_{sc} V_{dd} + \alpha C_L V_{dd} V_s f_{clk} + I_{static} V_{dd} \quad (2)$$

Among these, $P_{switch\text{-}dynamic}$ is treated as the major component for P_{Tot}. In above equation 2, I_{sc} indicates the short circuit current, C_L is the node/load parasitic capacitance, α denotes average number of switchings that have occurred in particular time period, V_s is the voltage swing (typically equivalent to V_{dd}), f_{clk} denotes clock frequency and I_{static} is the static current. PDP metric is always used to measure the energy expended in performing a specific action and serves as a vital performance parameter while evaluating optimization for a circuit component designed, implemented and tested under varying technologies, wide range of operating frequencies, and setups. Full adder cells are essential components in digital system design to perform binary addition, which is fundamental for performing arithmetic operations and data processing in digital circuits. Application Specific Integrated Circuits (ASIC), Microprocessors and DSP processors depends on efficient arithmetic cells for specific computations like convolution and advanced filtering [4]. Full Adder (FA) is widely used as one the main module to construct such arithmetic cells. Full Adder cell play a significant role in controlling the critical path of complicated arithmetic operations including, division, multiplication exponentiation, and more [5]. Moreover, in various data processing applications such as digital signal processing, cryptography, and data compression, full adder cells facilitate the computation and manipulation of binary data efficiently.

Despite their importance, full adder cells have several challenges in their design and implementation. Some of these challenges are achieving fast computation, minimizing power consumption, robustness for process variations, better noise tolerance, and optimizing area utilization in integrated circuits. So meeting these requirements are important for realizing the full adder cells to construct high-performance digital systems.

The integrated circuits (ICs) performance is limited by the effectiveness of arithmetic processes within the cell. The choice of circuits for implementing adder cells depends on various performance metrics. Different ways of designing logic tend to focus on one aspect of performance but may neglect the other. The PDP of the FA cell impacts the complete system performance. Considering this, designing an energy efficient FA cell with minimal propagation delay has become crucial for modern digital systems [2].

Improving performance according to Moore's law requires more than just advancing fabrication technology; it also involves focusing on other factors, particularly implementing a suitable circuit design [6]. Various logic styles and techniques have been developed for arithmetic cells, which reduce the total cost and improving the whole performance of ICs. Minimizing the V_{dd} is a prominent approach for decreasing power consumption; however it results in slower circuit's speed and reduces the driving capacity of circuits. Many static logic styles such as pass transistor logic (PTL) and C-CMOS logic structures are play a vital role in constructing the low power FA cells. The C-CMOS FA cell structures are more robust, and it facilitates transistor sizing which allows scaling of different voltages to guarantee the proper functionality [7].

Many investigations have been published on optimizing low-power and high speed full-adders. These papers explore various conventional logic styles, such as C-CMOS [8], CMOS Transmission Gate (CMOS TG) [9], Pseudo nMOS [10], PTL [11], Cascode Voltage Switch Logic (CVSL) [12], Complementary PTL (CPL) [13], Differential Cascode Voltage Switch Logic (DCVL)[14], DCVL with the pass-gate tree (DCVSPG)[13], Double Pass transistor logic style (DPL) [15], Swing-Restored PTL (SRPL) [16], Swing-Restored CPL (SR-CPL)[17], Energy Economized PTL (EEPL) [18], and as well as different logic structures for building the adder module.

In recent days, researchers focus on the hybrid design approach that incorporates features from multiple logic styles. Yingtao et al. [19] introduced a 12-transistor low power hybrid FA cell using MUX logic and it is capable of reduced switching activity, charge recycling capability along with reduced short circuit power consumption. Pankaj et al. [20] proposed a novel FA cell by modifying the internal logic structure and this circuit is significantly reducing the PDP.

Naseri et al [21] introduced 6 low power hybrid FA cells by altering the EXOR/EXNOR logic gate stricture for high-speed applications. The novel structures overcome the drawbacks of conventional logic by removing the inverter logic in the critical path. Also it replacing the positive feedback at the output terminal. Mehedi et al. [22] proposed a hybrid Full Adder for full voltage swing using a scalable XOR-XNOR block designed for large word-length architectures. They highlighted that many FA cells performing well as 1-bit adder but extending them for wide word length is more difficult. Jyoti et al. [23] recommended a high-speed 20-transistor hybrid FA (HFA) structure using three distinct elements for arithmetic applications.

Sharmila et al. [24] proposed a novel FA cell based on reversible logic. They conveyed that proposed FA cell more useful in designing the current-mode logic circuits. Authors highlighted that information retention and inverse computation are feasible in reversible logic. So that in recent years' researchers prefers reversible logic for low-power VLSI circuit design. Azeem et. al [25] introduced a high performance 14-T HFA using PTL and GDI logic for arithmetic applications. They pointed out that hybrid styles are most preferable for implementing FA cell in recent years. Rahimi et. al [26] introduced a high performance 9-Transistors Full Adder cell based on pseudo dynamic logic for low power arithmetic applications. Since the circuit has reduced number of internal nodes which are connected with ground, it is more energy efficient than C-CMOS, CMOS TG, PTL and DPL.

The objective of this research is to combine the benefits of multiple logic designs to construct the hybrid FA cell. The proposed hybrid methods can leverage the strengths of each logic design technique while mitigating their respective limitations. This integration can improve the FA cell's performance in terms of speed, power efficiency, and noise tolerance compare to other conventional structures.

2 Full adder using alternative logic

The alternative style full adder cell gives a different approach compared to the conventional full adder circuits. This alternative logic structure employs a unique internal logic using the multiplexers. The Boolean functions $A+B$, $A.B$, $A\oplus B$ and $\overline{A\oplus B}$ are selected from the two distinct multiplexers to produce the output signals. Such designs are aims to achieve the delay balance between the Sum and Carry signals. Furthermore, PTL are the powerless/groundless logic structures and they are used to build power efficient full adder cell using alternative logic. The focus on optimizing power consumption and reducing propagation delays discriminates this alternative full adder logic cell. This differentiation makes it a potential improvement over other conventional designs for building low-power arithmetic circuits

Aguirre [27] proposed an Alternate Full Adder cell using Multiplexer for High Speed Application is illustrated in Figure 1. This structure comprises of three distinct modules. The Block 1 generates the logic output of $A+B$, $A.B$, $A\oplus B$ and $\overline{A\oplus B}$ simultaneously. So it apparently lessens the propagation delay of Carry signal present in the conventional full adder logic. Block 2 and Block 3 are the two independent 2X1 multiplexers evaluate the Sum(S_0) and Carry(C_0) from the outputs obtained from Block 1. Unlike Conventional Full Adder circuit, the alternative full adder cell evaluates the Sum(S_0) and Carry(C_0) outputs with relatively equal propagation delay.

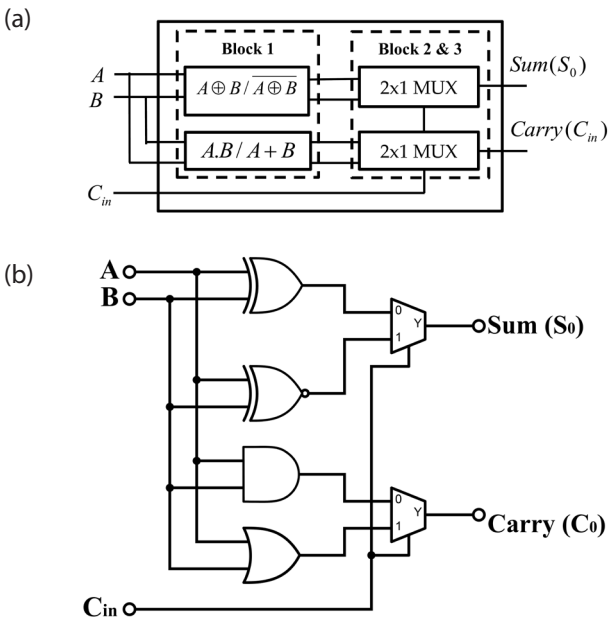


Figure 1: (a&b) : Full Adder Structure using Multiplexer based Alternative Logic

Referring to the FA functionality from the Table 1, we can observe that Sum (S_0) signal is chosen from logic values $A\oplus B$ and $\overline{A\oplus B}$ with the help of third input C_i. When C_i=0, multiplexer-1 will chose $A\oplus B$ logic value

and C_i=1, multiplexer-1 will chose $\overline{A \oplus B}$ logic value for Sum (S_0).

Table 1: 1-bit Full adder circuit logic table

Inputs			Block 1 Outputs				Outputs	
A	B	Ci	A XOR B	A XNOR B	A.B	A+B	Block 2 Sum (S0)	Block 3 Carry (C0)
0	0	0	0	1	0	0	0	0
0	0	1	0	1	0	0	1	0
0	1	0	1	0	0	1	1	0
0	1	1	1	0	0	1	0	1
1	0	0	1	0	0	1	1	0
1	0	1	1	0	0	1	0	1
1	1	0	0	1	1	1	0	1
1	1	1	0	1	1	1	1	1

Similarly, the multiplexer-2 chose one of the output from *A.B* or *A+B* logic for the Carry(C_0) based on the third input C_i. In both Sum (S_0) and Carry(C_0) generation cases, third input C_i will be act as control signal for the multiplexers 1 & 2. Selecting the sum and carry from Multiplexer simultaneously will significantly reduce the overall propagation delay. So alternative full adder structures are widely used to construct the high speed datapath circuits. The alternative logic configuration has the following features.

- The signals internally generated are not utilized to control the output of the multiplexer. Alternatively, the third input signal 'C_i' controls the mux output and produces maximum voltage swing without any additional delay. This apparently lessens the total propagation delay of the FA circuit.
- In submicron fabrication technologies, diffusion capacitances of source/drain terminals act as an important role. In alternative logic, C_i is connected only with few transistors Gate terminal and it is not connected with any of the source/drain of the transistors. This configuration significantly reduces the load capacitance of the C_i input. Therefore critical path propagation time for C_i is minimized. So large module's overall propagation delay can be reduced.
- The outputs signal's (S_0 and C_0) propagation delay could be varied by adjusting size of the logic gates (XOR/XNOR and AND/OR) separately present in the Block 1. This characteristic is beneficial in scenarios where the skew between incoming signals is critical, such as in wave pipelining. Additionally, it helps to maintain propagation delay balancing at the output port. It reduces the risk of glitches in cascaded structures.

3 Hybrid full adders using modified DPL

As the technology moving into sub-micron level, many novel circuit styles and structures were introduced recently to overcome the limitations of the C-CMOS logics. PTL is a fundamental digital circuit style, depends on MOS transistors as pass gates to implement logical functions. PTL circuits are designed by either NMOS or PMOS transistor. This difference from the C-CMOS design, which uses both NMOS and PMOS transistors, makes PTL simpler and potentially better. But the choice is typically based on the technology process and optimization goals. Usually the PTL circuits are constructed by connecting the pass gates to obtain complex logic functions. Multiplexers, demultiplexers, flip-flops, and other digital circuit's modules can be implemented using pass transistor configurations. PTL has gained attraction due to its low power consumption, and ability to operate at high speeds.

Even though PTL circuits are simpler than other conventional styles, it is also have some challenges in implementation. Signal degradation due to the resistance introduced by the pass switches is recognized as one of the main issue faced by PTL. As signals pass through multiple stages of pass gates, the total resistance can lead to a significant reduction in signal levels. Threshold drop is another concern present in the PTL circuits. The voltage drop caused the each pass transistor can influence change in the logical threshold levels. While the voltage drop isn't a big problem in nMOS logic, it can cause issues in CMOS by making both p and n transistors conduct simultaneously. This incident seriously affects the circuit's noise margin and overall reliability. Always pairing the nMOS transistor with a pMOS is a complex solution to achieve the necessary full swing in output voltage. Figure 2 depicts the EX-OR gate

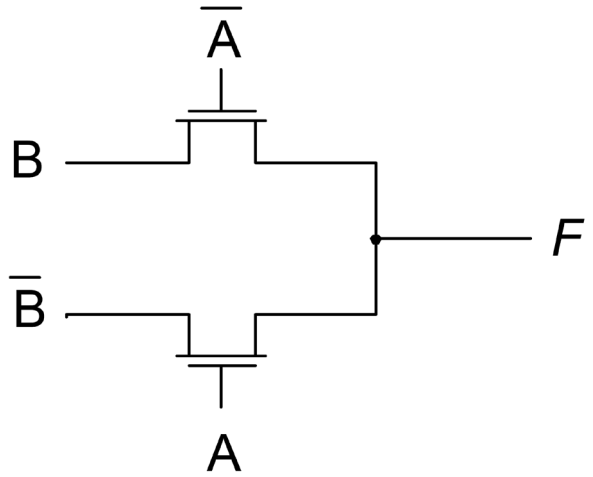


Figure 2: EX-OR Logic Gate implementation using PTL

($F = A'.B + A.B' = A \oplus B$) implementation through NMOS pass transistor logic. Figure 3 depicts the Threshold drop at the output terminal of the PTL gate.

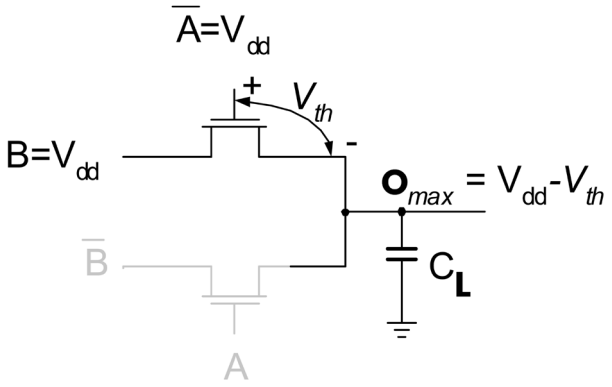


Figure 3: Threshold drop at output of the pass-transistor gate

The introduction of new CMOS logic families, such as CPL and DPL using pass-transistor circuits, aimed to improve both speed and power efficiency. Employing CPL in Digital circuit design not only resulted in an efficient implementation but also fast logic operation due to higher logic functionality and lower input capacitance. However, lower supply voltage CPL implementation, it is essential to consider the challenges posed by speed degradation and noise margin. These issues are arising due to discrepancy between logic threshold voltage and fluctuation of input signal levels caused by process variations. Also, CPL facing the threshold voltage drop problem while the signal passing via series of pass-transistors and its voltage was lessened by one V_T (threshold voltage drop). In the modern CPL versions, the "threshold drop" issue is addressed by using a special inverter that could restore the signal amplitude to its maximum potential. Since the signal restoration in CPL is not depending on the load present at the output port, signal restoration is done quickly during the signal transition with less amount of power.

DPL is another modified CPL style designed to fulfill the drawbacks of CPL in reduced supply voltage configurations. DPL was initially developed to address the 'threshold drop' issues in CPL and provide an alternative style to PTL. It is implemented with dual-stage architecture, using both NMOS and PMOS transistors in parallel for each pass gate, effectively eliminating the 'threshold drop.' Therefore, there is no need for level-restoring inverters after each logic block, improves speed of DPL. As mentioned previously, DPL gates improve the overall circuit performance at lower supply voltages by employing the both nMOS and PMOS transistors. Due to the symmetrical structure of DPL, load at the input side is equally distributed between all the inputs. The XOR/XNOR gates designed by DPL exhibits perfect symmetry. With the help of dual transmission property and symmetrical arrangement, the DPL works effectively in wave pipelined circuits [28]. In DPL, dual current path is created due to the structure of the parallelly connected NMOS transistors and PMOS transistors for each input signal's combinations and produces very small equivalent resistance compared with other conventional logic structures.

As reported by Uming Ko et al. [29], DPL was the highly energy-efficient logic methodology compared to other discussed logics. DPL can more effectively tackle challenges such as signal degradation and threshold drop, resulting in improved signal integrity and driving capability. DPL is well-suited for applications requiring improved signal integrity, minimal signal degradation, and better driving capability. Its dual-stage architecture makes it advantageous for high-speed digital circuits, memory cells, arithmetic units, and other scenarios where noise margins are more critical. Though DPL has many advantages, it is facing certain drawbacks such as Complexity and Area Overhead due to dual-stage architecture. Figure 4 depicts the AND and NAND Logic Gates using DPL. In this paper, we proposed two FA cells built using alternative structure by DPL to enhance noise margins, increase the operating speed and decrease power dissipation.

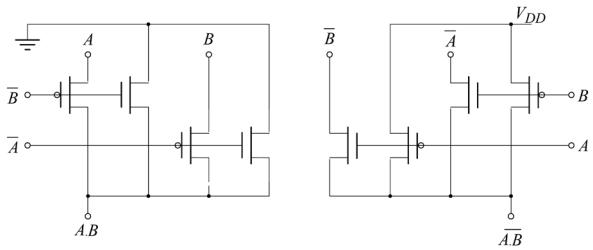


Figure 4: AND and NAND Logic Gates using DPL

Figure 5 shows the Proposed Full Adder 1 based on alternative logic using DPL. The Full Adder circuit is realized through the Alternative logic structure using DPL. In this structure, $A \oplus B$ and $\overline{A \oplus B}$ were obtained through two DPL circuits. For example, $F = A'.B + A.B' = A \oplus B$ and $A'.B / A.B'$ is obtained through both NMOS and PMOS which ensures Good Logic 1/0 is delivered through the pass switch. Similarly, all the sum of product terms for $A \oplus B$ and $\overline{A \oplus B}$ were obtained in the first stage through both NMOS and PMOS transistor to get the better voltage swing. Since $A \oplus B$ and $\overline{A \oplus B}$ were generated in parallel, there is negligible delay difference between them. Unlike CPL, $A \oplus B$ and $\overline{A \oplus B}$ operate at full swing levels, and there is no need for swing restoration logic at the $A \oplus B$ and $\overline{A \oplus B}$ nodes.

The subsequent stage is the two parallel 2x1 multiplexers obtained through alternative logic. Sum and Carry of the FA circuit is generated by those multiplexers with almost equal propagation delay.

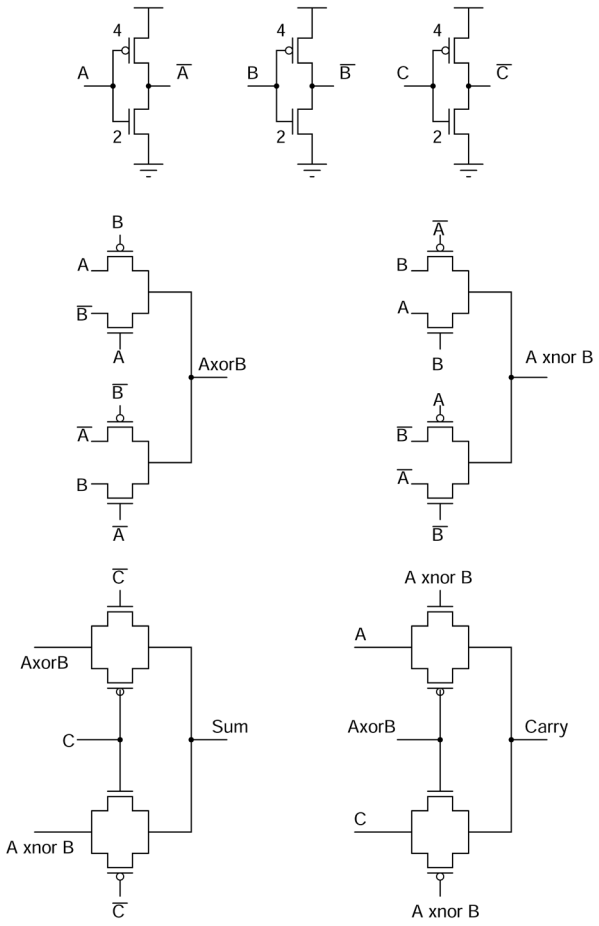


Figure 5: Proposed alternative logic based Full Adder 1 using DPL

In the Sum structure the multiplexer is controlled by the third input C which is not an internally generated signal. So that it can produce full voltage swing output at the Sum terminal with less propagation delay. At the same time, the Carry signal is produced by second multiplexer where either $A \oplus B$ and $\overline{A \oplus B}$ will act as control signal to select the input. Since $A \oplus B$ and $\overline{A \oplus B}$ are internally generated by the circuits, the Carry signal has slightly smaller voltage swing than Sum signal with small amount of additional delay. The second proposed circuit will overcome this issue by not using the internally generated signals for controlling the multiplexers.

Figure 6 shows the Proposed Hybrid Full Adder 2 based on alternative logic using DPL based on alternative logic using DPL. In the first stage, logical values $A \oplus B$ and $\overline{A \oplus B}$ are obtained using DPL and like similar way and

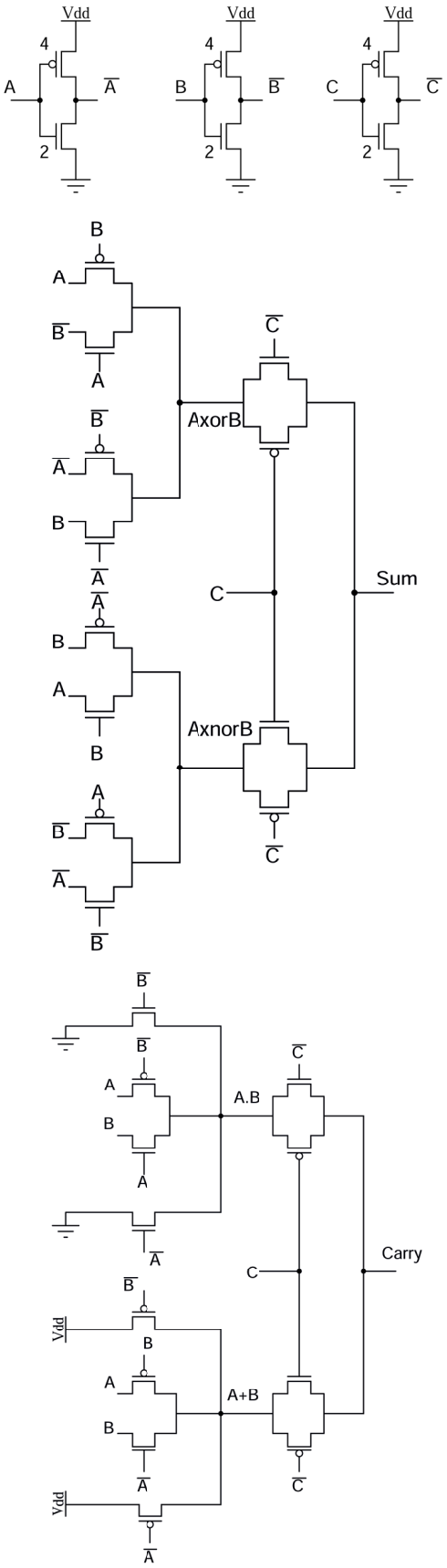


Figure 6: Proposed Hybrid Full Adder 2 based on alternative logic using DPL

obtained through modified DPL. Similar to proposed FA 1, the second proposed adder also generates all the sum of product terms in parallel with full voltage swing.

Since $A \oplus B$, $\overline{A \oplus B}$, $A + B$ and $A.B$ outputs obtained in parallel manner, there is no significant propagation delay difference among them. Also, they are generated the through DPL, signal restoration is not required. In the $A.B$ and $A + B$ network, we have included two additional NMOS/PMOS transistors in which connections of their source terminals with either ground/V_{dd} supply to enable quick discharging/charging of the node. The second stage is the two parallel multiplexers similar to proposed FA 1. But here the Sum and Carry multiplexers are controlled by third input signal rather than internally generated signal. So the Sum and Carry output will be at full voltage swing without any additional delay.

4 Simulation environment, results and discussions

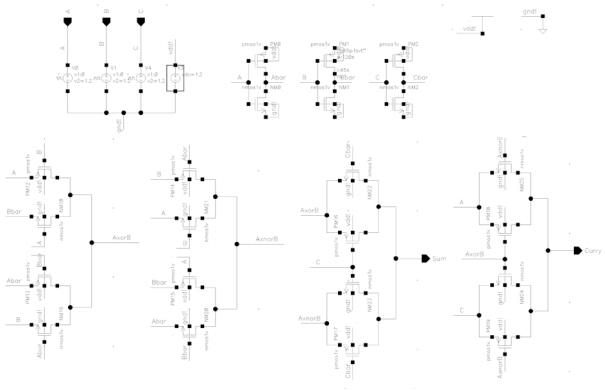


Figure 7: Proposed FA Cell 1 schematic design

Figure 7 and Figure 8 show the proposed full adders schematics designed in cadence virtuoso schematic editor. Figure 9 and Figure 10 depict the transient analysis waveforms of the proposed Full Adders obtained by using Analog Design Environment L tool. Figure 11 and Figure 12 show the layouts obtained through Cadence Layout XL tool for the proposed Full Adder Cells. Table 2 illustrates the comparison results of Min and Max delay, Average delay, Power, PDP, transistor count and area requirement for each FA cell using several conventional and novel full adder styles discussed in our literature namelyC-CMOS [8], CMOS TG [9], Pseudo nMOS [10], PTL [11], , CVSL [12], CPL [13], DCVL [14], DCVSPG [13], , DPL [15], SRPL [16], SR-CPL [17], EEPL [18], Naseri (HFA-22T) [21], Mehedi [22], Jyoti [23], Sharmila [24], Azeem [25], Rahimi [26], Proposed Logic 1 and Proposed Logic 2. Since proposed full adders are designed using DPL

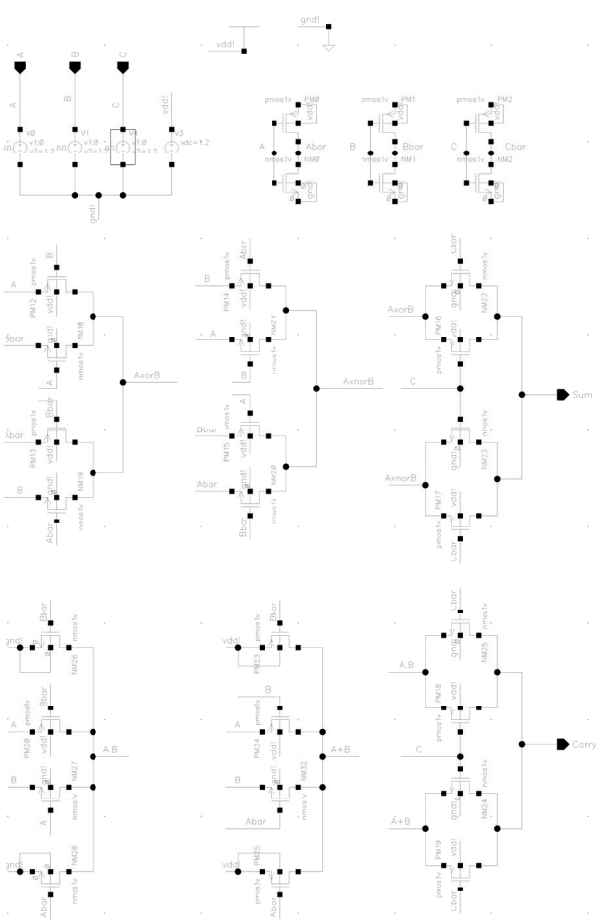


Figure 8: Proposed Full Adder 2 schematic design

and they ensure the full voltage swing output in all the conditions. In the proposed full adder 1 carry signal is produced by internally generated signals, the voltage swing for carry is little lower than the carry signal produced by proposed full adder 2. Additional inclusion of transistors in the $A \oplus B$, $\overline{A \oplus B}$, A+B and A.B logic modules significantly reduces the switching time by quickly charge/discharge the internal nodes. The fast switchings make the proposed circuits better suited for constructing arithmetic circuits and DSP processors etc. for real-time applications.

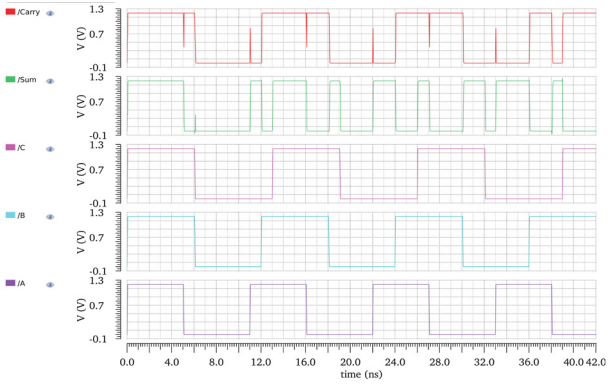


Figure 9: Proposed FA 1 Transient Analysis waveform

From the Table 2, we observed that average delay of proposed logic 2 is 165.81ps and it is smaller than all other logics. Rahimi [26] and Mehedi [22] full adder cells average delay are 172.62ps and 173.37ps respectively. In power dissipation part, EEPL consumes 323.05µW power and it is the lower than all other logics. Our proposed logic 2 and Naseri (HFA-22T) [21] consumes average power of 350.82µW and 355.94 µW respectively. While considering the PDP, proposed full adder 2 has 0.0582pJ and followed by Mehedi [22] and Rahimi [26].

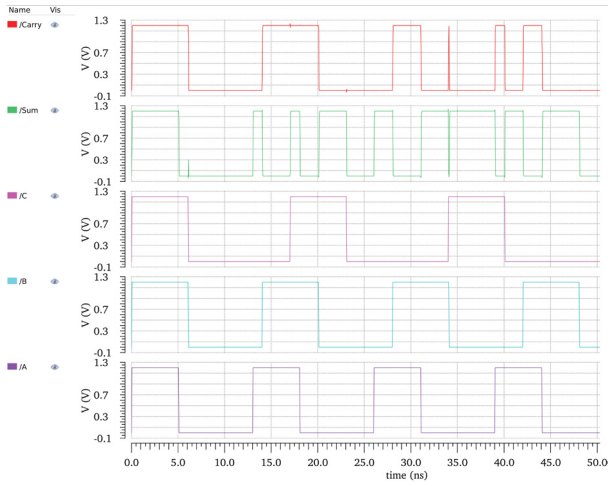


Figure 10: Proposed FA 2 Transient Analysis waveform

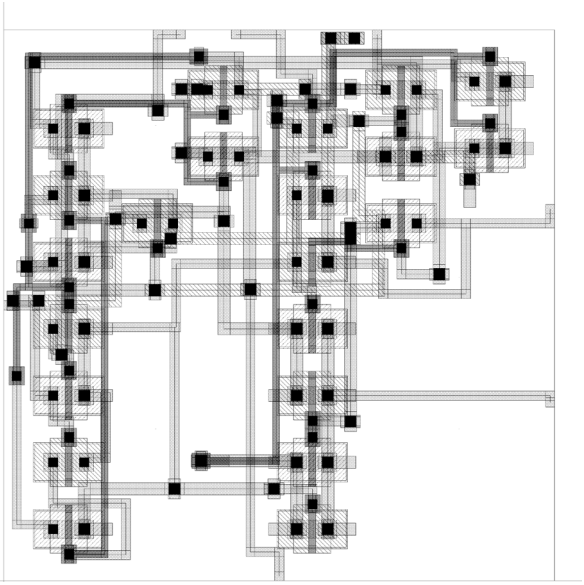


Figure 11: Proposed Full Adder 1 Layout

From previous literatures we observed that, mux based alternative structures and DPL significantly reduces the propagation delay. Also DPL consumes lesser power compared to other conventional logic, due to reduced switching activity. Observed results from Table 2 shows that our proposed logics based on Multiplexer and DPL significantly reduces the power and propagation delay.

Table 2: Comparison of simulation results of various FA cells in 45nm technology

S. No.	Name of the FA Cell	Delay (ps)			Avg. Power (µW)	Avg. PDP (pJ)	Transistors Count	Area (µm²)
		Avg. Delay	Maximum Delay	Minimum Delay				
1	Conventional CMOS	280.25	341.35	227.99	362.41	0.1016	28	18.85
2	CMOS TG	321.09	410.38	268.16	394.36	0.1266	16	11.63
3	Pseudo nMOS	332.95	434.29	307.86	476.27	0.1586	18	13.54
4	12-Transistor	289.55	366.38	245.22	395.62	0.1146	12	8.08
5	PTL	256.09	319.58	225.00	412.27	0.1056	16	11.17
6	CPL	294.97	381.92	249.80	408.56	0.1205	32	20.25
7	SR-PL	271.71	334.36	223.80	372.03	0.1011	28	18.86
8	SR-CPL	244.772	280.92	186.98	338.79	0.0829	26	16.33
9	DPL	198.00	264.68	174.18	378.23	0.0749	48	30.63
10	CVSL	245.10	315.24	216.51	395.07	0.0968	27	17.70
11	DCVL	228.28	296.29	197.42	380.48	0.0869	30	20.46
12	DCVSPG	214.85	276.04	178.97	366.96	0.0788	28	18.71
13	EEPL	352.12	448.03	292.12	323.05	0.1138	32	20.81
14	Naseri (HFA-22T) [21]	188.69	237.92	159.35	355.94	0.0672	22	14.32
15	Mehedi [22]	173.37	220.14	144.25	369.623	0.0641	22	13.68
16	Jyoti [23]	199.68	249.22	166.18	365.67	0.0730	20	13.85
17	Sharmila [24]	221.65	280.32	186.80	399.12	0.0885	27	17.57
18	Azeem [25]	208.15	258.34	173.33	396.05	0.0824	14	9.04
19	Rahimi [26]	172.62	216.91	144.63	373.49	0.0645	9	5.59
20	Proposed Logic 1	176.51	217.04	145.38	384.39	0.0678	22	14.04
21	Proposed Logic 2	165.81	204.00	136.56	350.82	0.0582	30	20.19

The lower PDP of the proposed full adder 2 more useful in constructing the energy efficient high speed circuits for portable devices. Figure 14 and Figure 15 show the graphical comparison of Average value of Delay, Power and PDP for the various full adder cells.

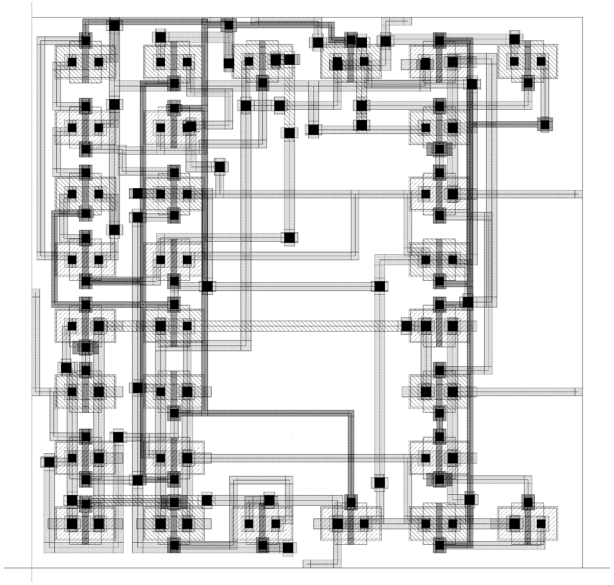


Figure 12: Proposed Full Adder 2 Layout

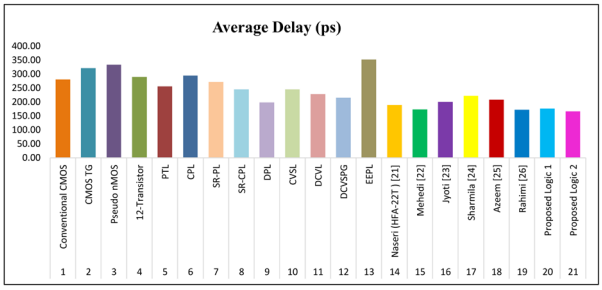


Figure 13: Average Delay Comparison of Various FA cells

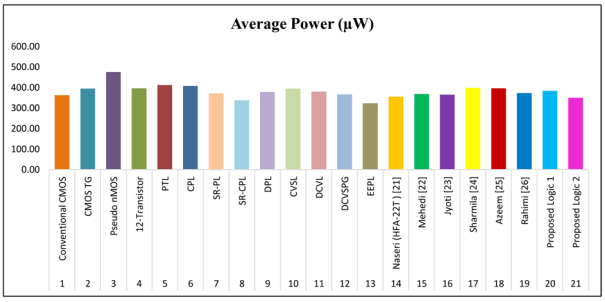


Figure 14: Average Power Comparison of Various FA cells

Table 3: Proposed FA 2 performance improvements with other logics

Sl. No.	Name of the FA Cell	% of Improvement for Proposed Logic 2			
		Avg. Delay	Avg. Power	Avg. PDP	Area
1	Conventional CMOS	69.017	3.304	74.602	-6.667
2	CMOS TG	93.644	12.410	117.677	-42.381
3	Pseudo nMOS	100.797	35.760	172.602	-32.929
4	12-Transistor	74.626	12.769	96.924	-59.964
5	PTL	54.445	17.517	81.500	-44.667
6	CPL	77.891	16.459	107.171	0.286
7	SR-PL	63.866	6.045	73.771	-6.583
8	SR-CPL	47.620	-3.430	42.556	-19.137
9	DPL	19.414	7.812	28.742	51.714
10	CVSL	47.820	12.615	66.467	-12.330
11	DCVL	37.671	8.455	49.312	1.339
12	DCVSPG	29.571	4.601	35.532	-7.333
13	EEPL	112.363	-7.916	95.553	3.048
14	Naseri (HFA-22T) [21]	13.797	1.459	15.456	-29.089
15	Mehedi [22]	4.555	5.360	10.159	-32.232
16	Jyoti [23]	20.426	4.234	25.525	-31.429
17	Sharmila [24]	33.674	13.767	52.076	-12.973
18	Azeem [25]	25.532	12.892	41.715	-55.208
19	Rahimi [26]	4.106	6.463	10.834	-72.298
20	Proposed Logic 1	6.453	9.569	16.640	-30.464

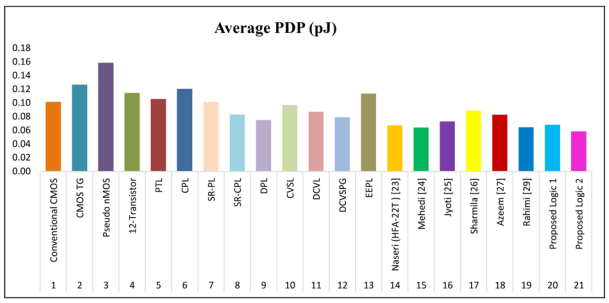
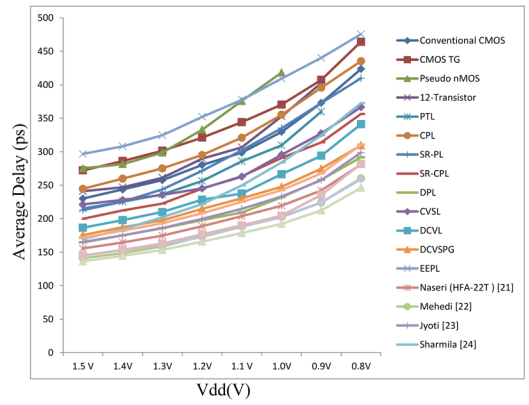
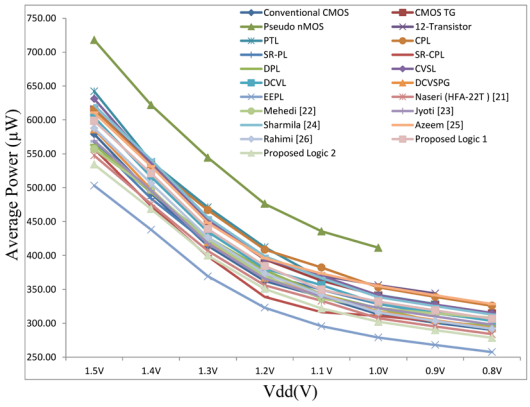


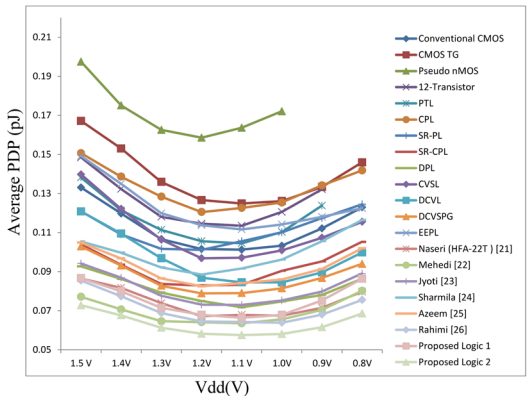
Figure 15: Average PDP Comparison of Various FA cells



(a) Delay



(b) Power



(c) PDP

Figure 16: FA Cells simulation results for different V_{DD} levels

Table 3 shows the proposed full adder cells performance improvement in various parameters. Since proposed full adder 2 is constructed with 30 transistors, the area requirement is significantly more than other logics. While comparing with other parameters, the proposed FA cell 2 is superior to other logics. The full adder cells efficiency and robustness can be analysed by varying the bias voltage (V_{DD}). To perform this, bias voltage is adjusted from 1.8V to 0.8V with 45nm CMOS technology and transient outputs were analysed.

Other than Pseudo nMOS, 12-Transistor and PTL, all the full adders are producing correct output in this range. Pseudo nMOS producing correct output up to 1V and 12-Transistor and PTL are producing correct output up to 0.9V. Our proposed full adders 1 and 2 are producing the output without any signal degradation upto 0.9V supply voltage and small degradation present in the 0.8V supply voltage.

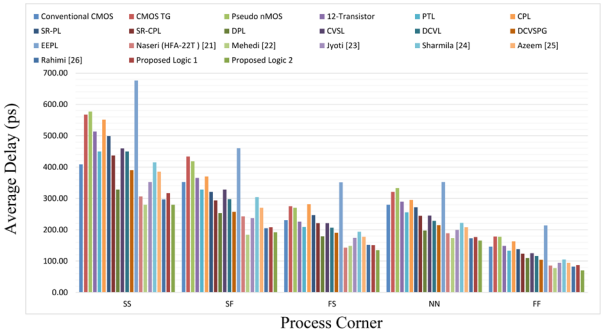
In this paper, we analysed average value of power, delay and PDP of all the FA cells by varying the supply voltage. Figure 16 illustrates the FA Cells simulation results for different V_{DD} levels. From the figures, we can understand that as the V_{DD} decreases, the propagation delay increases, and power dissipation decreases. However, the PDP value initially decreases, and after reaching the voltage level of 1.2 to 1.1, it begins to increase.

Experimental observations showed that proposed full adder 2 along with Mehedi [22] and Rahimi [26] full adders PDP values are almost equal for the V_{DD} ranging from 1.0V to 1.3 V which makes these full adders suitable for operating at wide range of power supply values. Also it is observed that lessening V_{DD} causes the drop in power consumption and rise in propagation delay. The PDP value is decreased while reducing supply voltage (V_{DD}) up to 1.1 V to 1.0V range and then it is begins to increase.

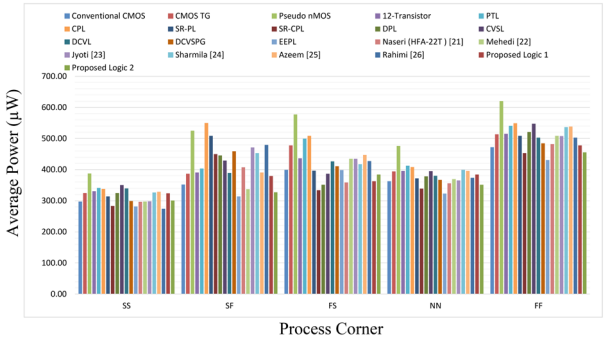
In the field of IC design, the attention to process corners holds significant importance as it allows designers to assess the reliability and robustness of the designed circuits under diverse manufacturing conditions. By Investigating various Process Corners will help to identify the key challenges associated with vital performance parameters such as Speed, Power Consumption, and etc. This analysis assures that the proposed design meets required specifications under the influence of different operating conditions. Nominal - Nominal (NN) or Typical - Typical (TT), Slow – Slow (SS), Fast - Slow (FS), Slow - Fast (SF) and Fast - Fast (FF) are the process corners present to analyse the circuits. In Cadence ADE, various Process Corners were chosen, and simulations were carried out to determine the Average Delay, Power, and Power-Delay Product. These simulations were

performed to determine the circuit's feasibility under various environments. Figure 17 depicts the performance of FA cells for different process corners. In the FF process corner setup, all the FA cells operate with minimal delay and consume more power. Alternatively, in the SS process corner setup, FA cells operate with increased propagation delay and lower power. Proposed Full adder 2 achieved lowest PDP of 0.0321pJ and 0.0582pJ in FF and TT corners. Naseri (HFA-22T) [21] achieved minimum PDP 0.051129pJ in FS process corner. Mehedi [22] full adder achieved 0.0621pJ in SF process corner. Rahimi [26] full adder achieved 0.0815pJ in SS process corner.

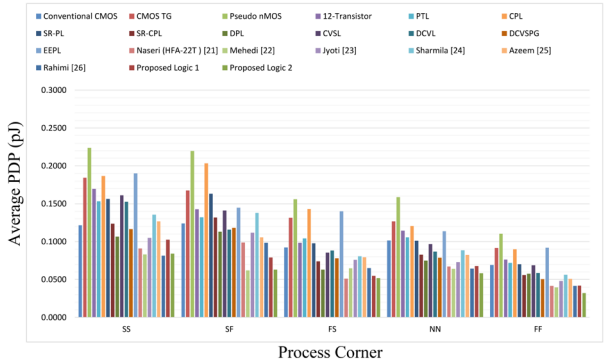
Noise tolerance is an imperative property for any integrated circuits to ensure reliable operation, maintain signal integrity, and prevent performance degradation due to various external factors. Designing any ICs with strong noise tolerance is the key factor to the overall success and correct functionality of electronic devices. Noise tolerance parameter will help to evaluate the ability of digital circuits to withstand to the influences of the noise signal. Both CPL and DPL offer better noise immunity compared to other logics. Differential operations due to Complementary pairs of Pass Transistors present in the CPL provide inherent noise immunity. DPL further improves the noise immunity by double passing of signals. This means that signals pass through the gates twice (i.e same logic implemented by two different logic gates), effectively amplifying the signal and minimizing the impact of noise.



(a) Delay



(b) Power



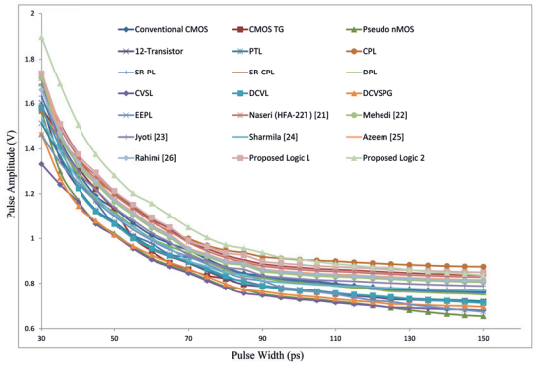
(c) PDP

Figure 17: Various Process Corners vs Delay, Power and PDP

Noise pulses with high amplitude and significantly large width in ICs may create unwanted switching, potentially causing the circuit to malfunction. In this article, Katopis [30] Noise Immunity Curve (NIC) was obtained to evaluate the noise tolerance of different Full adder circuits in response to noise input. A logical error will occur at the locus point (T_n, V_n) for the gate, where T_n represents the noise pulse duration and V_n represents the noise pulse's amplitude.

Average Noise Threshold Energy (ANTE) metric [31] is the quantitative value of noise tolerance and it is computed from the NIC.

(a)



(b)

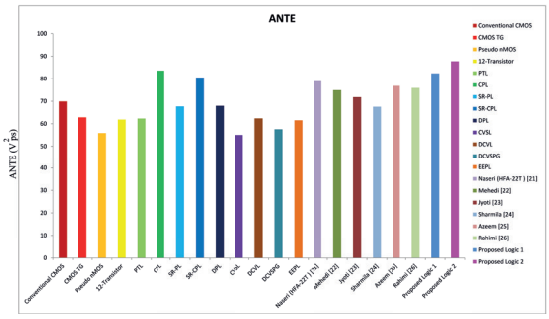


Figure 18: (a) NIC for various FA Cells (b) ANTE for various FA Cells

$$ANTE = E(V_n^2.T_n) \quad (3)$$

$$ANTE = (V_1^2.T_1 + V_2^2.T_2 + ...V_n^2.T_n)/n \quad (4)$$

Figure 18 shows that NIC plot and ANTE for full adder circuits discussed in this paper. The higher ANTE value represents that the circuit has better Noise immunity. The proposed full adder 2 and full adder 1 have the ANTE value of 87.72 and 82.32. As we discussed earlier, the our DPL based logics have better noise immunity than other logics.

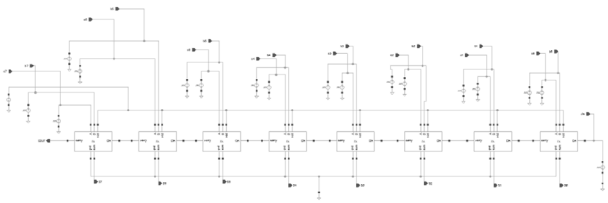


Figure 19: 8 bit Parallel Adder using proposed full adder 2

The functionality verification of our proposed full adder 2 for higher order bits is done by designing a 8-bit parallel adder (Ripple Carry Adder). Figure 19 shows that the 8-bit parallel adder implementation using cadence virtuoso schematic editor. The 8-RCA has average delay, power and PDP of 1485.68ps, 3690.618µW and 0.589613pJ.

5 Conclusion

In this paper, two novel full adder structures based alternative logic using double pass transistor have been proposed. The alternative logic is implemented by separate XOR/XNOR structure to increase speed of the circuit. Our proposed Full Adder cells performances are compared with 19 various conventional adders including C-CMOS, CMOS TG, PTL and recently reported hybrid full adders. The various simulations were performed by Cadence EDA tools with 45nm CMOS technology. The proposed FA Cell 2 has minimum of 10.16% improvement with respect to PDP value. The average delay of the proposed full adder 2 is minimal than all other logics and the average power of the proposed full adder 2 is superior to that of all other logics, except for EEPL. All the FA cells were simulated under different supply voltage ranges from 0.8V to 1.5V and our proposed full adders performed well in those conditions. Simulations were conducted in various process corners and our proposed full adder 2 shows highest performance with respect to PDP in NN and FF process corners. In other process corners, both the full adders have lower PDP value than most of the logics. The noise immunity of circuits is measured using NIC and ANTE and our proposed full adder 2 has highest ANTE value. Also both the full adders are less susceptible to noise when simulated by a noise pulse width 150ps and below. Our proposed designs offer practical insights into improve the circuit performance in developing the modern electronic systems. Also they pave the way for the realizing faster and energy-efficient computing structures in various domains such as digital signal processing, communication systems, and embedded computing. Additionally, the robust performance of our FA cell across different supply voltages and process corners ensures their suitability for diverse applications in both high-performance computing and low-power embedded systems. Further investigation can be done by exploring various optimization techniques to improve the performance and efficiency of the proposed full adders. Also, investigating full adder cells compatibility for emerging semiconductor technologies, such as advanced CMOS nodes or alternative materials, may provide the insights for future computing systems.

6 Conflict of Interest

The authors declare no conflict of interest.

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