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Analog Circuits Sizing Using Multi-Objective Evolutionary Algorithm Based on Decomposition

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Abstract: Several analog circuit design has been suggested where a layout generator is used after a circuit sizing. But, many iterations between circuit sizing and layout generator stages are needed to obtain desired specifications. This paper proposes a new equation and simulation-based method for circuits sizing of CMOS operational amplifiers (op-amps) by considering layout effects. In the proposed method, layout effects are considered during the sizing step. Layout effects are devices parasitics and geometry information that are extracted from a new automated layout generator. Optimization is performed using multi-objective evolutionary algorithm based on decomposition (MOEA/D). In order to evaluate the performance of the proposed sizing method, the design of folded-cascode and three-stage op-amps are provided in a 0.18µm process CMOS technology with 1.8 V supply voltage. The simulation results exhibit the good performance of the proposed sizing method.

Keywords: Analog circuits sizing; Equation and simulation-based method; Automated layout generator; Multi-objective evolutionary algorithm based on decomposition; Operational amplifiers

Določanje velikosti analognih vezij z uporabo večciljnega algoritma na osnovi dekompozicije

Izvleček: Predlaganih je bilo več načinov načrtovanja analognih vezij, pri katerih se po določitvi velikosti vezja uporabi generator postavitve. Vendar je za pridobitev želenih specifikacij potrebnih veliko iteracij med fazama določanja velikosti vezja in generatorja razporeditve. Ta članek predlaga novo metodo, ki temelji na enačbah in simulaciji, za določanje velikosti vezij operacijskih ojačevalnikov CMOS (op-amperov) z upoštevanjem učinkov postavitve. V predlagani metodi se učinki postavitve upoštevajo v fazi določanja velikosti. Učinki razporeditve so parazitske lastnosti naprav in informacije o geometriji, ki se pridobijo iz novega avtomatiziranega generatorja razporeditve. Optimizacija se izvede z večobjektnim evolucijskim algoritmom, ki temelji na dekompoziciji (MOEA/D). Da bi ocenili učinkovitost predlagane metode za določanje velikosti, so na voljo zasnove zloženih kaskadnih in tristopenjskih operacijskih ojačevalnikov v tehnologiji CMOS z 0,18 µm procesom in napajalno napetostjo 1,8 V. Rezultati simulacije kažejo dobro učinkovitost predlagane metode določanja velikosti.

Ključne besede: Določanje velikosti analognih vezij; metoda na osnovi enačb in simulacij; avtomatiziran generator postavitve; večobjektni evolucijski algoritem na osnovi dokompozicije; operacijski ojačevalniki

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1 Introduction

Designing of analog integrated circuits includes three phases: topology selection, circuit sizing and layout extraction [1-4]. Experience of expert designers can be useful for designing simple circuits containing less number of devices. But, for the complex circuits the search space may be large. Therefore, it may be time consuming and complicated tasks for designers to generate an optimal solution for design variables [5]. Several methods have been proposed for automatic designing of analog integrated circuits using a set of rules depending on the circuits knowledge with respect to desired specifications. But, more effort is required to define new set of rules for different topologies.

Optimization-based methods can be divided into three categories as follows: equation-based [6-7], simulation-based [8-9] and equation and simulation-based methods [10-11]. It should be noted that se-

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vere performance degradation may be occurred after post-layout simulation due to layout parasitics. In the equation-based method, the circuit equations should be solved in order to satisfy the desired specifications. In the simulation-based method, a circuit simulator is utilized and a set of design variables are chosen such that the target specifications are satisfied. Finally, in order to have a trade-off between speed and precision of the two mentioned methods, equation and simulation-based method is employed.

Some works are suggested for dedicated analog blocks [12-15]. But defining the layout template frameworks or custom tools are the main limitation of using these methods. Model-based approach can be applied for automated analog circuit sizing [16-17]. The major advantage of the model-based approach is that the optimization process can be efficiently done by the performance models. In addition, evaluating the models needs much lower computational cost compared to the circuit simulations. This method has the additional advantage of reusing the models. The main drawback of the model-based method is the deviation between the desired circuit performances and the obtained circuit performances.

The gm/ID technique has been proposed in [18]. Its application in the circuit sizing has been shown in [19]. In another method, designer intervention is needed to estimate the gm/ID values [20]. In order to alleviate designer intervention, simulated annealing (SA) is employed to determine length (L) of transistors and gm/ID as variables with repeated reference to the gm/ID curve [21]. In [22], it has been shown that the performance constraints can be satisfied. However, severe performance degradation may be occurred after post-layout simulation due to layout parasitics. Therefore, a large number of iterations are needed between the circuit sizing and the layout generation.

Several Computer-Aided Design (CAD) tools have been proposed for the analog circuits [23-25]. It should be noted that the circuit performance may be influenced by layout parasitics. Therefore, deviation between the desired specifications of the circuit and the post-layout simulation results can be observed. Analog integrated circuits are sensitive to the layout parasitics. As a result, many iterations between the circuit sizing and layout synthesis are essential in order to obtain the desired target specifications [26]. If the mentioned issues are not considered, circuit overdesign may occur with the cost of increasing circuit power and area. On the other hand, circuit underestimation may deteriorate the post-layout simulation results. Therefore, it is required to incorporate layout information during sizing to alleviate the designing complexity and also the time-to-market.

In order to overcome the mentioned problems, sizing step should be performed by considering the layout effects. The sizing method to consider the layout effects includes parasitic-aware sizing and geometry-aware sizing [27-28]. In the parasitic-aware sizing method, layout parasitics are extracted continuously and then they are employed in the sizing process. In the geometry-aware sizing method, the geometrical parameters value such as width and length of MOS transistors are chosen to optimize the layout area. Several analog layout-aware sizing methods have been introduced in the literature. A CAD tools supporting layout aware circuit sizing is introduced in [29]. But, some of the layout parasitics are not considered. In another method, the sizing is performed by a knowledge-based tool using the equations [30]. This method is based on trial and error in which inside each loop the layout tool should be called several times in order to estimate the parasitics. The method introduced in [31] uses a genetic algorithm for circuit sizing. In this method, a cost function is defined based on a set of formula for circuit sizing. But the obtained results might be different from the real simulation results. In [32], multiple floorplan templates are employed in order to optimize the area of the placement. However, the layout parasitics are not regarded explicitly. Another parasitic-aware sizing method is introduced in [33]. This method can only be used for a pre-defined floorplan. An analog layout generation using modified cuckoo optimization algorithm (MCOA) is suggested in [34]. Layout parasitics are extracted to avoid the circuit performance deterioration. But, the layout information is not included in the sizing loop. A two-stage equation and simulation-based method for optimization of CMOS op-amps parameters is suggested in [10]. However, layout effects are not taken into account.

In this paper, an automatic equation and simulation-based methods for circuit sizing by considering layout effects is proposed. In this method, multi-objective evolutionary algorithm based on decomposition (MOEA/D) is used as optimizer. Circuit performance and layout effects are considered in the proposed method. In this paper, an automated method is adopted for placement and routing in analog layout generation using MOEA/D. In addition, both parasitics and geometrical information of the layout are regarded in the proposed method. The rest of the paper is organized as follows: The MOEA/D is described in Section 2. The proposed automatic sizing method is introduced in Section 3. Simulation results are given in Section 4. Finally, conclusion is provided in Section 5.

2 Multi-objective evolutionary algorithm based on decomposition (MOEA/D)

Recently evolutionary multi-objective optimization (EMO) algorithms have been widely utilized in many application fields [35-36]. EMO algorithms can be designed to search for a non-dominated solution set. Therefore, the entire Pareto front of a multi-objective optimization problem (MOP) can be approximated. In this paper, the MOP is introduced as follows:

$$\begin{aligned} &\text{Minimize}\,(f_1(x), f_2(x), \ldots, f_M(x)) \\ &\text{Subject to}\, g(x) \geq 0, X_L < x < X_H \end{aligned} \tag{1}$$

Where $f_i(x)$, $i = 1...M$ is the objective function, M indicates the number of objectives, x includes design variables, and X_L and X_H are their lower and upper bounds, respectively. The design constraints is shown by the vector $g(x)\geq 0$.

Multi-objective evolutionary algorithm based on decomposition (MOEA/D) has been introduced for MOP [37]. In the MOEA/D, a MOP is decomposed into several scalar sub problems so that the optimization is done simultaneously. It has been shown that using the information obtained from the solutions of neighborhood subproblems, the MOEA/D has less computational cost. This characteristic has been proved using many numerical tests.

In the MOEA/D, a scalar function is used to decompose a multi-objective optimization problem into a number of scalar optimization sub-problems. In this method, optimization is performed simultaneously by the evolutionary algorithm. In the MOEA/D, each non-dominated solution of the MOP is associated with an optimal solution of the single objective optimization problem and it can be calculated by a specific weight vector. A set of weight vectors is employed by the MOEA/D to provide different search directions. The different weight vectors can direct to search the different regions of the objective space. The decomposition a multi-objective optimization problem into N sub-problems is possible by Tchebycheff method. In this method, objective function of the j-th (j=1,2,...N) sub-problem is as follows:

$$g^{te}(x \mid \lambda^j, z^*) = \max_{1\leq i\leq m} \left\{ \lambda_i{}^j \mid f_i(x) - z_i^* \mid \right\} \tag{2}$$

Where $\lambda^j = \left(\lambda_1{}^j, \ldots, \lambda_m{}^j\right)^T$ demonstrates a weight vector, $z^* = (z_1^*, \ldots, z_m^*)^T$ represents a reference point. For each Pareto optimal point x^* there can be found a weight vector so that x^* is the optimal solution of (2). It should be mentioned that each optimal solution of (2) is a Pareto optimal solution of problem (1).

3 Proposed sizing method

First, the proposed placement and routing stages for the layout generation are explained. Then, the proposed circuits sizing by considering the layout effects is presented.

3.1 Placement

In the placement stage, the area of floorplan is optimized by simultaneous consideration of the constraints such as symmetry and proximity. It is necessary to place the devices by considering symmetry and proximity constraints in order to alleviate the parasitic coupling effects and also to improve circuit performance. The implementation details of these constraints can be found in [38]. It is worth to mention that the design rules must be satisfied in this stage. The devices to be placed on the floorplan are represented by k blocks M_1 …, M_k The objective function is defined for the placement stage as follows:

$$f_P = f_{oP1}(x) \tag{3}$$

$$f_{oP1}(x) = Width_{floorplan} \times Height_{floorplan} \tag{4}$$

In the above equation, $x = \{(x_1, y_1), \ldots, (x_k, y_k)\}$ indicates the coordinates of the left-bottom corners of the modules, $f_{oP1}(x)$ is the area of the floorplan. $Width_{floorplan}$ and $Height_{floorplan}$ represent the floorplan width and height, respectively. In the placement stage, optimization is performed using the MOEA/D.

3.2 Routing

In the routing stage, the terminals of the layout devices are electrically connected. In this proposed method, each wire is divided into d segments. Each segment is indicated by segment direction, segment layer and

Segment Direction	Segment Layer
Up Down Left Right	Layer 1 Layer 2 ⋮ Layer m

Figure 1: Wire Representation

segment length as shown in Figure 1. Segment direction is defined as up, down, left and right. Segment are located in the layers from 1 to m, where m is the number of the layers.

Positions of the segments are adjusted automatically so that the wire length between terminal pairs to be minimized. The objective functions for routing stage are proposed as follows:

$$f_R = (f_{oR1}(x), f_{oR2}(x), f_{oR3}(x)) \quad (5)$$

$$f_{oR1}(x) = \sum_{i=1}^{d} Length_{Segment_i} \quad (6)$$

$$f_{oR2}(x) = \sqrt{(x_{T_E} - x_n)^2 + (y_{T_E} - y_n)^2 + (z_{T_E} - z_n)^2} \quad (7)$$

Where $f_{oR1}(x)$ is the sum of the segment lengths from the starting terminal (T_S) to the last point on the wire (n). $(x_{T_S}, y_{T_S}, z_{T_S})$ and (x_n, y_n, z_n) are the coordinates of the starting terminal and the point n, respectively. $f_{oR2}(x)$ shows the euclidean distance from the point *n* to the target terminal (T_E) with coordinates $(x_{T_E}, y_{T_E}, z_{T_E})$ (See Figure 2). Objectives $f_{oR1}(x)$ and $f_{oR2}(x)$ are defined based on A^* algorithm [39]. Objectives $f_{oR3}(x)$ is the number of vias in the wire. Current-density to determine the segment width and design rules are the constraints in the routing stage.

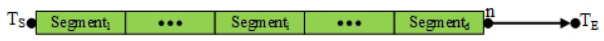

Figure 2: The wire segmentation

3.3 Parasitics Extraction

Interconnect parasitics that are considered here are wire resistance, wire substrate capacitance and wire coupling capacitance. Mathematical representations for resistance and capacitance for a tile on a layer in terms of their length and width are as below [40].

$$R = \rho_{sh} \times (\text{Length}/\ \text{Width}) \quad (8)$$

$$C_{sub} = C_a \times (\text{Length} \times \text{Width}) + C_{sw} \times (2 \times \text{Length}) \quad (9)$$

$$C_{coup} = C_c \times (\text{Length}/\ \text{distance}) \quad (10)$$

Where ρ_{sh} is sheet resistance per unit length, C_a indicates substrate capacitance per unit area, C_{sw} demonstrates capacitance per unit length, C_c shows coupling capacitance per unit length, and distance is defined as the space between two tiles. A resistance-capacitance (RC) π model is utilized to show net resistance and capacitance.

3.4 Circuit Sizing

The flowchart of the proposed circuits sizing by considering layout effects is shown in Figure 3. The proposed method details are as follows:

Step 1: Firstly, design variables such as width, length and the number of fingers of the MOS transistors and the passive components values, bias voltages and currents are selected.

Step 2: Target specifications of the operational amplifiers (op-amps) are defined using equations. Specifications of the circuit such as DC-gain, phase margin (PM), power dissipation (P_{diss}), settling time (ST), slew rate (SR) and unity-gain-bandwidth (UGBW) are evaluated. The optimization of the solutions is performed by MOEA/D.

Step 3: If the desired specifications are not satisfied, new solutions are searched by MOEA/D. In order to provide new solutions, design variables values that are mentioned in the step 1 are changed during optimization process. Otherwise, the solutions are given to the next stage.

Step 4: The netlist of the circuit is generated that is essential for HSPICE simulation.

Step 5: In order to evaluate the target specifications, schematic simulation is performed by HSPICE software.

Step 6: If the desired specifications are satisfied, the solutions are given to the placement step. Otherwise, new solutions are searched by MOEA/D. Solutions are defined similar to the step 3.

Step 7: A compact floorplan is generated in the placement stage by simultaneous consideration of symmetry and proximity constraints and also design rules.

Step 8: After placement stage, the routing is performed. The router generates wires between terminals as well as satisfying the constraints.

Step 9: The parasitics of the layout are extracted in order to perform post-layout simulation.

Step 10: If the circuit post-layout performance satisfies the desired specifications, the algorithm stops. Otherwise, MOEA/D is looking for new solutions.

4 Performance Evaluation

The proposed analog circuit sizing method is performed in a 0.18µm 1.8V CMOS technology. A new MATLAB toolbox is provided which is connected to HSPICE software. It can generate a netlist for HSPICE and also

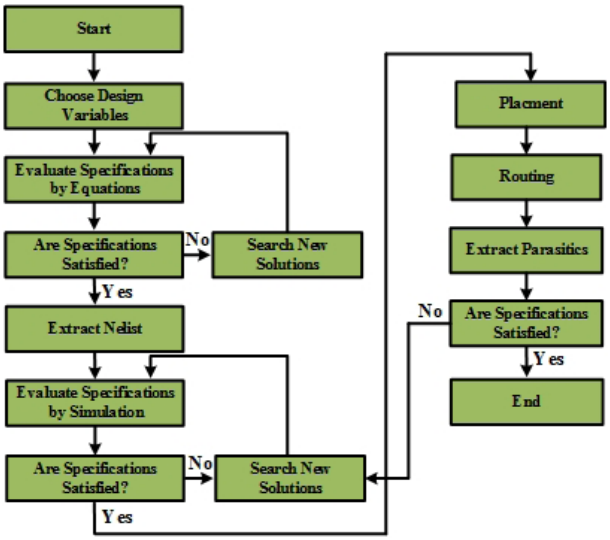

Figure 3: Flowchart of the proposed sizing method

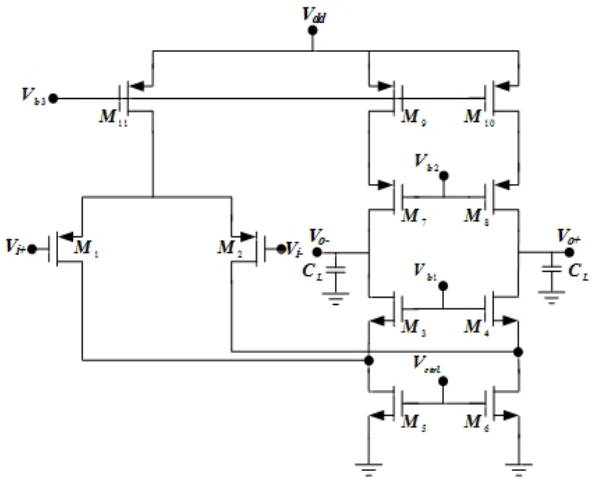

Figure 4: Schematic of the folded-cascode op-amp [5]

run it automatically in order to evaluate the target specifications. MOEA/D is implemented in MATLAB R2016b version and are here tested on Intel(R) core™ i5-4460 CPU @ 3.2 GHz with 16 GB RAM. The op-amps are an essential block in many mixed-mode systems [41-43]. In following, the design of folded-cascode and three-stage op-amps are presented.

4.1 Folded-cascode op-amp

The schematic of the folded-cascode op-amp with a p-channel input pair is shown in Figure 4 [5]. The design variables are the transistor sizes (width and length), the passive components values and the bias voltages values. The target specifications of the circuit are DC-Gain, UGBW, SR, P_{diss} and PM.

This circuit is designed by the proposed circuit sizing method. Designing is performed using minimum channel length transistor (0.18µm), width of the MOS transistors are chosen as 2µm≤ Wj ≤190µm, and bias voltage range is defined as $0.3V \leq V_{bi} \leq 1.5V$. Desired target specifications of the folded-cascode op-amp including DC-Gain, UGBW, SR, PM and Pdiss are shown in Table 1. MOEA/D is executed with a population of 100 individuals with 100 iterations. An example of placement stage progress using the proposed automated layout generator is shown in Figure 5. The Figures 5.a and 5.b show that the results are not compacted and symmetry and proximity constraints are not satisfied. The final result is depicted in the Figure 5.c in which the layout area is optimized and constraints for symmetry, proximity and design rules are satisfied.

The obtained result from the placement stage (Figure 5.c) is utilized for the routing stage. An example of wiring progress using the proposed automated layout generator is demonstrated in Figure 6. The results show that the objective functions defined by the equations (5)-(7) are optimized so that the shortest wire between two terminals is generated. The final result is shown in the Figure 6.c. The final layout after the routing is made by the proposed layout generator and the result is depicted in the Figure 7. The area of the layout is 27µm×43µm. The total number of wires is 26. In the Figure 7, metal 1 and poly are shown by cyan and blue colors, respectively. Design rules are also satisfied in the routing stage. It is worth to mention that in the routing stage the wires length are determined by current-density constraints.

The size of transistors for the folded-cascode op-amp layout shown in the Figure 7 are reported in Table 2. The pareto optimal fronts (POFs) of the folded-cascode op-amp including DC-Gain versus SR, DC-Gain versus UGBW, P_{diss} versus SR and PM versus UGBW are shown in Figure 8. As can be seen from the POFs, the proposed method can satisfy the target specifications well. The comparison results of the proposed method and the existing methods are reported in the Table 3. Two main advantages of the proposed method compared with the methods introduced in [10-11, 34] can be described as follows: 1) Circuit sizing and layout generation steps are not considered simultaneously in the existing methods. Therefore, circuit performances such as PM and UGBW may be degraded due to layout parasitics after post-layout simulation. It should be noted that in [10-11], the floorplan area is estimated approximately. 2) A set of solutions are provided by MOEA/D in the proposed method compared to the single solution in the existing methods [10, 34]. Therefore, the proper circuit can be selected for the specific application in the proposed method. Figure 9 show the POFs of the folded-cascode op-amp when only the simulation stage in

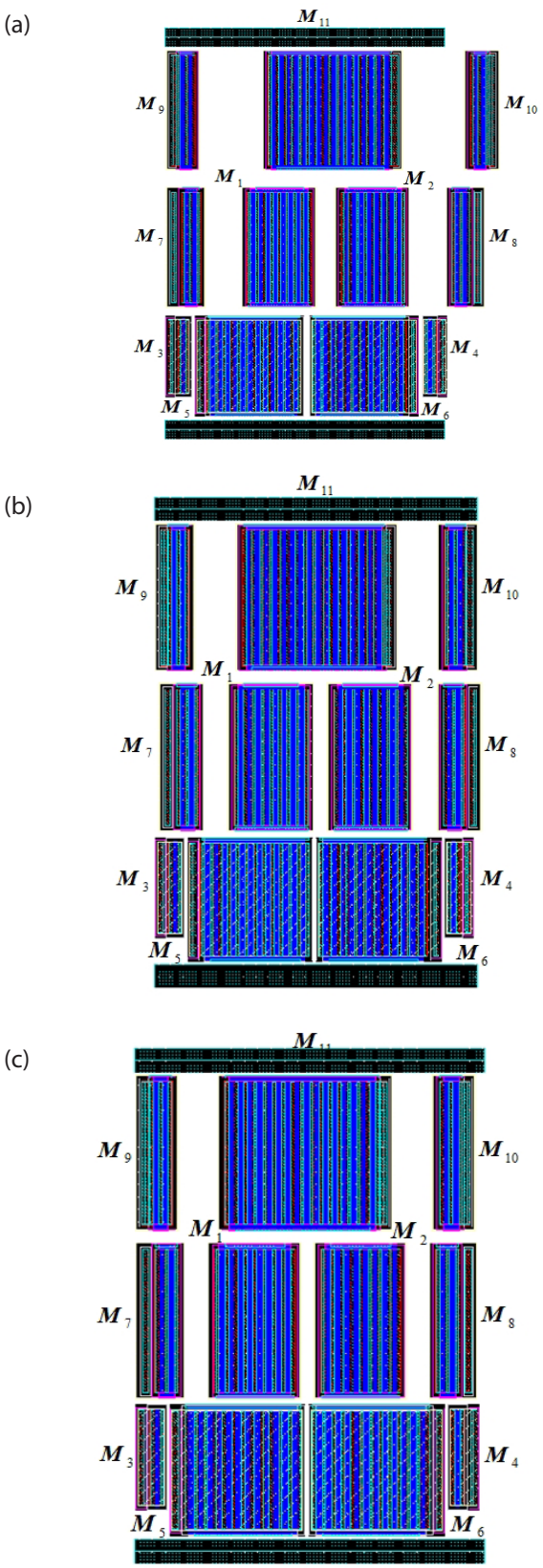

Figure 5: Example of placement stage progress using the proposed automated layout generator: (**a**) floorplan after 1 generation, (**b**) floorplan after 10 generations, (**c**) floorplan after 100 generations.

the Figure 3 is used. As can be seen from the results, the Figure 9.b is less widespread compared to the Figure 8.b. It shows the better performance of the proposed equation and simulation-based method compared to the simulation-based method.

Table 1: Desired target specifications of the folded-cascode op-amp

No.	Target Specifications	Value
1	DC-Gain	>50 dB
2	UGBW	>350 MHz
3	SR	>400 V/µs
4	PM	55°<PM<65°
5	Pdiss	Minimized

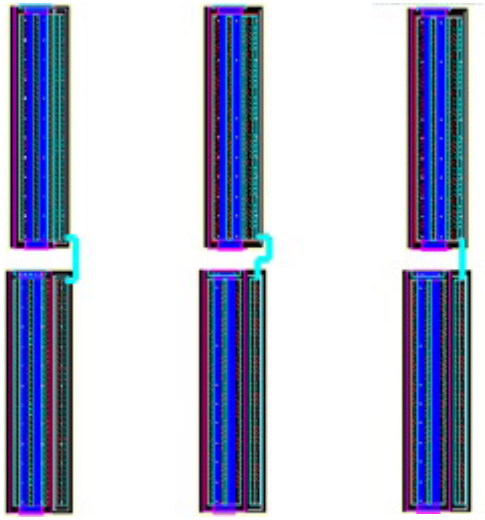

Figure 6: Example of routing stage progress using the proposed automated layout generator: (**a**) Wiring between two terminals after 1 generation, (**b**) Wiring between two terminals after 10 generations, (**c**) Wiring between two terminals after 100 generations.

Table 2: Size of transistors for the folded-cascode op-amp.

Parameter	Value
$(W/L)_{1,2}$	8x11.7µm/0.18 µm
$(W/L)_{3,4}$	1x7.8µm/0.18 µm
$(W/L)_{5,6}$	12x9.7µm/0.18 µm
$(W/L)_{7,8,9,10}$	2x111.7µm/0.18 µm
$(W/L)_{11}$	16x11.7µm/0.18 µm

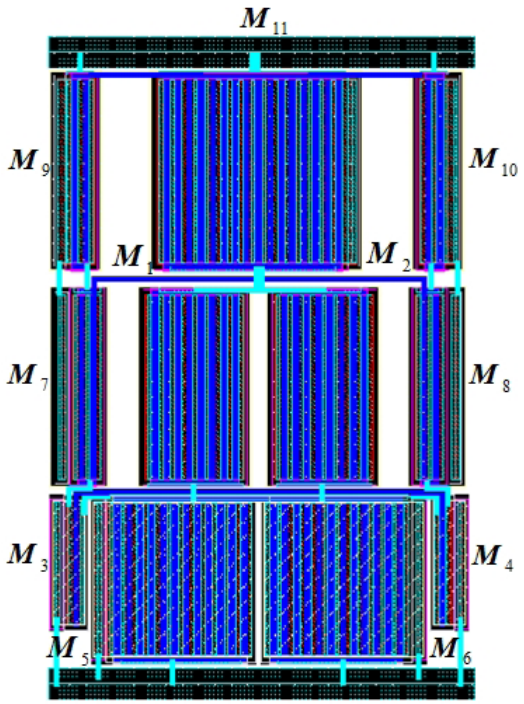

Figure 7: The layout generated by proposed method.

Table 3: The comparison results of the proposed method and the existing methods.

Specifications	This work	[10]	[11]
DC_Gain (dB)	53.9	53.9	53.4
Phase_Margin (°)	62.7	62.9	64.5
UGBW (MHz)	398	398	285
Power_Dissipation (mW)	1.1	1.1	0.79
Slew_Rate (V/µs)	534	470	320
Layout Area (µm^2)	1161	-	-
Total run time (s)	1880	1087	1023

4.2 Three-stage op-amp

In [43], optimization of the settling performance of a three-stage amplifier shown in Figure 10 is studied. This circuit is designed by the proposed method. One solution to the sizing result is shown in Table 4. The placement and routing results are done by the layout generator and the result is depicted in Figure 11. The area of the layout is 33µm×36µm. The total number of wires is 23. In this figure, metal 1 and metal 2 are shown by green and yellow colors, respectively. The POFs of the three-stage op-amp including ST versus P_{diss}, DC-Gain versus P_{diss}, SR versus P_{diss} and UGBW versus PM are shown in Figure 12. Table 5 reports the comparisons of post-layout simulation results of the proposed method with the existing methods. As can be seen from the results, the proposed method can achieve better ST compared to the existing methods [10, 11]. Since circuit sizing and layout generation steps are not considered simultaneously in the existing methods, the ST values are degraded after post-layout simulation

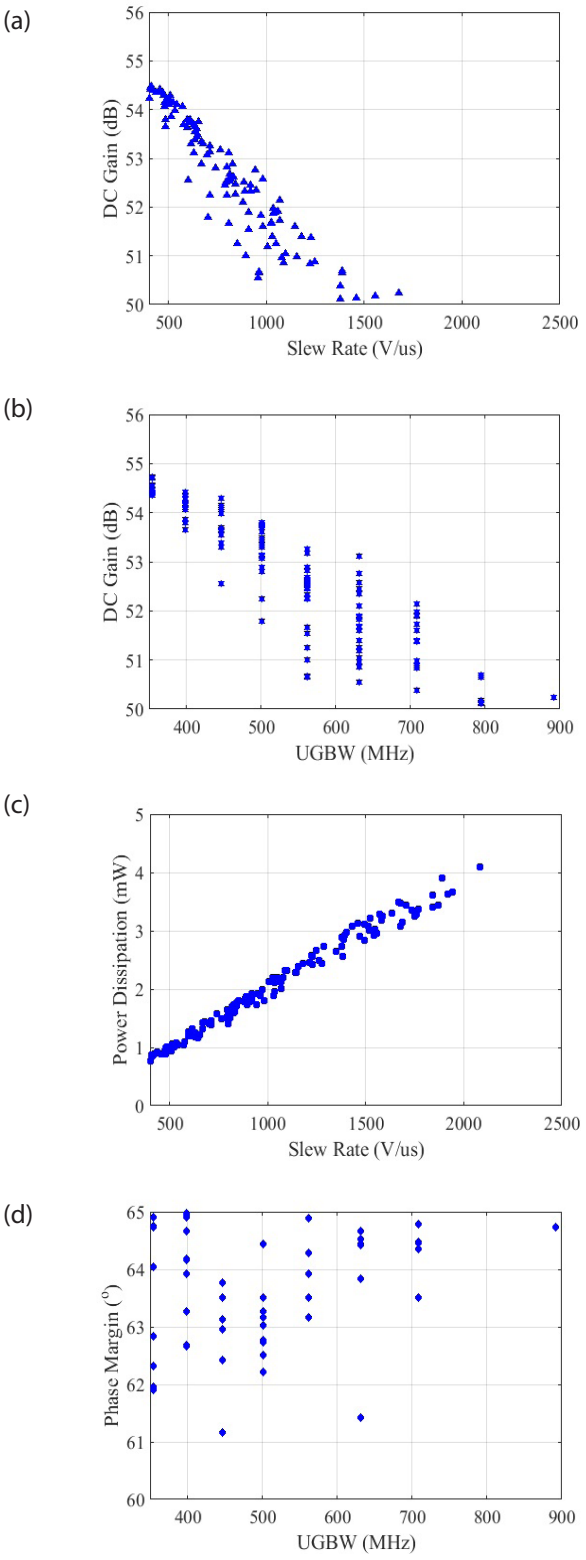

Figure 8: POFs of the folded-cascode op-amp using the proposed method: **a**) DC-gain versus SR, **b**) DC-gain versus UGBW, **c**) Pdiss versus SR, **d**) PM versus UGBW.

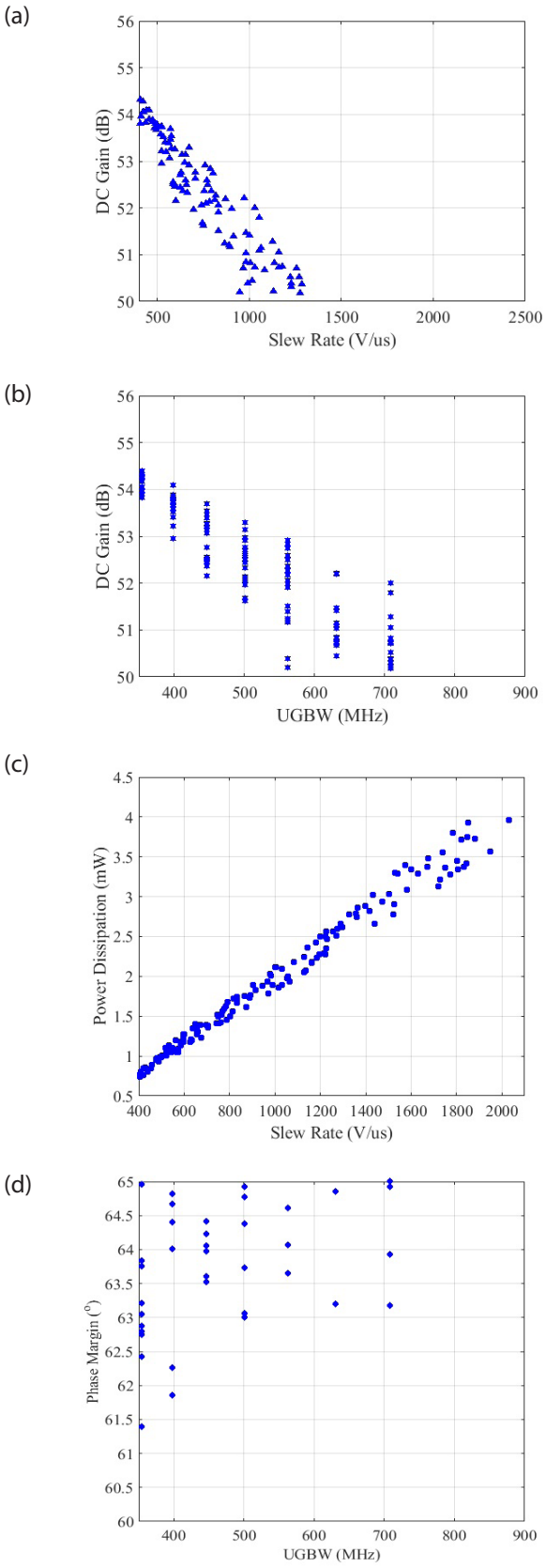

Figure 9: POFs of the folded-cascode op-amp obtained from only the simulation stage: **a**) DC-gain versus SR, **b**) DC-gain versus UGBW, **c**) P_{diss} versus SR, **d**) PM versus UGBW.

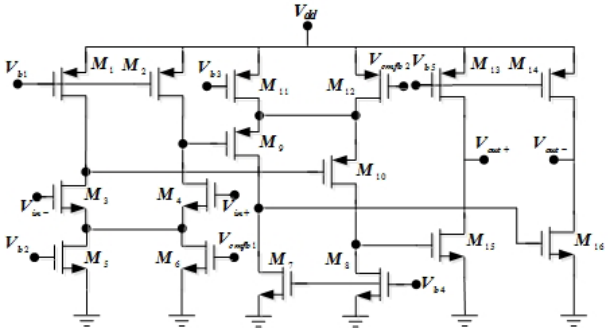

Figure 10: CMOS Three-Stage op-amp [43].

Table 4: Size of transistors for three-stage op-amp.

Parameter	Value
$(W/L)_{1,2,9,10}$	5x10µm/0.18 µm
$(W/L)_{3,4,5,6,7,8}$	5x5µm/0.18 µm
$(W/L)_{11,12}$	5x20µm/0.18 µm
$(W/L)_{13,14}$	5x20µm/0.18 µm
$(W/L)_{15,16}$	5x4µm/0.18 µm

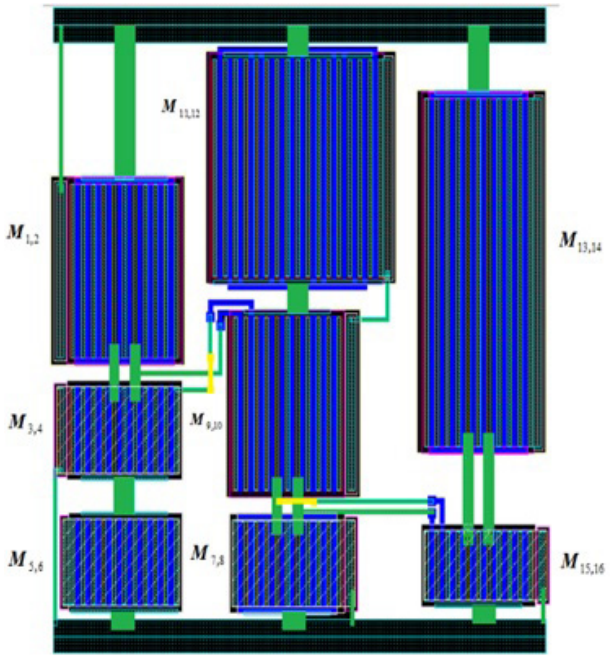

Figure 11: The layout generated by the proposed method.

Table 5: Comparisons of the post-layout simulation results for the three-stage op-amp.

Specifications	This work	[10]	[11]
1% Settling time (ns)	<4.4	4.9	5.2
Total runtime (s)	1531	1266	1134
Layout Area (mm^2)	0.0012	-	-

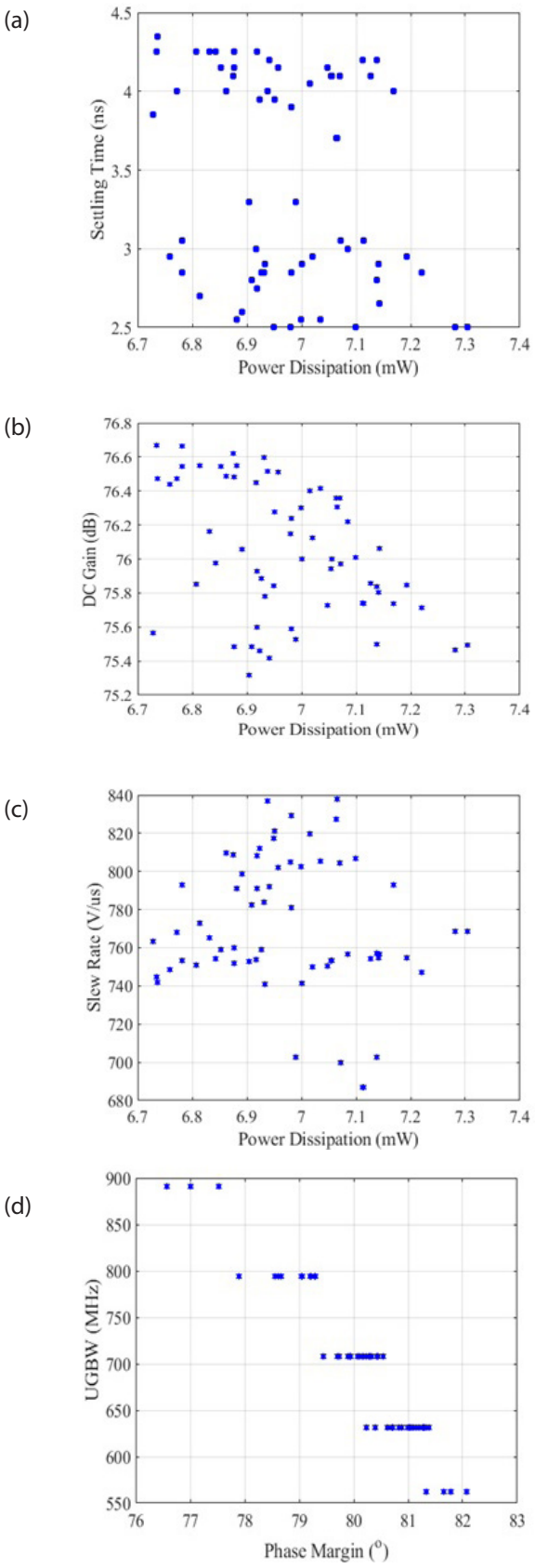

Figure 12: POFs of the three-stage: (a) ST versus P_{diss}, (b) DC-gain versus P_{diss}, (c) SR versus P_{diss}, (d) UGBW versus PM.

5 Conclusions

In this paper a new circuit sizing method has been proposed. During sizing process, layout effects including parasitics and geometry effects have been considered. A new placement method has been suggested in which compact floorplan has been generated by considering a set of constraints. A routing process has been presented to generate wires between terminals automatically. Design rules have been satisfied in the both of placement and routing stages by the proposed layout generator. The MOEA/D has been used for optimization which is suitable for multi-objective optimization problems. In order to evaluate the performance of the proposed circuit sizing method, designing of the folded-cascode and three-stage op-amps have been performed. The results indicated that the proposed circuit sizing method is quite promising.

6 Conflicts of Interest

The authors declare no conflict of interest.

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