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Design of Capacitive Sensing Chopper Amplifier Used in Artificial Nose Detection System

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Abstract: In this paper, we present the theoretical background and design procedure of a fully differentiated precision charge amplifier that can be used to detect small capacitive changes in an artificial nose detection system (ANose). We will show that with appropriate topology and optimization of circuit parameters, we can reduce 1/f noise and the offset and thus improve the sensitivity while keeping the power consumption at an acceptable level. Since the rate of capacitive changes due to adsorption/desorption is slow, a well-known technique such as chopping and autozeroing is used in a new way and described in the paper. The advantages and disadvantages of the proposed techniques are described. A combination of these two techniques in a single topology and new capacitive sensor ports are used to improve the detection sensitivity. Ideally, a sensitivity of 3 zF/√Hz can be achieved, but it could be slightly worse due to various non-idealities not considered.

Keywords: Fully differential chopper amplifier 1; Capacitive sensors 2; Ripple reduction loop (RRL) 3; Artificial nose 4

Nabojni Sekalni Ojačevalnik za Detekcijo Kapacitivnih Sprememb v Umetnem Nosu

Izvleček: V članku je predstavljeno načrtovanje ter teoretičen in simulacijski postopek pri izgradnji popolnoma diferencialnega, natančnega sekalnega nabojnega ojačevalnika, ki služi zaznavanju majhnih kapacitivnih sprememb v sistemu Umetni nos. Pokazali bomo, da lahko s pravilno topologijo in optimizacijo parametrov vezja zmanjšamo 1/f šum in ničelno napetost ter tako izboljšamo občutljivost, hkrati pa ohranimo porabo energije na sprejemljivi ravni. Ker je hitrost kapacitivnih sprememb zaradi adsorbcije in desorbcije relativno počasna, smo uporabili tehniko sekanja in zmanjševanje ničelne napetosti in 1/f šuma. Ti dve tehniki sta v članku uporabljeni na nov način in bosta podrobneje opisani. V nadaljevanju sledi opis prednosti in slabosti predlagane tehnike. Kombinacija obeh tehnik sekanja v eni topologiji in nove, diferencialne kapacitivne senzorske povezave se uporabljajo za izboljšanje občutljivosti zaznavanja. Teoretični izračun kaže, da je v idealnem primeru možno doseči občutljivost 3 zF/sqr(Hz). V realnosti pričakujemo nekoliko slabšo občutljivost, zaradi različnih neidealnosti, ki jih nismo upoštevali pri teoretičnem izračunu.

Ključne besede: Popolnoma diferencialen sekalni ojačevalnik 1; Diferencialni kapacitivni senzorji 2; RRL 3 ; Umetni nos 4.

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1 Introduction

The development and optimization of a detection system for artificial nose (ANose) with increased sensitivity for measuring small changes in differential capacitance represents a significant improvement in sensor technology. The collaboration between LMFE, JSI and FKKT in improving the ANose system emphasizes the importance of interdisciplinary collaboration in improving sensor capabilities [1] - [7].

The transition from an existing ANose system with thirty differential capacitive sensor pairs and thirty ASICS [2, 7] to a new integrated system with 256 capacitive sensor pairs integrated on a single ASIC shows promising progress in sensor array technology and ANose. The integration of the electronics for all channels on a single ASIC requires the development of an extremely low-noise input charge amplifier with minimal area and low power consumption. This innovation is essential for accurate measurements of small capacitive changes on modified capacitors due to adsorption processes.

The focus of the work is to analyze the influence of different noise sources that affect the overall noise during the measurements and to design a circuit that can improve the noise characteristics. This analysis is crucial for optimizing the noise performance of the new system. Through a detailed analysis of the chopping tech-

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nique, the capacitive sensor setup and the ripple reduction loop (RRL), the paper provides valuable insights into the design considerations and techniques used to achieve high sensitivity and low noise in the ANose system. The inclusion of simulation results in the paper adds a practical dimension to the theoretical framework and demonstrates the effectiveness of the proposed design and techniques.

The article is organized as follows. Section 2 presents the basic concept of the chopping technique. A one channel of ANose with the proposed capacitive sensor and the connection of a specially arranged chopper amplifier to the differential capacitive sensor pair is discussed in Section 3. The working principle of the ripple reduction loop (RRL) is described in Section 4. Section 5 presents some simulation results, while the last section concludes the article.

2 Chopping technique

The use of the chopping technique in the amplifier design for the ANose detection system is well justified. Chopping is a well-known method for attenuating offset voltage, 1/f noise and other unwanted artifacts in CMOS amplifiers, especially when amplifying small, low-frequency signals. In the context of the ANose detection system, which involves measuring extremely small changes in the capacitance, it must be ensured that the noise contribution and offset voltage of the amplifier do not distort the small signals. By designing a chopper amplifier, the system should effectively suppress these noise sources and maintain the integrity of the measured signals, allowing accurate detection of capacitance changes caused by adsorption processes. The use of a chopper amplifier in this application is a thoughtful approach to overcoming the challenges associated with amplifying and capturing small signals in a high-precision sensor system. By taking advantage of chopping, the design can improve signal quality, increase sensitivity and minimize the effects of noise and offset voltage, optimizing the performance of the ANose sensing system to detect small capacitance changes.

For this reason, we have developed a chopper amplifier. The operating principle is shown in a simplified block diagram in Figure 1. a) [9]. The challenges associated with DC input offset voltage and 1/f noise in CMOS amplifiers are significant, especially in high-precision applications such as the ANose sensor system. To combat the effects of 1/f noise, it is critical to select a chopper frequency in the amplifier design that exceeds the 1/f noise corner frequency of the amplifier. In addition, with this approach we may also measure the noise spectrum caused by the adsorption/desorption process in a band up to several 100kHz.

In the chopper amplifier configuration, the input signal is first subjected to upward modulation, where the signal is modulated to a higher frequency. Both the 1/f noise and the offset voltage of the amplifier are then added to the high frequency modulated signal. The amplified signal, including the noise and offset, is then modulated again with the same frequency, resulting in demodulation of the signal back to a lower frequency, while the offset voltage and 1/f noise are modulated upwards. This demodulation technique effectively separates the desired signal from the unwanted noise and offset components by up-modulating the noise and offset so that they can be removed later in the process.

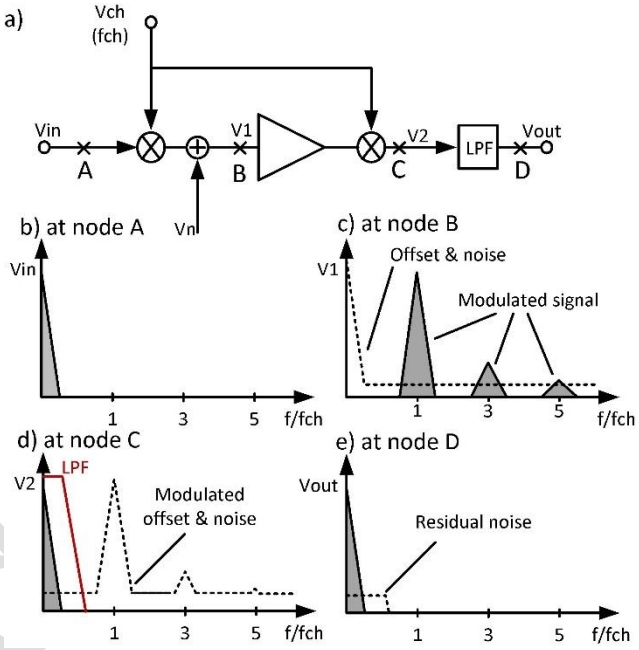

Figure 1: Simplified block diagram of chopper amplifier with spectrums in various nodes. a) Block diagram of chopper amplifier. b) Spectrum of the input signal Vin (node A), c) Spectrum of offset and noise together with the modulated input signal after amplification (node B), d) Spectrum after the second chopper (node C). The red shape represents the transfer function of a first order LPF filter, and e) the spectrum after the LPF (node D).

By integrating this modulation-demodulation approach into the design of the chopper amplifier, the system can effectively counteract the effects of 1/f noise and offset voltage of the circuit. Consequently, this strategy improves the overall quality and precision of the signals and facilitates the detection of small capacitance changes. In addition, the application of low-pass filtering in the system attenuates high-frequency components, as shown in Figure 1e). It is obvious that the chopper technique contributes to the reduction of 1/f noise and offset voltage when the chopper frequency exceeds the 1/f noise corner frequency of the amplifier. Furthermore, it is important to recognize that in practical scenarios, the level of thermal noise at the output of a chopper amplifier may slightly exceed that of a standard amplifier due to the folding of the thermal noise. In addition, charge injection effects may occur during operation of the amplifier, which must be taken into consideration [10]. To summarize, the inte-

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gration of chopper amplifiers with modulation-demodulation techniques together with low-pass filtering is a powerful strategy to attenuate the noise and the offset voltage problems, ultimately improving signal quality and accuracy.

3 One channel of ANose system

Figure 2 shows the simplified circuit diagram of one channel of the measuring system amplifier, which contains several important components for accurate signal processing. The programmable input DC signal source generates two DC voltages, Vsp and Vsn, which serve as input signals to the system. These DC voltages are chopped by the input differential chopper Ch01, resulting in the square wave signals Vin1 and Vin2; chopping frequency is programmable. They are connected to a pair of capacitive differential sensors as shown in Figure 2. The charges coming from the sensors are further processed by a low-noise charge amplifier consisting of a Gm1_Gm2 cell, which converts the charges into voltages via a feedback loop consisting of a differential chopper (Ch02) and feedback capacitors Cfb.

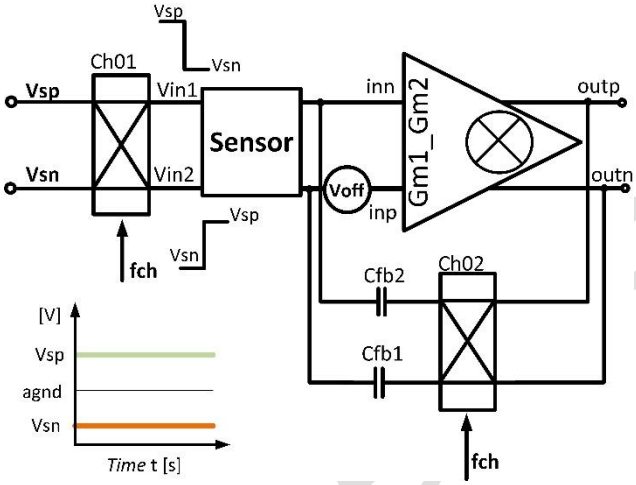

Figure 2: Charge amplifier for one channel of ANose detection system.

The arrangement of the components in this amplifier channel shows a systematic approach to signal processing and amplification. By using chopping techniques and incorporating feedback mechanisms, the amplifier design aims to increase sensitivity, reduce noise and optimize signal integrity for accurate detection of small capacitance changes in the ANose detection system. It is important to note here that the signal coming from the sensor due to capacitive changes can be several orders of magnitude smaller than offset or 1/f noise; fortunately, with correct signal processing it appears in different frequency band.
The integration of programmable input signals, differential chopping and a low-noise charge amplifier illustrates a comprehensive approach to signal processing in the measuring system. This design enables the precise measurements of extremely small capacitance variations and improves the overall performance and sensitivity of the ANose sensor system. The signal processing scheme shown in Figure 2 assumes that the chopping frequency exceeds the 1/f corner frequency of the amplifier. The signals Vin1 and Vin2 are square wave signals with a frequency fch and amplitudes of Vsp-Vsn, which represent the DC voltage difference between Vsp and Vsn. It is important to note that signals Vin1 and Vin2 are 180° out of phase; when Vin1 is connected to Vsp, Vin2 is connected to Vsn and vice versa (see Figure 3:a).

The details of the connection of the input voltages Vin1 and Vin2 to the capacitive differential sensor are shown in Figure 3.a. A sensor consists of two differential sensor pairs with a comb-like structure (see Fig. 3 b). Comb capacitors are covered with a thin layer of silicon dioxide. Each pair is then functionalized with different receptor molecules [1].
The measurement of sensor capacitance changes due to the adsorption of target molecules are significantly influenced by the electric field. In humid air, the breakdown voltage—where the air becomes conductive due to ionization—ranges from 5 to 10 megavolts per meter (MV/m). For 1um space between fingers of comb sensors capacitors and sensing voltage of 5V, we are already at the limit. However, it is possible to reduce the sensing voltage but then also the sensitivity is reduced. In addition, the gap between fingers cannot be smaller because of sensor functionalization technology. This is the main reason why 180 nm CMOS technology is good for our detection system.

Assuming that surface of Cp is functionalized, and surface of Cn is not functionalized, the adsorption of target molecules changes the capacitance Cp, while the capacitance Cn remains the same. The capacitance changes due to adsorption are represented by Cads1 and Cads2 on Figure 3.a. The signal connection structure ensures that the differential signal generated by the sensor pair is effectively detected and processed by the differential charge amplifier, so that the charges at the output of the charge amplifier are effectively converted into differential voltage. To detect these small differential capacitance changes, each part of the sensor is divided into two parts to extract differential charges across the inn and inp nodes.

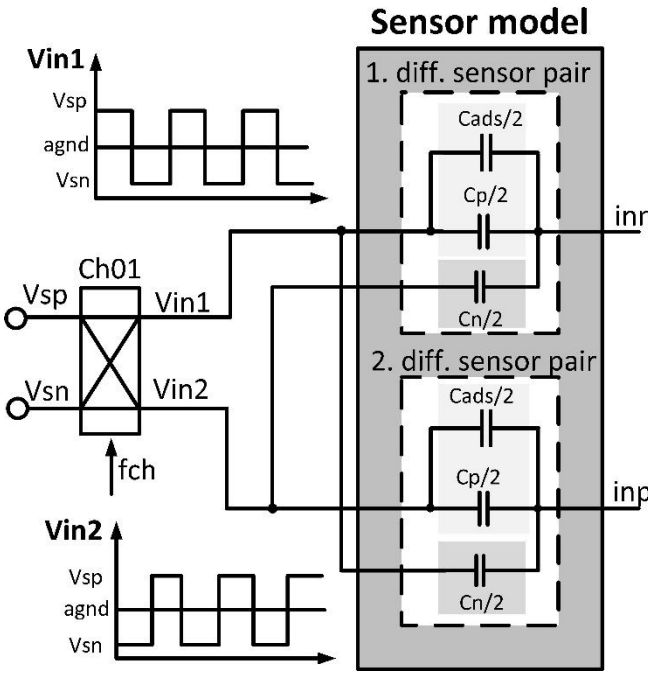

Figure 3: a) Differential capacitive pair connection.

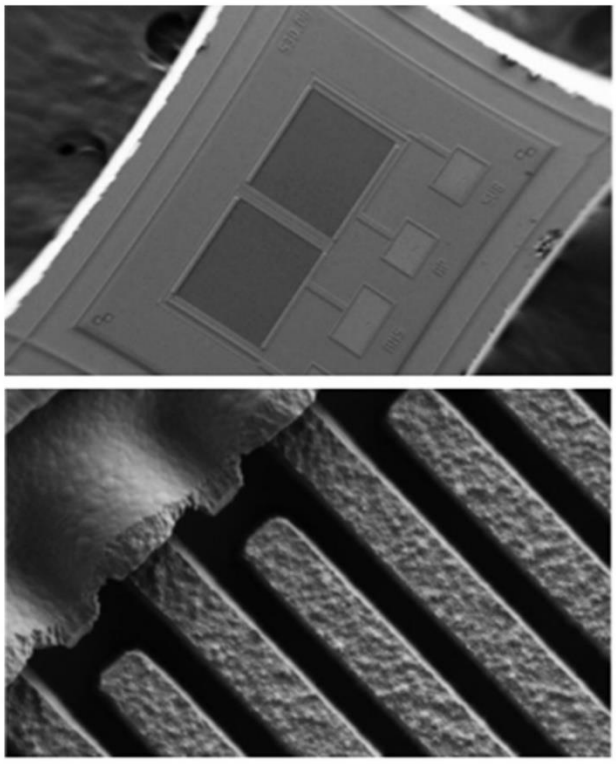

Figure 3: b) Comb capacitive sensor.

By organizing the sensor structure in this way, two pairs are formed as shown in Figure 3. The first pair includes Cp1 + Cads1 and Cn1, while the second pair consists of Cp2 + Cads2 and Cn2. In addition, the signals Vin1 and Vin2 are connected to the differential sensor pairs, as shown in Figure 3. Vin1 is connected to a node consisting of capacitors Cads1 and Cp1, while Vin2 is connected to a node with Cn1. In the second differential sensor pair, the Vin2 signal is connected to Cads2 and Cp2, while Vin1 is connected to Cn2.

At this point we assume that Vsp -Vagnd = Vagnd - Vsn = Vs, so that the charges in time (n-1) and (n) at the first differential sensor pair at inn and assuming that the sensors are connected to the virtual ground of the charge amplifier are (1) and (2):

$$q(n-1) = (V_s(n-1) - \mathrm{Vagnd}) \cdot (C_{ads1} + C_{p1} - C_{n1}) \quad (1)$$

$$q(n) = (V_s(n) - \mathrm{Vagnd}) \cdot (C_{n1} - C_{ads1} - C_{p1}) \quad (2)$$

Charges in time (n-1) and (n) on the second differential sensor pair on inp are given by (3) and (4):

$$q(n-1) = (V_s(n-1) - \mathrm{Vagnd}) \cdot (C_{n2} - C_{ads2} - C_{p2}) \quad (3)$$

$$q(n) = (V_s(n) - \mathrm{Vagnd}) \cdot (C_{ads2} + C_{p2} - C_{n2}) \quad (4)$$

Now let's take a closer look at the signals in the time domain and parts of the charge amplifier. For one differential capacitive pair, and if Vsp = - Vsn = Vs, we can calculate the voltage step Vin1 on one capacitor pair according to (5):

$$\mathrm{Vin_1} = \mathrm{V_{sp}} - \mathrm{V_{sn}} = 2\,\mathrm{V_s} = \Delta\mathrm{Vin} \quad (5)$$

The same is true for the second differential pair (6):

$$\mathrm{Vin_2} = -\mathrm{V_{sn}} - \mathrm{V_{sp}} = -2\,\mathrm{V_s} = -\Delta\mathrm{Vin} \quad (6)$$

$$|\mathrm{Vin_1}| = |\mathrm{Vin_2}| = \Delta\mathrm{Vin} \quad (7)$$

The signals Vin1 and Vin2, generated after the first chopper in the circuit in Figure 3, have rectangular shapes with a step size of ΔVin, as suggested in (5), (6) and (7). These waveforms consist of transitions between two different voltage levels, resulting in a square wave or a rectangular waveform at the output. The step size ΔVin indicates that the amplitude is the difference between the high and low voltage levels Vsp and Vsn. Assuming an ideal amplifier (block Gm1_Gm2) with an offset voltage of zero and assuming that Cp = Cn and Cads=0 and also that the nodes inn and inp are at virtual ground potential, the charge conservation equation for the simplified single-ended circuit during the transition of the input signal from low to high at Vinp (or from high to low at Vinn) can be expressed as equation (8):

$$[\Delta\mathrm{Vin} \cdot (C_{p1} + C_{ads1}) - \Delta\mathrm{Vin} \cdot C_{n1}] + [(\mathrm{Voutn}(n) - \mathrm{Voutn}(n-1)) \cdot C_{fb1}] = 0 \quad (8)$$

For Cads=0 the output voltages are equal, therefore:

$$\mathrm{Voutn}(n) = \mathrm{Voutn}(n-1)$$

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At the transition from high to low, the circuit behaves similarly to the transition from low to high, but with reversed polarity, since the input voltage jump by –ΔVin, and thus the changes in the output voltages also have reversed signs. If the capacitances Cads1 and/or Cads2 are no longer zero, the output voltages are also no longer zero:

$$\mathrm{Voutp(n)} = \mathrm{Voutp(n-1)} + \frac{C_{ads1}}{C_{fb2}}\Delta\mathrm{Vin} \quad (9)$$

$$\mathrm{Voutn(n)} = \mathrm{Voutn(n-1)} - \frac{C_{ads2}}{C_{fb1}}\Delta\mathrm{Vin} \quad (10)$$

Looking differentially and if $C_{fb2} = C_{fb1} = C_{fb}$:

$$\mathrm{Vout_{diff}(n)} = \mathrm{Vout_{diff}(n-1)} + \Delta\mathrm{Vin} \cdot \frac{C_{ads1}+C_{ads2}}{C_{fb}} \quad (11)$$

The differential output voltage is proportional to ΔVin and the ratio between (Casd1 +Cads2) and Cfb.

The first sub cell within the amplifier block gm1_gm2, called gm1, acts as a transconductance amplifier. This sub-cell converts the input voltage applied to node inn into an output current as defined in equation (12).

$$\mathrm{ip} \cong \left(\frac{\frac{C_{ads1}}{C_{fb2}}\Delta\mathrm{Vin}}{A}\right) \cdot g_{m1} \quad (12)$$

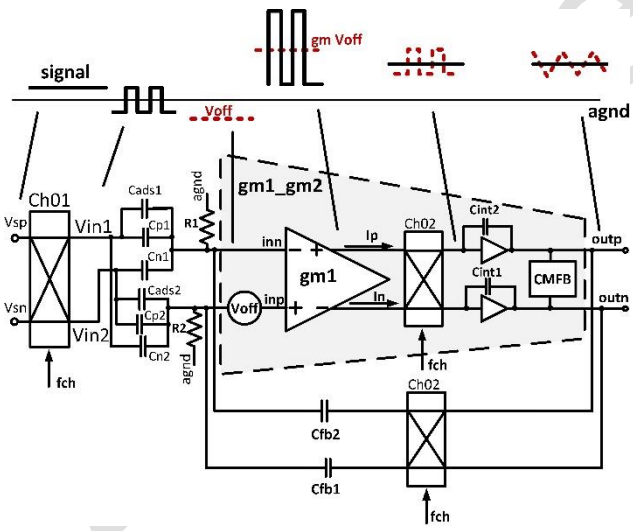

Figure 4: Charge amplifier with signals in the time domain. Black signals are caused by Cads, while signals in red are due to the offset voltage of the op-amp.

It is assumed that the influence of the parasitic capacitance at the inn node on the circuit is negligible, assuming ideal behavior in the time domain. The expression

Table 1: Value of charge amplifier parameters.

Parameters of charge amplifier			
Cads	100fF	Cp1, Cp2	200fF
Ain	1V	Cn1, Cn2	200fF
vdd	5V	R1, R2	30kΩ
Voff	5m	Cint1, Cint2	250fF
agnd	2.5V	Cfb_1, Cfb_2	200fF
Vsp	3.5V	fch	1M
Vsn	1.5V		

containing gm1 as the trans-conductance of the first stage and A as the ideal open-loop gain of the entire amplifier gm1_gm2 refers to the operating characteristics of the amplifier block. A similar expression applies to the input inp. The chopper Ch02 reverses the connection of ip and in into two integrator stages; they convert currents to voltages and at the same time serve as low-pass filters. The voltage at the output of the integrator is calculated from equation (13):

$$\mathrm{Voutp(t)} = \mathrm{Voutp(0)} + \frac{\mathrm{ip}\cdot t}{C_{int2}} = \mathrm{Voutp(0)} + \frac{\left(\frac{C_{ads1}}{C_{fb2}}\Delta\mathrm{Vin}/A\right)\cdot g_{m1}\cdot t}{C_{int2}} \quad (13)$$

Since ip = -in, the voltages Voutp and Voutn at the end of Tchp/2 are Voutp = -Voutn. This condition indicates an antiphase relationship between the output voltages at the end of the first half of the chopping period. At the transition from (inn, inp) to (outp, outn), the cell gm1_gm2 acts as a voltage amplifier, with Voutp and Voutn representing integrated versions of the output currents (ip, in) derived from gm1.
The common mode feedback loop (CMFB) serves as a correction mechanism for the common mode output voltage. By using two integrators in the circuit design, the currents ip and in are effectively converted into two voltages. Up to this point, we have neglected the offset voltage of the amplifier. If we add the model of the offset voltage of gm1 to equations (12) and (13), we obtain equation (14). This equation gives a more detailed insight into the total output current (ip, in), taking into account the characteristics of the transconductance and the effects of the offset voltage of the gm1 amplifier.

$$\mathrm{ip} = \left(\frac{\frac{C_{ads1}}{C_{fb2}}\Delta\mathrm{Vin(t)}}{A}\right) \cdot g_{m1} + \frac{V_{off}}{2} \cdot g_{m1} \quad (14)$$

The current ip is now made up of both the direct current component (DC), which is caused by the offset, and the alternating current component (AC), which is caused by the input voltage. This combined current is then

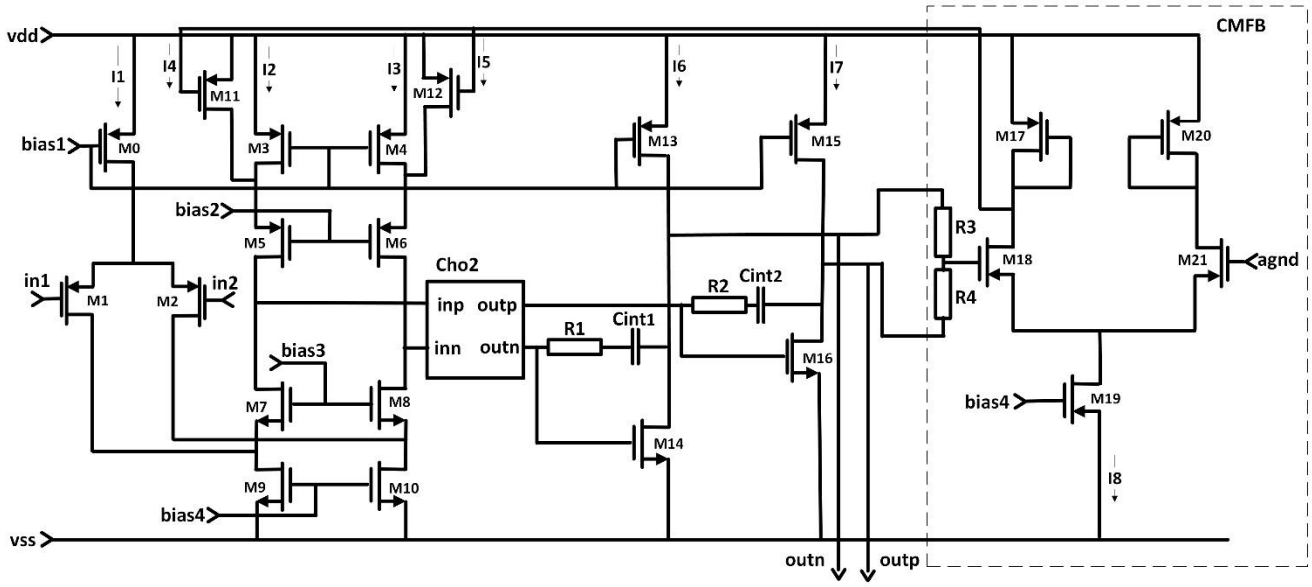

Figure 5: Simplified circuit diagram of gm1_gm2 cell.

chopped with Ch02, a component that reverses the connection of the currents to two output stages. Under ideal conditions, the process is equivalent to multiplying each signal by ±1, so that the measured signal is down sampled, and the offset is up-sampled. See Figure 4 for time domain signals and Table 1 for values of simulation parameters. The voltages Voutp and Voutn at time t are calculated according to equation (15):

$$V_{outp}(t) = V_{outp}(0) + \frac{C_{ads1} g_{m1} \Delta \boldsymbol{Vin}\, t}{C_{fb2} C_{int2} A} + \frac{\boldsymbol{v_{off}} g_{m1} t}{C_{int2}} \quad (15)$$

Equation (18) represents the complete output voltage, (16) represent the DC part, while (17) represent the V_{AC} part.

$$V_{DC} = \frac{C_{ads1} g_{m1} \Delta \boldsymbol{Vin}}{C_{fb2} C_{int2} A} \mathrm{t} \quad (16)$$

$$V_{AC} = \frac{\boldsymbol{v_{off}} g_{m1}}{C_{int2}} \mathrm{t} \quad (17)$$

$$V_{outp}(t) = V_{outp}(0) + V_{DC} + V_{AC} \quad (18)$$

V_{DC} is contribution of Cads1 and V_{AC} is contribution of the offset voltage (voff) and the 1/f noise of the gm1 cell.

Figure 5 shows simplified circuit diagram of gm1_gm2 cell. It is built as modified folded cascode amplifier that implements a gm1 part of the cell using PMOS folded cascode circuit. The output currents are chopped using chopper Cho2, which is constructed from for CMOS switches, followed by two integrator stages. The common mode feedback amplifer(CMFB) controls the common-mode output voltage levels through the gm1 stage. The value of transistors dimensions, supply current, bias voltage and passive component of gm1_gm2 cell are presented in Table 2.

The ripple caused by the offset voltage, which is transferred to frequency fch, can significantly affect the signal quality and accuracy.

Table 2: Dimensions of transistors, supply current, bias voltages and passive components of gm1_gm2 cell.

Parameters of gm1_gm2 cell			
Mo	$16\frac{10u}{2u}$	R1, R2	5kΩ
M1, M2	$4\frac{24u}{1u}$	R3, R4	1.5MΩ
M3, M4	$12\frac{10u}{2u}$	bias1	4V
M5, M_6	$16\frac{10u}{0.5u}$	bias2	3.668V
M7, M_8	$16\frac{8u}{1u}$	bias3	1.187V
M9, M_{10}	$24\frac{8u}{2u}$	bias4	0.9V
M11, M12	$4\frac{10u}{2u}$	I1	80uA
M13, M15	$32\frac{10u}{2u}$	I2, I3	60uA
M14, M16	$8\frac{8u}{1u}$	I4, I5	20uA
M17, M20	$4\frac{10u}{2u}$	I6, I7	160u
M18, M21	$4\frac{4u}{1u}$	I8	40u
M19	$8\frac{8u}{2u}$	agnd	2.5V
vdd	5V	vss	0V

For example, if we have an offset voltage of 10mV, the amplitude of the AC voltage at the chopping frequency for fc=1 MHz, transconductance of 0.1mS and Cint=10pF, the calculated output AC voltage, also

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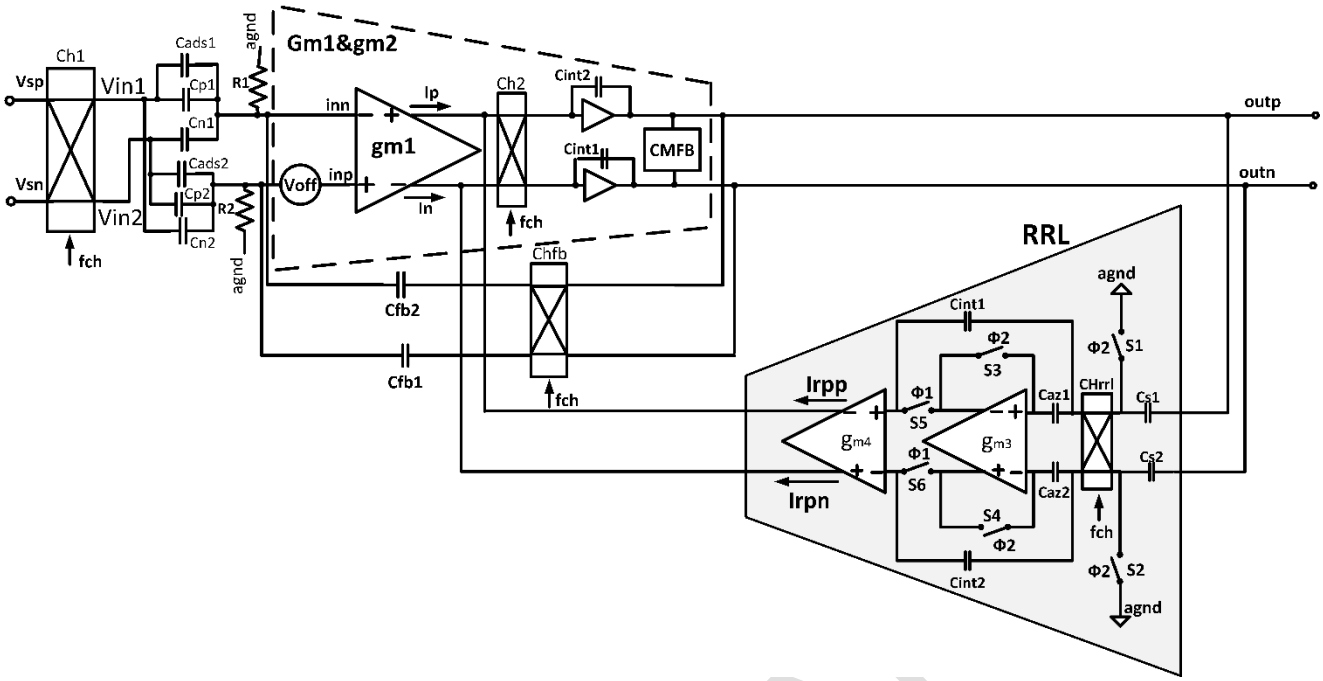

Figure 6: RRL that consists of sensing capacitors Cs1, Cs2, a demodulating chopper CHrrl, autozeroed S-C integrator and a compensation transconductor gm4.

known as ripple voltage, is 50mV. To attenuate or remove this ripple caused by the offset voltage (and 1/f noise), we could use LP filtering, however more efficient and better technique is so called ripple reduction loop (RRL), that will be described in the next section.

3.1 Ripple reduction loop

The ripple at the output due to the modulated offset and 1/f noise of the transconductance amplifier cell gm1 is undesirable as it can affect the accuracy and performance of the system, especially in applications with low frequency signals such as ANose. There are several effective techniques to mitigate this ripple, such as filtering techniques and other suppression techniques described in the literature [9], [10]. It is crucial to address this issue as excessive ripple can eat up headroom and degrade the quality of the output signals. One approach to reduce the ripple is the ripple reduction loop (RRL) shown in Figure 6 and the value of parameters are listed in Table 3.

Table 3: Parameters of RRL that are used in simulation.

Parameters of RRL			
Caz1, Caz2	33fF	$Cint1_{RRL}$, $Cint2_{RRL}$	33fF
Cs1, Cs2	33fF	fch	1MHz

RRL is specifically designed to detect the ripple at the output of the voltage amplifier. As soon as the ripple is detected, the RRL generates compensating currents to compensate the DC offset current generated by the transconductance amplifier gm1. Ideally, it is possible to reduce the ripple completely. In the ideal case, the output ripple of the signals Voutp and Voutn should no longer be present after using the RLL technique [8].

Ripple voltage at the output can be calculated from equation (19):

$$V_{ripple} = \frac{(V_{offset} \cdot g_{m1})}{(2 \cdot f_{chop} \cdot C_{int})} \quad (19)$$

The ripple caused by the offset voltage can be reduced by decreasing gm1 or increasing Cint. Since reducing gm1 can lead to increased noise, this approach is not effective. Adjusting parameters such as chopping frequency (fch) and integration capacitance (Cint) can affect the residual offset, chip area and power consumption. By using the RRL technique, the system can effectively suppress the output ripple and improve the overall performance and stability of the charge amplifier.
In this paper, an AC-coupled discrete-time ripple reduction loop (RLL) is presented. The block diagram and the components of the ripple reduction loop (RRL) are shown in Figure 6. This diagram illustrates how the RLL is structured, and which are the main components involved in the ripple reduction process.

The ripple reduction loop (RRL) consists of the following important components:

i. Sensing capacitors (Cs1,2). These capacitors Cs1,2 sense and convert the large ripple voltage at the amplifier's output into an AC current, which is proportional to the slope of the ripple.
ii. A demodulating chopper (CHrrl). The demodulating chopper processes the AC current generated by the sensing capacitors, helping to

extract and isolate the ripple component for further signal processing

iii. An integrator. It is utilized to integrate the AC current signal, acting as a low-pass filter to smooth out the ripple and convert it into a voltage signal proportional to the ripple amplitude. It serves also as S/H stage.

iv. A compensation trans-conductor gm4. It receives the voltage signal from the integrator and generates compensating currents to compensate the effects of the ripple in the output signals.

The RRL generates a notch at frequency fch with a width determined by flexible design parameters such as Cs1,2 and gm4 [8]. A passive integrator consisting of a current buffer and an integration capacitor used in the RRL has the offset of the current buffer, which produces a second harmonic ripple that would require a large integration capacitor for filtering [10], [11]. In our system, we designed an integrator with automatic zeroing and switched capacitor (see Figure 6), as this is a common technique used in precision analog circuits to reduce offset errors. In this design approach, the integrator is reset during one phase of the operating cycle so that its offset voltage is stored on a self-zeroing capacitor (Caz1,2). The implementation of a self-zeroing switched capacitor (SC) integrator in the circuit enables periodic storage and clearing of the offset voltage. This process minimizes the offset error of the integrator and the S/H stage and improves the accuracy of the circuit by effectively reducing the unwanted voltage offsets of the RLL. However, it is essential to note that the output of the integrator must not be connected to gm4 during the integration phase of the offset cancellation. If such a connection is made, there is a risk that error-compensating currents will be fed into the voltage amplifier (block gm1&gm2). During this time, the voltage at the input of gm4 is kept constant by the voltage stored in the capacitors Cint1 and Cin2.

The SC integrator consists of sampling capacitors Cs1,2, a demodulation chopper CHrrl, integration capacitors Cint1,2, auto-zero capacitors Caz1,2 and a single-stage operational amplifier gm3. CHrrl is synchronised with fch, and the remaining switches (S1-S6) are controlled with the switching frequency faz, which is set to half of fch (see Figure 7). The signal faz contains an integration phase Φ1 and an auto-zero phase Φ2, and each phase comprises a complete cycle of fch. Thus, a ripple can be detected and stored by the full-cycle ripple reduction loop (RRL) operation during Φ1. A timing diagram is shown in Figure 7.

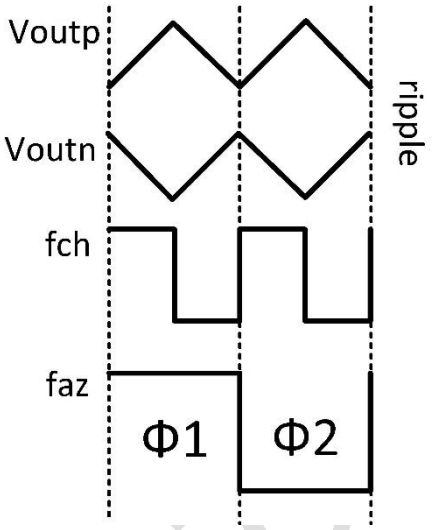

Figure 7: Timing diagram of output ripple, chopping frequency (fch) and auto zeroing frequency (faz), which is set to half of fch.

During Φ1, Cs1,2 plays a critical role in the operation of the circuit by converting the ripple voltage into an alternating current. This alternating current is further processed by demodulation of CHrrl (a demodulating chopper). The demodulated signal is then integrated at Cint1 and Cint2. The voltages at capacitors Cint1 and Cint2 are used to drive gm4, which converts the differential voltage into two currents to compensate for the offset current of gm1. During phase 2 (Φ2), the measuring capacitors Cs1,2 are short-circuited to the analog ground so that no ripple current can be integrated. At the same time, the input voltage at gm4 is kept at a constant level, as the voltages at Cint1 and Cint2 are kept constant during this phase.

This configuration ensures that no additional ripple current is introduced or integrated during Φ2 and the input voltage at gm4 remains stable. Gm3 is configured in the unity gain configuration so that its offset is sampled and stored on Caz1,2. During this time, Cint1 and Cint2 are disconnected from the output of gm3, hold the voltage set at the end of the last Φ1 and are connected to the input of gm4. In this way, the correct compensation current is fed into gm1 in both phases. Ideally, the compensation current fully compensates the offset current of gm1 so that no output ripple occurs in the steady state.

Before looking at the simulation results, let's calculate SnR and minimum capacitance that can be detected using proposed charge amplifier. Assume the BW is 1Hz, Cads = 100fF, Cp = Cn = 200fF, Vndth_in = 10nV/. RMS signal and RMS noise at the output of the charge amplifier can be calculated from equations (20) and (21):

$$V_{sout\_RMS} = \frac{V_{in}}{\sqrt{2}} \cdot \frac{C_{ads}}{C_{fb}} \tag{20}$$

$$V_{ndout\_RMS} = V_{ndth_{in}} \left(1 + \frac{C_{ads}+C_p+C_n}{C_{fb}}\right) \tag{21}$$

The calculated SnR for the proposed conditions is 140dB/√Hz. The minimum capacitance that can be detected, is thus Cads>=2.82· zF/√Hz.

4 Simulation results

The presented topology of a fully differential capacitive coupled chopper amplifier with a differential capacitive sensor pair at the input and RRL was simulated in Cadence using TSMC's 180nm CMOS technology PDK.

The simulation consists of the same blocks as shown in Figure 6. First, a capacitively coupled charge amplifier is simulated when the RRL is switched off. The ripple at the output of the charge amplifier is mainly caused by the offset voltage of the transconductance amplifier gm1. In the simulation, we set the offset voltage of gm1 to 5mV, which corresponds to the typical offset of CMOS amplifiers, Cads = 0fF, Vin = 1V, fch = 1MHz, gm1= 0.1mS and Cint =10pF. The calculated output voltage ripple from equation (19) is Vripple= 25mV and the measured voltage ripple from the simulation is 26mV, which is almost identical (see Figure 8 and Table 1).

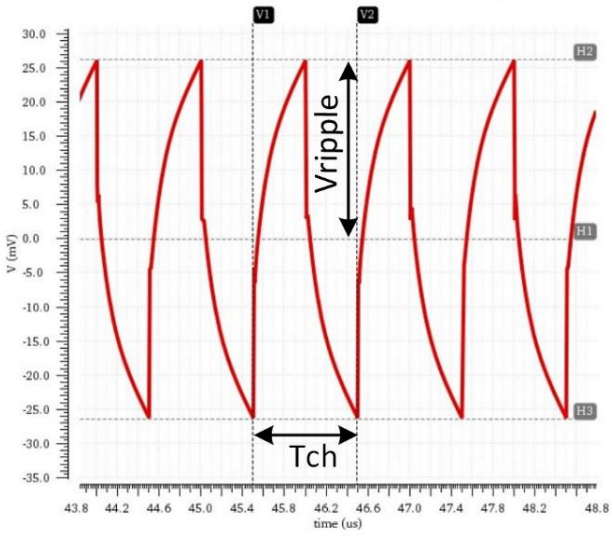

Figure 8: Differential signal at output of charge amplifier without RRL and with Cads is 0.

Figure 9 shows the result (output voltages) when RRL is switched on. It can be seen that RRL can suppress the ripple caused by the offset voltage of gm1 by a factor of approx. 100. If you enlarge the diagram in Figure 9a, you can see that some ripple is still present (see Figure 9b).

The measured ripple is 0.00038 V, as shown in Table 1 in the third row. Then we performed another simulation when Cads was no longer zero. The DC output voltages (see Figure 9 and Figure 10) are calculated using equations (9) and (10). The data used for the simulations are Vin = 1V, Cads1 = Cads2 = 100fF and Cfb1 = Cfb2 = 200fF and the signal ground is Vdd/2 = 2.5V. The DC output voltages are 3V and 2V, i.e. 0.5V, which are different. First, we simulated the system when RRL was switched off.
And then we did a simulation when RRL was switched on. The measured voltage ripple without RRL is 26mV and the measured voltage ripple with RRL is 0,3mV.

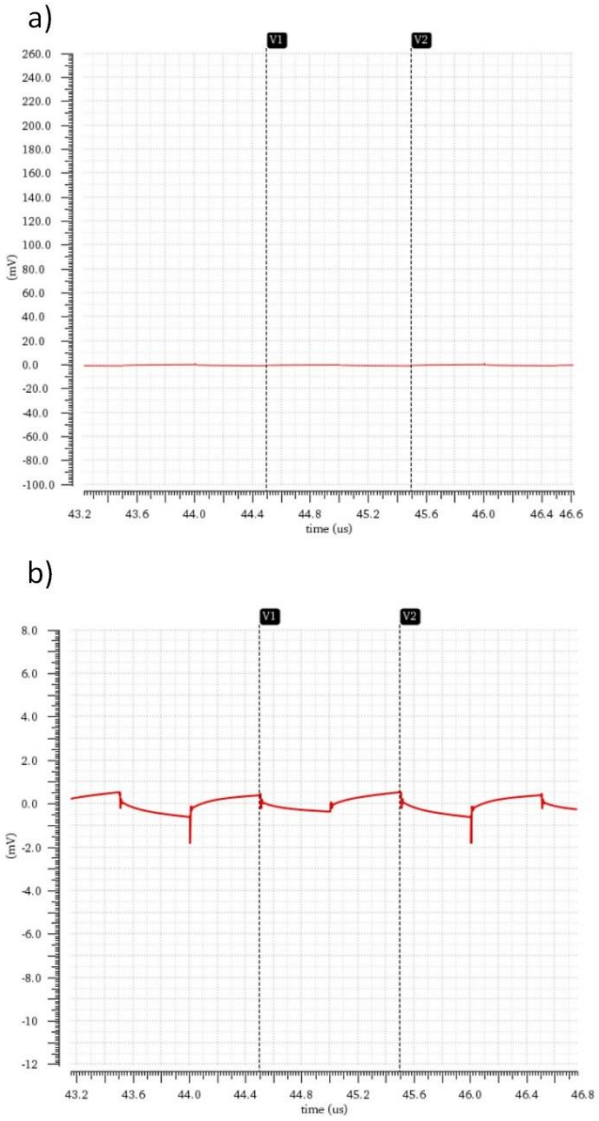

Figure 9: a) Simulation result at the output of the charge amplifier with RRL and with Cads is 0. b) The second graph is a zoom of the first graph in y direction.

The ripple reduction loop (RRL) reduces the ripple voltage by at least a factor of 100, which is the main reason why the RRL is indispensable in our system on a chip. Table 1 shows the different voltage ripples and differential output voltages when changing the values of cads without RRL and with RRL. It can be seen from Table 1 that RRL effectively suppresses the ripple voltage caused by the offset voltage of a gm1 cell.

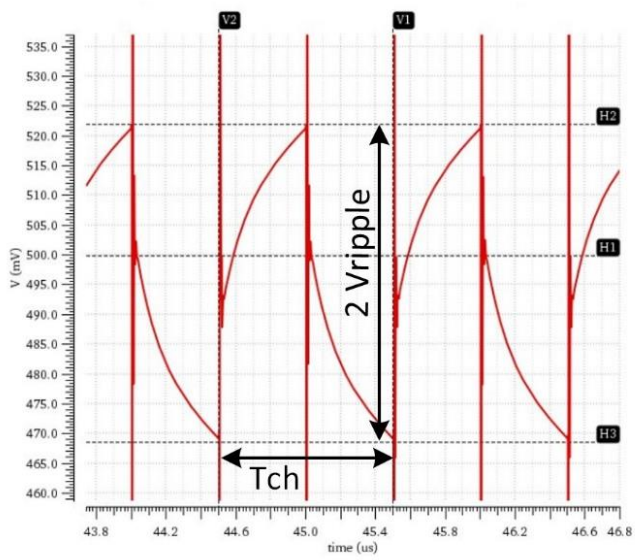

Figure 10: Differential signal at outputs of the charge amplifier without RRL and Cads is set to 100fF.

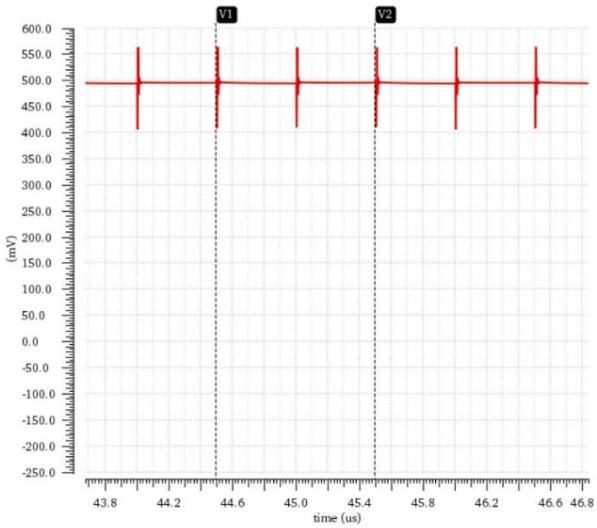

Figure 11: Simulation result at outputs of the charge amplifier with RRL and Cads is set to 100fF.

Table 4: Different values of Cads without and with RRL.

	Cads	RRL	Vripple	Vdiff
1.	0fF	No	0.02608V	0V
2.	100fF	No	0.02634V	0,52V
3.	0fF	Yes	0.00038V	0V
4.	100fF	Yes	0.0003V	0,49V

If we compare the above results with the results from article [8], we find that our system without including RRL has a 10x lower output ripple voltage (Vripple). That means that if we suppress the output ripple voltage by 100x with added RRL, we are left with output ripple voltage in the order of microvolts.

In last decade, a lot of work has been done in field of offset compensation. Article [8] presents a low-power precision instrumentation amplifier for use in wireless sensor nodes with ripple reduction loop, positive feedback loop and DC servo loop. Chip was fabricated in 65nm technology with fixed gain of 100 and BW in Hz, with low supply voltage (1V) and current (1.8uA). They achieve reduction of output ripple by 1000x. The article [12] proposes the use of a so-called fill-in technique to eliminate IMD pulses in chopper amplifiers that is caused by the interaction between the input signal and the chopper clock. The chip was made in 180nm BCD process with 5V supply voltage and 0.55mA with GBW of 4.2MHz with fin of 79kHz. Reported results for fin = 79kHz with fill-in technique is -125.9dB at 1kHz. Article [13] describes amplifier for electroretinography (ERG) and new method dynamic offset zeroing for reduction of large unwanted ripple. The chip was fabricated in 0.18um technology, with supply volage of (0.5 -1.8) V with 7uA supply current. The gain of the system is 60dB and BW of 300Hz. The reported residual ripple in rms is 6mV.

The comparison of results from the literature with our own circuit is difficult, since we try to measure extremely small capacitive changes, while in other work different quantities are measured. However, comparing the remaining ripple of our circuit with the work of [8] shows that, the remaining ripples are similar. Furthermore, the circuitry described in [8] and [13] have smaller bandwidth, compered to ours. The article [12] talks about suppression of CH-induced unwonted IMD tone at a certain frequency, depending on input signal frequency and con not be directly compered with our system.
Our system measures extremely small differential capacitive changes with sensitivity in a range of zF/√Hz with programmable bandwidth in a range of several 100kHz. We think that our simulation results shows that we constructed good system with suppressed ripple by factor of 100x, which means that we are left with less than 0.3mV ripple at the output. This motivates us for future research and system improvements.

5 Conclusions

In this paper, we present the first steps towards building a precision artificial nose detection system comprising 256 differential capacitive pairs and complete front-end electronics for all channels on a single ASIC. The presented topology of capacitive sensors and chopper amplifier with a proposed new topology for differential capacitive sensors is the main contribution. However, the topology requires further optimization.
Other performance parameters need to be addressed and carefully simulated. One of them is the noise characteristics, which directly affect the detection capability and tell us how sensitive our detection system can be and how close the real detection limit is to the theoretical calculation from Section 3. We will also perform

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other simulations and analysis of the existing topology, including frequency domain simulations, CMRR, PSRR, gain accuracy, etc. We intend to continue work on building an even more complex topology which includes AD conversion. Furthermore, we will compare the simulation results with experimental data in future studies.

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