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Design and Efficiency Enhancement of Polar Encoder Based on Universal Logic Gates Utilizing QCA Technology

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Abstract: Nano-scale circuit designs can be implemented using a transistor-free method called Quantum-dot Cellular Automata (QCA). QCA circuits are denser, quicker, and need less energy than the commonly used transistor-based technologies. In QCA technology, like in many other technologies, it is crucial to send and receive information securely. The QCA-based polar encoder circuit is one of the circuits that makes this possible. There are some drawbacks to the polar encoders circuit in QCA technology, and a strong design with high speed and low cell count is also strongly required. This paper presents three new and largely used circuits for QCA-based polar encoders. The G2 (2-bit) design is a single-layer structure with 16 cells only and a total area of 0.02 μm2, while its delay is 0.5 clock cycles. A suggested G4 design would be 121 cells, requiring a total size of 0.16 μm2 with a delay of 1.50 clock cycles. The G8 design has a delay of 3.5 clock cycles at a total size of 0.8 μm2 with 564 cells. All designs are simulated using QCADesigner. The tests and the simulations prove the supremacy of the proposed circuits over the best previous circuits in terms of speed, number of cells, and space used for implementation.

Keywords: Polar Encoder, Quantum-Dot, Cellular Automata, QCADesigner, Nano Communication. Nano Electronic.

Oblikovanje in povečanje učinkovitosti polarnega dekodirnika na osnovi univerzalnih logičnih vrat z uporabo tehnologije QCA

Izvleček: Zasnove vezij v nanometrskem merilu je mogoče izvesti z metodo brez tranzistorjev, imenovano kvantni celični avtomati (QCA). Vezja QCA so gostejša, hitrejša in potrebujejo manj energije kot običajno uporabljene tehnologije, ki temeljijo na tranzistorjih. Pri tehnologiji QCA je tako kot pri številnih drugih tehnologijah ključnega pomena varno pošiljanje in sprejemanje informacij. Polarno kodirno vezje, ki temelji na QCA, je eno od vezij, ki to omogoča. Vezje polarnih kodirnikov v QCA-tehnologiji ima nekaj pomanjkljivosti ter potrebuje močno zasnovo z visoko hitrostjo in majhnim številom celic. V tem članku so predstavljena tri nova in večinoma uporabljena vezja za polarne kodirnike, ki temeljijo na QCA. Zasnova G2 (2-bitna) je enoplastna struktura s 16 celicami in skupno površino 0,02 μm2, njena zakasnitev pa je 0,5 takta. Predlagana zasnova G4 bi imela 121 celic, za kar bi potrebovali skupno površino 0,16 μm2 , zakasnitev pa bi bila 1,50 takta. Zasnova G8 ima zakasnitev 3,5 takta pri skupni velikosti 0,8 μm2 in 564 celicami. Vse zasnove so simulirane s programom QCADesigner. Testi in simulacije dokazujejo premoč predlaganih vezij nad najboljšimi predhodnimi vezji glede hitrosti, števila celic in prostora, porabljenega za izvedbo.

Ključne besede: polarni kodirnik, kvantne točke, mobilni avtomat, QCADesigner, nano povezljivost, nanoelektronski

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1 Introduction

Broadly, research has been the hallmark of years gone by in finding a proper alternative to transistor-based technologies [1-3]. Because transistor-based technologies have reached their physical limit, they result in many pathologies, such as short-channel effects,

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design variance, and heat. One of the most promising alternatives is Quantum-dot Cellular Automata (*QCA*) technology [4, 5]. These are due to the remarkable features and benefits of QCA, such as rapid switch speed, operation frequency in the terahertz rate, high device density, and low power dissipation [6, 7]. It is because of the fantastic characteristics and advantages of QCA, including its rapid switch speed, terahertz operating frequency, extremely high device density, and very low power dissipation [7, 8]. A number of different implementations, including atoms, molecules, and semiconductors that have been studied based on electrostatic interactions, have been proposed to replicate bistable and local QCA paradigm interactions. In addition, several experimental gadgets have been built and successfully tested [9]. Due to the novelty of this technology, many researchers have presented different designs for different circuits, such as encoder circuits, adders, calculating units, subtractors, and polar code circuits [10]. Polar codes significantly reduce block error probability, with an asymptotic error exponent upper bound. However, the number of studies on polar encoders is rare, and there is a need to design faster circuits with fewer cells and optimal space consumption [11]. Polar encoders are relatively new, having been first introduced in *2009* by *E. Arikan [12]*. A polar encoder is one that has *K* inputs and *N* outputs (*N,K*). Its fundamental premise is channel polarization to separate the noiseless channel from the noisy channels [12].

In QCA technology, the role of a polar encoder has not been taken so serious, and there was a need to present new circuits that realize the issue of a polar encoder as a critical aspect of this technology [13]. Ensuring reliable data transmission and securing the information of the users are very crucial. This demands presenting the function of a polar encoder in this technology. QCA technology will be able to increase its potential in establishing a safe transfer of data so that the important information of the users can be protected by highlighting the design of new circuits and appreciating the worth of this topic. A polar encoder is to be designed in order to meet the growing demand of reliable data transmission and strong protection of information in QCA technology. It means that with respect to QCA technology, there are problems in the polar encoder circuit, data transfer, and reliable information protection; apparently, what is demanded is sturdy designs at fast speeds and few cells. In such a paper, the authors have proposed low-cell QCA-based polar encoder circuit architecture at the nano-scale level. The designs are simple, adaptable, and realized in a single layer. The primary structural component of the circuit is the majority gate. The suggested circuits are built and tested using *QCADesigner-E*, a program for modeling QCA circuits. The important contributions are as follows:

I. Offering the designs of single layer *2-bit, 4-bit, and 8-bit* polar encoders in QCA;
II. Assessing the size, latency, cell counts, and logic gate counts of suggested circuits;
III. Evaluating the quantum cost and energy dissipation of suggested circuits.

As a result, a novel polar encoder circuit design and implementation were given in the current research. Section 2 gives an overview of earlier efforts as well as the history of QCA. Section 3 presents the suggested polar encoder circuit's design, implementation, and simulation results. Section 4 provides comparison and evaluation charts and tables for significant QCA parameters, and Section 5 presents this article's conclusions.

2 Backgrounds and related work

2.1 Preliminaries for QCA

Recently, nano-designs have gotten much attention in many fields [14-16]. QCA provides a new idea in nano-scale. The most fundamental unit of a QCA component is a cell. In a cell, there are two free electrons and four free quantum dots. Two free electrons are allowed to travel freely amongst the four quantum dots and, through electrostatic interaction, can achieve two stable states [17]. The binary *"1"* and binary *"0"* can be represented by the two stable states. Figure 1 depicts the fundamental components of the QCA technology [18]. Normal cells and rotated cells are two categories of QCA cells. The 2 stable states of QCA cells are shown in Figure 1 (a).). Each cell in a mathematical sense can be described by polarization *P*, whereby (Here *p1, p2, p3, and p4* will be the probabilities of the electron across the dots.):

$$p = \frac{(p1 + p3) - (p2 + p4)}{(p1 + p2 + p3 + p4)} \quad (1)$$

Figure 1 (b) shows a three-input majority gate, and Figure 1 (c) depicts an inverter [11]. The inverter can reverse an input signal, whereas the 3-input majority gate can produce an output based on majority rules [19]. We are aware of four different QCA models. There are numerous theories for each of the four schemes. Both magnetic and molecular QCA cells can operate steadily at room temperature [20]. The majority gate is regarded as the basic logic gate in QCA, defined by the function:

$$\text{Majority}(Input_1, Input_2, Input_3) = (Input_1 \times Input_2) + (Input_1 \times Input_3) + (Input_2 \times Input_3) \quad (2)$$

This function provides the majority value of between inputs $Input_1$, $Input_2$, and $Input_3$. The inverter is a simple gate that makes an inversion of the input state:

$$Inverter\ (IN) = (\overline{Out}) \quad (3)$$

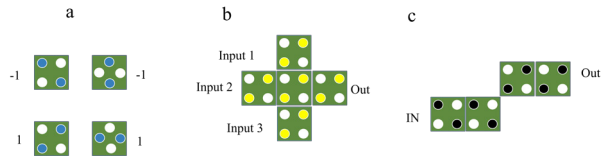

Figure 1: QCA Assemblies; (a) primary cells, (b) majority gate, (c) inverter gate.

The architecture of the QCA circuit heavily relies on the QCA clock mechanism. First off, it supplies the required power to QCA circuits [21]. Second, it aids in data transmission pipelining. In QCA, there are four clock zones (*Zones 0-3*), each of which is driven by a four-phase clock signal [22]. Each clock zone has one of four phase states, including *Switch, Hold, Release, and Relax*, using ($\pi/2$) phase-shifted signals. The *Switch* state marks the start of computation, whereas the *Hold* state maintains polarization. The QCA cell is ready for the following computation during the *Release and Relax* stages [17].

2.1 Related works

In this section, important encoder circuits in QCA technology are examined.

Salimzadeh, et al. [23] proposed the design and implementation of a fault-tolerant priority encoder. In this study, a fault-tolerant priority encoder was designed, with a primary focus on providing a new fault-tolerant majority gate. Simulations were conducted using the QCADesigner software *V. 2.0.3*, revealing improved performance of the proposed structure. The problem with this method is the use of many cells and its low speed.

Also, Safoev, et al. [24] proposed a QCA-based priority encoder using the Toffoli gate. In the paper, it is suggested that a reversible priority encoder be designed, which has played a key role in addressing encoding and decoding processes. This research pays attention to QCA technology as a new technology for implementing reversible priority encoder circuits. This paper presents a new architecture for a reversible encoder. A low-cost design for the Toffoli gate is presented to facilitate the implementation of the proposed reversible encoder circuit. The circuit has been tested with the QCADesigner simulation tool. The result shows it to have a correct operation. However, the problem in this circuit is using the Toffoli gate since this gate is an old gate with a low speed for generating the output.

Das and De [25] provided a QCA-based circuit for a polar encoder. Using a bottom-up approach, they designed a QCA-based polar encoder circuit that consumes low power at the nano-scale level. They also explored the impact of stuck-at-fault errors on generating valid polar codes and proposed test vectors to ensure proper circuit implementation. Notably, the proposed circuit boasts low energy dissipation, fast circuit latency, and a small device area. The results confirmed the circuit's accuracy. However, this design suffers from inadequate performance and excessive cell usage.

Finally, Ahmed, et al. [26] proposed a design of a QCA-based cost-efficient polar encoder. The use of polar encoders in secure communication was discussed extensively in this article, leading to the creation of a polar encoder utilizing QCA technology. This encoder had an area of *0.1944* μm^2 on one layer and contained *600* cells. The total area for implementing this circuit was *0.7225* μm^2. Due to the large number of cells, and also very high hardware implementation space, this design cannot be used practically, and the unavailability of easy access to the inputs and outputs is one of the important limitations of this circuit.

3 Polar encoder design

The polar encoder represents a variety of fault correction codes in communication systems that increase the reliability of data transmission. These codes are of great importance and a must due to their tremendous superiority in transferring data without faults and their performance superiority compared with other methods. In the polar encoder method of data encryption, information is divided into several blocks that are then mapped to a set of binary symbols. This set of symbols then combines the data with varying levels of confidence [27]. Finally, the data is transmitted through communication channels, and after receiving the information, the receiver extracts and sorts the data using a polar decoder. These codes increase speed, reduce complexity, and provide better security in public communication channels. In general, it can be supposed that polar encoders and decoders are very promising solutions for safe communications at the nano level and in complex circuits, and with new designs, their use will increase.

Figure 2 shows the schematic or block diagram of a polar decoder and encoder for communication at the nano level. The schematic diagram includes various sections such as input and output values, communication channel, polar decoder section, and polar encoder section. In this schematic, to create a polar encoder, several *GN* bits are selected as information input, and the rest of the inputs remain fixed. The frozen bits can

be assigned a value of either *"1" or "0"*, but usually, they are fixed at *"0"*.

A straightforward recursive rule defines G_N. G_2 is created initially, then G_4 is formed by concatenating G_2 units, and G_8 is constructed by concatenating G_2 and G_4 units. To construct G_2N, N copies of G_2 and two copies of G_N are utilized. The *XOR* gate is the fundamental building block of polar encoder structures, specifically G_2, G_4, and G_8. G_2 requires only one *XOR* gate to produce the output, which has two inputs and two outputs. Table 1 presents the truth table for this gate. The design of G_2 in QCA is shown in Figure 3, and it is created and simulated in the *QCADesigner* tool. The design is a single-layer structure with only *16* cells and a total area of *0.02 μm²*, and it has a latency of *0.5 clock cycles*.

Table 1: The truth table for QCA-based G2 circuit

I_1	I_2	O_1	O_2
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	1

The implemented G_2 circuit is used to create the G_4 circuit and this circuit is shown in Figure 4. This circuit uses 121 quantum cells in an area of 0.16 μm² and has a latency of 1.50 clock cycles. It is also worth mentioning that this circuit has *4 inputs* and *4 outputs*. As shown in Figure 5, the G_8 circuit has *8 inputs and 8 outputs* and is implemented by combining *4, G2* circuits and *2, G4* circuits. Also, according to Figure 6, the G_8 circuit is designed and implemented in one layer based on QCA technology and has accessible and convenient inputs and outputs. With a total of *564* cells, the proposed design occupies a total area of *0.8* μm² and has a latency of *3.5 clock cycles*.

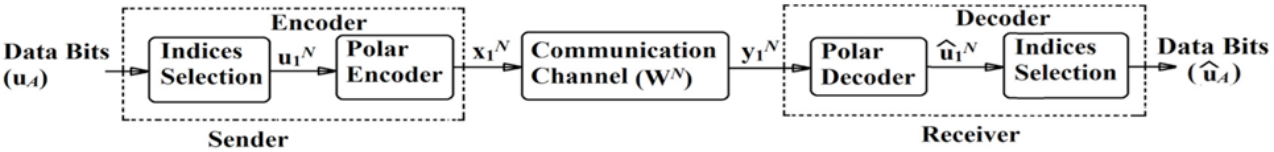

Figure 2: Data communication with Polar encoder [26]

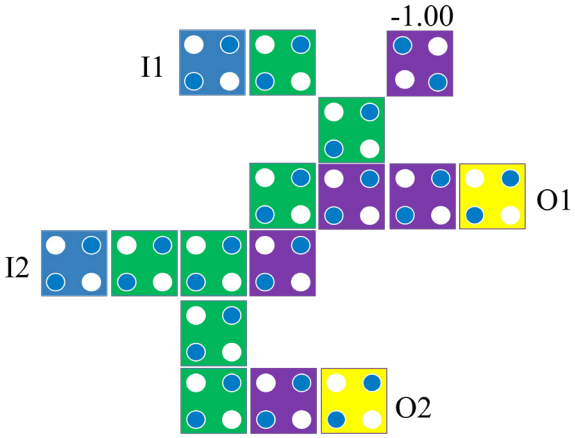

Figure 3: The proposed QCA design for the G_2 circuit

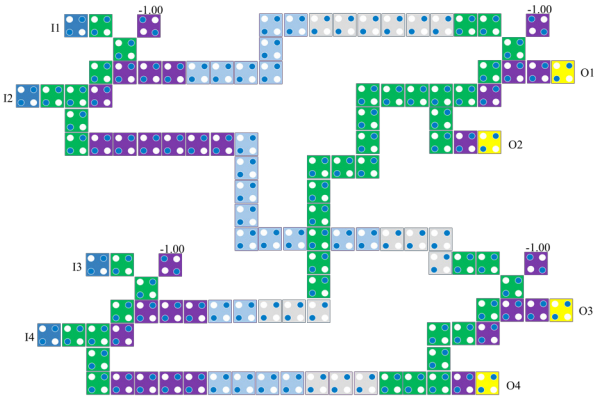

Figure 4: The proposed QCA-based G_4 circuit

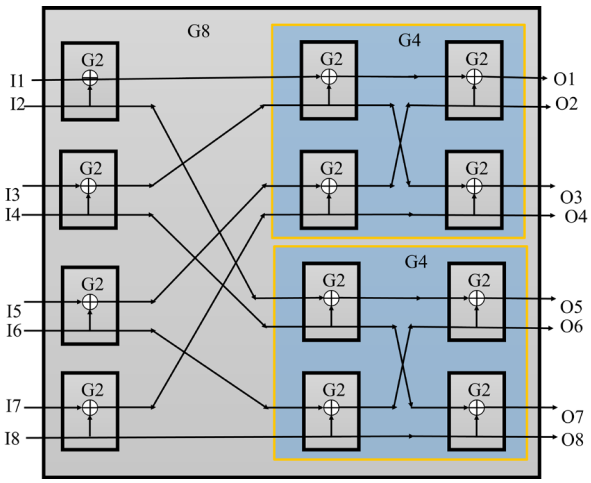

Figure 5: The applied G_8 block diagram

The (*8,4*) polar encoder has the same structure as G_8, but I_1, I_2, I_3, *and* I_5 are held at logic *"0"* as frozen bits. Figure 7 illustrates the QCA layout for this structure, and its performance parameters are identical to those of the G_8 structure. Consequently, this configuration includes four information bits (I_4, I_6, I_7, *and* I_8) and eight output bits. The design consists of a total of *560* cells, occupies an area of *0.8 μm²*, and has a latency of *3.5 clock cycles*.

The G_2 polar encoder circuit with QCA uses the least number of cells implementing a *XOR* gate that is necessary in

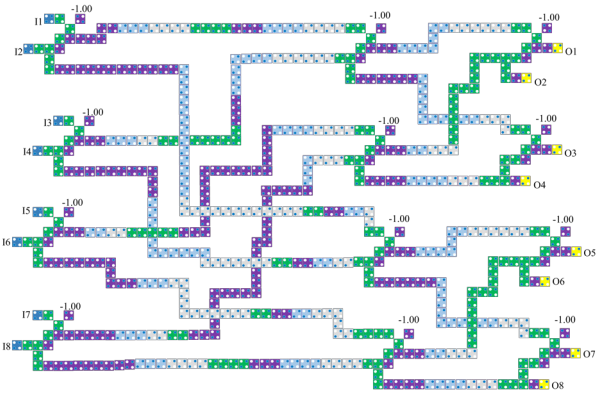

Figure 6: The proposed QCA implementation of G_8

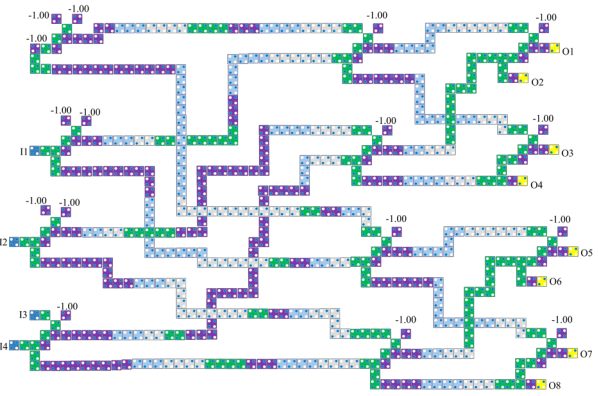

Figure 7: The proposed QCA implementation of the proposed (8, 4) polar encoder

encoding operations. The output of the G_2 polar encoder circuit can thus be expressed for this *XOR* gate as:

$$XOR(I_1,1_2)=I_1 \oplus I_2 \quad (4)$$

The G_4 *and* G_8 circuits are cascaded from the basic G_2 units. For the output in case of G_4, it can be given by:

$$G_4(I_1, I_2, I_3, \text{and } I_4) = XOR(XOR(I_1,1_2), XOR(I_3,1_4)) \quad (5)$$

The G_8 circuit extends this approach, with four G_2 circuits and two G_4 circuits:

$$G_8(I_1, I_2, I_3, I_4, I_5, I_6, I_7, \text{and } I_8) = \\ = XOR(G_4(I_1, I_2, I_3, \text{and } I_4), G4(I_5, I_6, I_7, \text{and } I_8)) \quad (6)$$

4 Discussions

The coherence vector and bistable vector characteristics are utilized in the simulation using the QCADesigner [18]. As described in [4], the simulation considers various parameters for coherence vector-based analysis:

1. Cell height and width: 18nm
2. Operating temperature: *1 K*
3. Relaxation time: *1.00e-015* s
4. Time step: *1.00e-016* s
5. Total simulation time: *7.00e-011* s
6. High clock: *9.80e-22J*
7. Low clock: *3.80e-23J*
8. The clock's amplitude factor: *2.0000*
9. Permittivity relative: *12.900*
10. The impact radius: *80 nm*
11. Layer separation: *11.5 nm*

Figure 8 displays the simulation waveform, which enables effortless verification of the structure's functionality. Take, for instance, the scenario where I_1 has a value of *0* and I_2 has a value of 1. Under these conditions, the outputs will be $O_1 = 1$ *and* $O_2 = 1$, with a delay of *0.5 clock cycles*. This outcome can be cross-checked with the information in Table 1. The simulation waveform facilitates the equal ease of verification of all input and output combinations.

Figure 9 illustrates the simulation waveform, which can be used to examine the simulation results. Suppose inputs I_1, I_2, I_3, *and* I_4 have values of 1, *0, 0, and 1*, respectively. In that case, the outputs will be $O_1 = 0$, $O_2 = 1$, $O_3 = 1$, *and* $O_4 = 1$. The same combination of outputs can be seen in the simulation waveform depicted in Figure 9. The output is generated with a latency of 1.*5 clock cycles*. All the input and output combinations can be validated similarly using the simulation waveform.

Figures 10 and 11 depict simulation waveforms for the proposed G_8 and polar encoder, respectively. The simulation results include all possible inputs for both the execution circuit and the expected output, demonstrating the circuits' accuracy. Likewise, by examining the simulation waveform, all input and output combinations are confirmed.

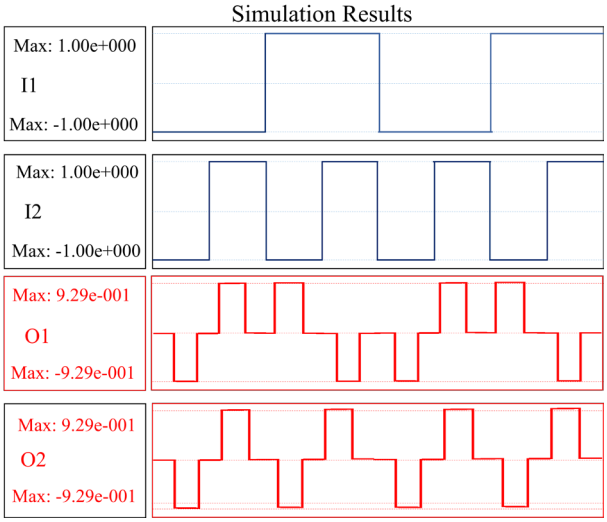

Figure 8: The simulation results of G_2 design

Table 2 provides a complete comparison of the proposed circuits and the best previous circuits in terms of cell count, area, and delay. The G_2 circuit of the new implementation has 16 cells with an area of 0.02 μm² and produces the final output after 0.5 clock cycles. Also, the G4 circuit of the new implementation has 121 cells with an area of 0.16 μm² and produces the final output after 1.5 clock cycles. It should be noted that the G8 circuit has 564 cells with an area of 0.8 μm² and produces the final output after 3.5 clock cycles. Finally, the (8,4) polar encoder circuit has 560 quantum cells and is implemented in the space of 0.8 μm2. According to the values of Table 2 and also the complete Figure 12, it can be seen that the circuits provided in all compared cases have provided the best performance and results.

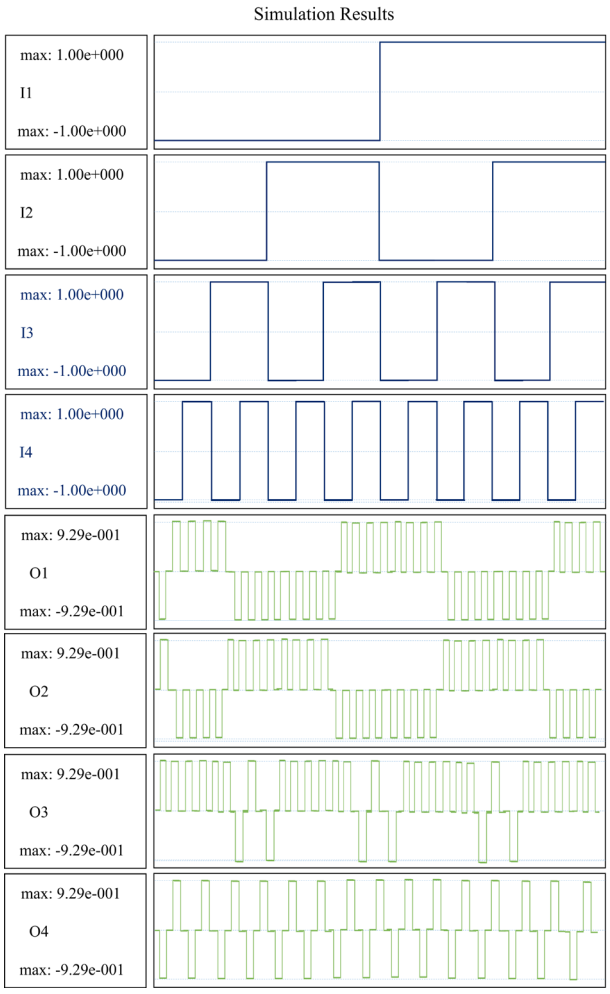

Figure 9: The simulation results of G_4 design

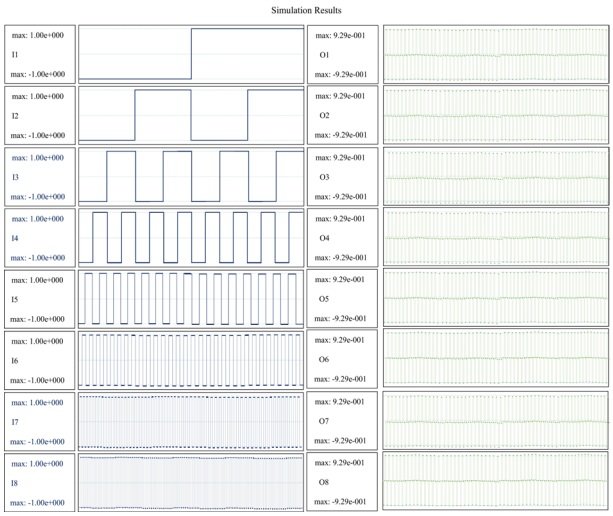

Figure 10: The simulation results for QCA-based G_8 circuit

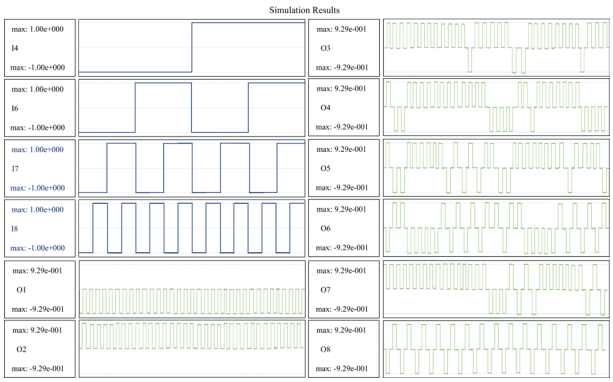

Figure 11: The simulation outcomes of QCA-based polar encoder

Table 2: Comparison between the proposed design and other state-of-the-arts

Designs	Area (μm²)	Cells	Latency
Proposed G_2	0.02	16	0.5
Proposed G_4	0.16	121	1.5
Proposed G_8	0.8	564	3.5
Proposed G $(_{8,4})$	0.8	560	3.5
Ahmed, et al. [26] G_2	0.016	21	0.5
Ahmed, et al. [26] G_4	0.132	133	1.75
Ahmed, et al. [26] G_8	0.7225	600	3.75
Ahmed, et al. [26] $(_{8,4})$	0.7255	600	3.75
Das and De [25] G_2	0.077	69	1.25
Das and De [25] G_{45}	0.456	322	3.25
Das and De [25] G_8	1.915	1188	6.25
Das and De [25] $(_{8,4})$	1.915	1188	6.25

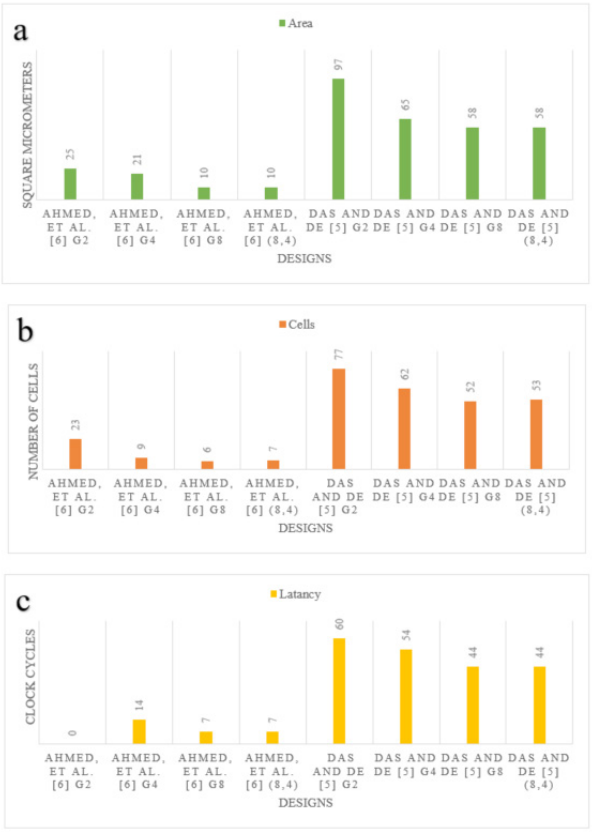

Figure 12: Chart of percentage improvement and comparison of QCA-based polar designs. (a) area, (b) number of cells, and (c) delay.

5 Conclusion

Emerging nanotechnology, known as *QCA,* has several noteworthy benefits, including reduced power dissipation, increased circuit density, and quicker speed. This technology offers increased component density, faster processing, and less latency with reduced power consumption. As a result, QCA technology is a wise option for nano-scale computing. It has also been determined that QCA is suitable for constructing various nano-communication devices and circuits. An essential and integral component of the QCA logic circuit family is communication. However, for producing secure communications, the polar encoding circuit is quite popular and frequently utilized. This circuit can improve data transmission efficiency and accuracy, opening up new possibilities for environmental monitoring and medical engineering applications. As a result, circuits for *2, 4, and 8* polar encoders have been devised and implemented in the paper. Only *16* cells, covering *0.02 μm²*, and a delay of 0.5 clock cycles were utilized in the G2 circuit; *121* cells, covering *0.16 μm²*, and a latency of *1.50 clock cycles* were employed in the G4 circuit. In addition, the suggested G_8 circuit has a delay of *3.5 clock cycles*, *564* cells, and an area of *0.8 μm²*. Lastly, the *0.8 μm²* size, *3.5 clock cycle* delay, and *560* cells were employed in the suggested (*8,4*) polar encoder design. QCADesigner *version 2.0.3* software was used to implement these new circuits and compare them to the best existing circuits. The results showed the superiority of the circuits presented in cell count, area, and latency compared to the most recent circuits. Future works utilizing the concepts provided here might involve implementing bigger, more bit-intensive circuits through the use of QCA-based polar encoders and decoders, as well as more optimum circuit construction.

Data Availability: *The article contains all the data.*

Conflict of interest: *No conflict of interest is found amongst the authors.*

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