Original scientific paper
https://doi.org/10.33180/InfMIDEM2025.101

Informacije MIDEM
Journal of Microelectronics,
Electronic Components and Materials
Vol. 55, No. 1(2025), 3 – 23

Challenges for Large-Scale Deployment of WBG in Power Electronics

Henrik Lavrič, Peter Zajec, Klemen Drobnič, Andraž Rihar, Vanja Ambrožič, Danjel Vončina, Mitja Nemec

Fakulteta za elektrotehniko, Univerza v Ljubljani, Ljubljana, Slovenia

Abstract: As the demand for efficient and high-performance power electronic devices continues to grow, wide bandgap (WBG) semiconductors have emerged as a promising solution due to their superior characteristics. However, realizing their full potential requires not only the development of advanced semiconductor materials but also the optimization of packaging techniques. This paper examines the crucial role of packaging in leveraging the benefits of WBG devices, with a particular focus on mitigating inductance and addressing other critical concerns. Drawing from previous research and discussions, we explore various strategies to minimize inductance effects, enhance thermal management, ensure reliability, and optimize electrical performance. Through an interdisciplinary approach that encompasses electrical engineering, materials science, and mechanical engineering principles, this paper highlights the latest advancements in WBG device packaging, providing valuable insights for researchers and engineers working towards more efficient and reliable power electronic systems.

Keywords: wide bandgap; semiconductors; power electronics; packaging; design

Polprevodniki s širokim prepovedanim pasom v pretvornikih močnostne elektronike

Izvleček: Ob nenehno naraščajočem povpraševanju po učinkovitih in visokozmogljivih napravah močnostne elektronike, se polprevodniki s širokim prepovedanim pasom (WBG) zaradi svojih izjemnih karakteristik kažejo kot obetavna rešitev. Uresničitev njihovega polnega potenciala poleg razvoja naprednih polprevodniških materialov zahteva tudi optimizacijo tehnik načrtovanja in pakiranja. Članek predstavi ključno vlogo načrtovanja pri izkoriščanju prednosti WBG naprav, s posebnim poudarkom na zmanjševanju induktivnosti in obravnavanju drugih ključnih vprašanj. Na podlagi prejšnjih raziskav in razprav raziskuje različne strategije za zmanjšanje učinkov parazitnih parametrov, izboljšanje odvoda toplote izgubnih moči, zagotavljanje zanesljivosti in optimizacijo električnih zmogljivosti. S pomočjo interdisciplinarnega pristopa, ki zajema načela elektrotehnike, materialov in strojništva, članek poudarja najnovejši napredek pri načrtovanju WBG naprav ter ponuja dragocen vpogled raziskovalcem in inženirjem, ki si prizadevajo za bolj učinkovite in zanesljive sisteme močnostne elektronike.

Ključne besede: širok prepovedan pas; polprevodniki; močnostna elektronika; pakiranje; načrtovanje

** Corresponding Author's e-mail: andraz.rihar@fe.uni-lj.si*

1 Introduction

Over the past few decades, various sectors, including aerospace, automotive, consumer electronics, industrial, and utilities, have increasingly adopted partial or complete electrification and digitization. This transition, largely driven by advancements in power electronics [1], has not only enhanced existing systems such as industrial electric drives but also facilitated the emergence of new applications, including transportation electrification and renewable energy systems.

By 2030, it is estimated that power electronics will be instrumental in processing about 80 % of global energy production and consumption, underscoring their critical role across multiple industries. Concurrently, the global power electronics market has seen substantial growth, with its value reaching approximately $20

How to cite:
H. Lavrič et al., "Challenges for Large-Scale Deployment of WBG in Power Electronics", Inf. Midem-J. Microelectron. Electron. Compon. Mater., Vol. 55, No. 1(2025), pp. 3–23

billion in 2022 (Figure 1). This market is forecasted to expand to around $32.6 billion by 2032, reflecting the increasing dependence on integration of power electronics technologies in diverse applications [2].

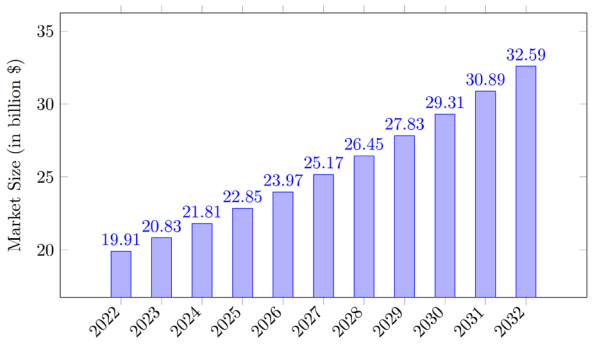


Figure 1: Projections of global market size for power electronics in $ billion. Adapted from [2].

An important shift in modern power electronics is an increasing adoption of wide bandgap (WBG) semiconductor devices [3], which offer superior performance characteristics compared to traditional silicon-based devices. WBG semiconductors, particularly silicon carbide (SiC) and gallium nitride (GaN), are pivotal in driving technological advances across various industries due to their ability to operate at higher efficiencies, frequencies, and temperatures, thus boosting reliability and enabling reduced size and higher power densities.

These improvements are especially important for applications in sectors such as renewable energy, automotive, and industry, where improved performance leads to greater energy savings and reduced environmental impact (Figure 2). The global market for WBG semiconductors is still relatively small but expected to exceed $5 billion by 2032 [4].

However, to fully realize the potential of WBG technologies, several issues must be addressed. Foremost among these is the development of robust packaging solutions capable of withstanding the increased thermal and electrical stresses present in high-performance applications [3], [5]. Additionally, the optimization of device characteristics, such as switching speeds and thermal management, is essential to reduce losses and improve the overall reliability of devices.

One of the key challenges in packaging of WBG devices is the mitigation of parasitic elements such as inductance, capacitance, and resistance. These elements can affect device performance and reliability, with inductance being particularly problematic due to its impact on switching transients, power losses, and electromagnetic interference (EMI). As operating frequencies increase, minimizing inductance is critical for harnessing the high-frequency capabilities of WBG devices.

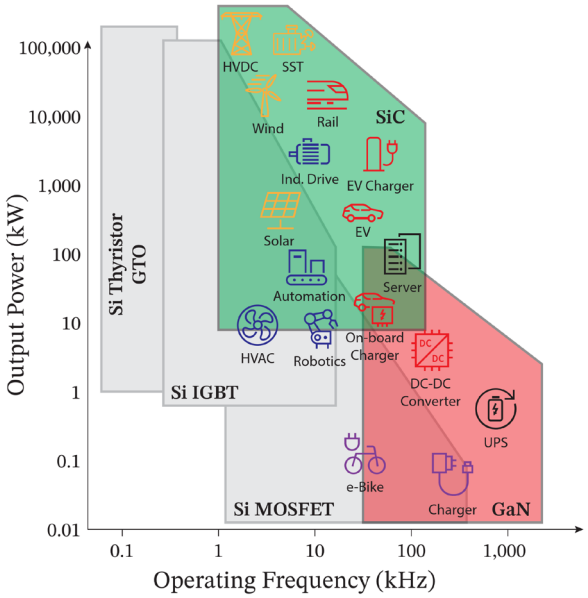


Figure 2: Typical applications with Si and WBG semiconductor switching devices, positioned according to their approximate rated values in terms of output power (kW) and operating frequency (kHz).

Moreover, the demand for compact, lightweight, and thermally efficient packaging solutions adds another layer of complexity to designing and implementing WBG device packages. Traditional packaging materials and techniques may no longer suffice to meet the stringent requirements imposed by the unique characteristics of WBG semiconductors, necessitating innovative approaches and materials to ensure optimal performance and reliability under various operating conditions.

This paper begins with an analysis of the switching phenomena in semiconductor devices (Section 2), followed by a review of WBG semiconductors including material properties, benchmarks, and benefits over silicon-based devices (Section 3). In Section 4 we discuss the effects of WBG device packaging, focusing on parasitics, thermal management, and reliability. Section 5 addresses packaging technologies for mitigation of parasitics effects, covering die attach methods, topside bonding, and innovative cooling strategies. Techniques for enhancing system performance through the integration of gate drivers, passive devices, sensors, and cooling bodies are outlined in Section 6. Section 7 details parasitics parameter estimation techniques and describes design optimization through co-simulation, as well as machine learning (ML) and artificial intelligence (AI) concepts. The paper concludes with a summary of key findings and future directions for WBG technology research in power electronics (Section 8).

2 Power electronics: why switching frequency and transition times matter

Power electronics focuses on efficient control of energy flow using semiconductor switches. Various converter topologies are employed, each designed for specific applications and performance criteria. The half-bridge topology is the most common one. This configuration typically consists of a switching leg with two serial connected power switches (Q_1 and Q_2) and either integrated or external freewheeling diodes, as illustrated in Figure 3.

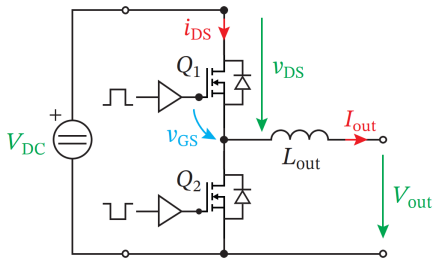


Figure 3: Switching leg with indicated input voltage/current and output voltage/current.

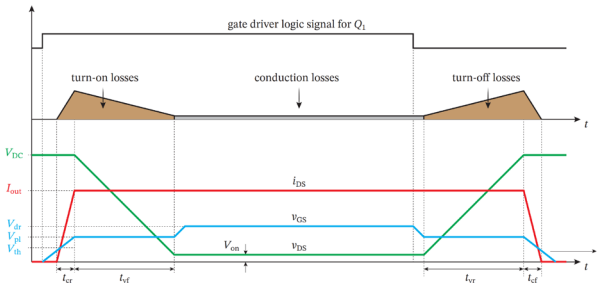


Figure 4: Simplified switching waveforms for turn-on and turn-off transitions in a half-bridge circuit for upper transistor Q_1

In a half-bridge converter, the switches Q_1 and Q_2 are usually driven complementarily using Pulse Width Modulation (PWM) logic signals, producing two distinct voltage levels at the output terminal. The converter operates with a constant input voltage V_{DC}. When Q_1 is on, the output terminal connects to the positive voltage rail; when Q_2 is on, it connects to the negative voltage rail. An output inductance L_{out} is typically included to smooth the output current I_{out}.

If output (and load) inductance is high enough we can simplify the analysis by assuming continuous output current and represent the converter as a constant current source I_{out}. Consequently, when the individual switch undergoes a state transition, a dead-time interval initiates during which the current commutates from the switch to the body diode of the opposite switch.

During the switching action (Figure 4) the transistor is transitioning from off-state to on-state, voltage across the terminals is slowly decreasing after the current increases. A comparable situation occurs when the transistor switches back to the off-state.

Switching losses P_{sw} in MOSFETs occur during these transitions. When the MOSFET is off ($V_{GS} = 0$ V), the voltage V_{DS} between the drain and source is blocked by the device, resulting in zero current ($I_{DS} = 0$ A) and no energy dissipation. Upon turning on the MOSFET, the current I_{DS} begins to increase, while V_{DS} remains constant until I_{DS} reaches its steady-state value. Subsequently, V_{DS} decreases to nearly zero, indicating the MOSFET is fully on and conduction losses commence. The instantaneous power during this transition forms a triangular profile, with the area beneath representing the energy dissipated during turn-on event. The transition time comprises the current rise t_{cr} and voltage fall t_{vf} times.

Turn-off losses are analogous to turn-on losses. In the on-state, V_{DS} is minimal, and current flows through. When turning off, V_{DS} increases while I_{DS} initially remains constant. Once V_{DS} reaches V_{DC}, I_{DS} decreases to zero. The energy dissipated during turn-off is similarly represented by the area beneath the power curve. Switching losses are a sum of turn-on and turn-off power losses that are determined by the product of the dissipated energy and the switching frequency.

Conduction losses P_{cond} in a MOSFET occur when the device is on ($V_{DS} = V_{on}$) and conducting I_{out}. The path between the drain and source acts as a resistance, denoted as $R_{DS,on}$. Thus, the conduction losses depend on the RMS current squared multiplied by the resistance and duty cycle. The losses in off-state can be ignored, as leakage current is negligible.

Thus, total power losses P_{tot} for switch Q_1 are

$$\begin{aligned} P_{tot} &= P_{sw} + P_{cond} \\ &= V_{DS} I_{DS} f_{sw} \left(\frac{t_{cr} + t_{vf}}{2} + \frac{t_{cf} + t_{vr}}{2} \right) + I_{DS}^2 R_{DS,on} D \end{aligned} \tag{1}$$

The thermal power in a converter attributed to losses must be removed by a cooling system. In most applications, the maximum output power is limited by thermal resistance (R_{th}) and the capacity of the cooling system to dissipate this heat, thereby limiting the overtemperature. Thus, the high-efficiency power switches allow for reduced cooling requirements which enables the design of devices with higher power density. Further reduction in volume and mass can be achieved by using smaller passive components such as capacitors and inductors.

Throughout periodic switching transitions, the average output voltage can be adjusted in accordance with the desired duty cycle mandated by PWM, thereby regulating the current flowing through the predominantly inductive output circuit. However, its RMS value is also subjected to the triangular waveform's superimposed AC component. Its peak-to-peak amplitude is directly influenced by the load's inductance, thereby impacting the physical dimensions of the inductor.

In the case of additional smoothing capacitors inserted behind the inductor, such as in DC/DC converters, a similar correlation between the switching frequency and the RMS current of the capacitor emerges. In both scenarios, passive elements can be significantly reduced in size (and cost) with an increase in switching frequency.

3 WBG semiconductors: material characteristics and operational benefits

WBG semiconductors have emerged as an alternative to traditional silicon due to their ability to operate more efficiently and/or to withstand higher voltage and temperature. This chapter focuses on their material properties and operational advantages. The section begins by classifying their bandgaps and detailing their physical material properties, and then discusses various benchmarking metrics. Towards the end, the chapter covers the system-level benefits of using WBG devices and provides a brief comparison of today's commercially available WBG devices, specifically SiC and GaN.

3.1 General WBG characteristics

3.1.1 Bandgap classification

The bandgap is essentially a non-existent or forbidden energy state for electrons, and its value equals the difference between the minimum energy of electrons in the conduction band and the maximum energy of electrons in the valence band. It is expressed in eV (electron-Volts) and depends on the type of material. In conventional semiconductors, the bandgap typically falls within the range of 0.6 eV to 1.5 eV. For example, germanium, silicon, and gallium arsenide have bandgaps of approximately 0.66 eV, 1.12 eV, and 1.42 eV, respectively [6]. Wide bandgap semiconductors are those with an energy gap of over 2.0 eV, including GaN and SiC, which are considered current or future alternatives to Si. In addition to wide bandgap semiconductors like GaN and SiC, the term ultrawide bandgap semiconductor applies to materials with even larger bandgaps, such as diamond and AlN [7]. These, along with Ga_2O_3, are considered by some to be the semiconductor materials of the future [8], [9].

3.1.2 Physical material properties

The most important physical properties of semiconductor materials are summarized in Table 1. The values or ranges of values in the table consist of minimum and maximum values obtained from various sources and are also to some extent conditioned by the development and progress of research over the years [8], [9], [10], [11], [12], [13], [14], [15], [16]. Some parameters are more and others less temperature-dependent [17]. For GaN technology, the upper value of electron mobility equals 2000 cm^2/Vs for the 2DEG layer [12]. This is a 2D layer of freely moving electrons (two-Dimensional Electron Gas) that forms at the interface between AlN and GaN materials due to the polar properties of the base cells of the crystal structures and the shear force at the interface between the two materials [18]. The freely moving electrons in the 2DEG layer essentially make the GaN HEMT (High Electron Mobility Transistor), a normally on transistor.

The wider bandgap leads to better electrical stability of the material at higher electrical fields and higher temperatures. WBG dies are therefore smaller compared to silicon ones, have better channel conductivity in the conduction state and enable higher switching speeds. The higher values of these two parameters are due to the easier movement of electrons through the crystal structure of the material under the influence of an electric field. The smaller dimensions of the WBG dies and consequently the smaller electrode dimensions as

Table 1: Basic material properties including minimum and maximum values from the sources [8] - [16].

	Si	4H SiC	GaN	Diamond	AlN	Unit
Bandgap E_G	1.1 - 1.12	3.25 - 3.26	3.39 - 3.44	5.46 - 5.6	6.2	eV
Critical electric field E_C	0.3 - 0.4	2.0 - 3.18	3.0 - 3.5	4.0 - 7.0	15	MV/cm
Electron mobility μ	1350 - 1500	650 - 1000	900 - 2000	1800 - 2200	450	cm^2/Vs
Hole mobility μ_H	450	90 - 120	10 - 120	1800	-	cm^2/Vs
Thermal conductivity λ	130 - 150	370 - 700	110 - 210	600 - 2300	285 - 340	W/mK
Relative permittivity ε_r	11.8	10	9.0 - 9.5	5.5	8.5	-
Electron saturation velocity v_S	1	2	2.4 - 2.5	2.3 - 2.7	1.4	10^7 cm/s

well as the slightly lower values of the relative permittivity result in small parasitic capacitances of the dies, which further accelerate the switching processes. Fast switching ensures low switching losses and the low resistance of the channel in the conductive state ensures low conduction losses. The small parasitic capacitances at the gate of the transistor also lead to low driving losses [19]. The blocking state of WBG dies is characterized by a lower leakage current, as fewer charge carriers are released due to the large bandgap. In WBG dies, there is only a very small, practically negligible (SiC) or no (GaN) reverse recovery charge, as the latter have no inherent reverse conducting diode. The lower power losses of the individual contributions lead to relatively low total power losses during device operation. The physical properties of the materials enable higher operating temperatures and better thermal conductivity, so that heat can be dissipated more efficiently.

3.1.3 Material's benchmarking

Based on certain physical parameters, various authors have derived criteria for comparing the performance or suitability of materials for specific applications, which can also be used to predict to some extent the properties of the semiconductor devices produced. Johnson's Figure of Merit (JFOM) gives a power-frequency product for low-voltage transistors. Keyes' FOM predicts the switching behaviour of transistors in integrated circuits. For power transistors, two Baliga's FOMs are of interest [20]. The first (BFOM) represents the denominator in an expression for calculating the specific resistance R_{on} of a material in the conductive state

$$R_{\text{on}} = \frac{4 \cdot V_B^2}{\varepsilon_r \cdot \mu \cdot E_C^3} = \frac{4 \cdot V_B^2}{\text{BFOM}} . \tag{2}$$

The BFOM essentially indicates the dependence of the conduction losses on the physical properties and is a measure of the performance of materials for low-frequency operation. The calculated dependencies of the specific resistances on the breakdown voltage V_B for the parameter limits of the individual materials listed in Table 1 are shown in Figure 5. The minimum values of the individual parameters were considered for the lines marked with _min (solid lines), while the maximum values were taken into account for the lines marked with _max (dashed lines). Explicitly, Figure 5 shows that the specific resistance of SiC is a hundred times or more lower than the specific resistance of Si and the specific resistance of GaN is four times or more lower than the specific resistance of SiC.

The second performance metric, BHFFOM (Baliga's High Frequency FOM), establishes the link between the physical characteristics and the ability to operate at higher frequencies, where a significant portion of the

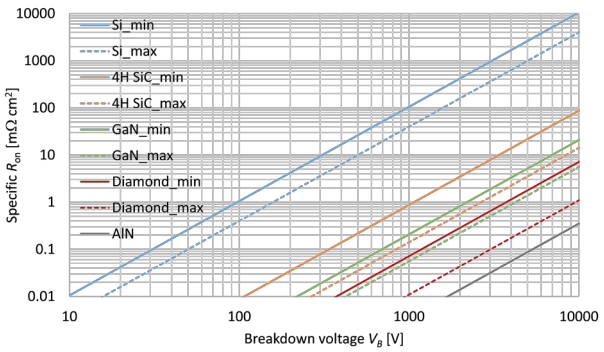


Figure 5: Specific resistances for five semiconductor materials; the calculations are based on minimum and maximum values of parameters taken from various sources.

losses are due to the charging and discharging of the specific input capacitance C_{in}. It has essentially been defined as the reciprocal of the product of specific resistance and specific input capacitance and is written with certain assumptions regarding the basic material properties [20] and the assumed control voltage at the gate of the transistor V_G

$$\text{BHFFOM} = \frac{1}{R_{\text{on}} \cdot C_{\text{in}}} = \mu \cdot E_C^2 \cdot \sqrt{\frac{V_G}{4 \cdot V_B^3}} . \tag{3}$$

The BHFFOM versus breakdown voltages for the minimal and maximal values of the individual materials listed in Table 1 are shown in Figure 6. Different V_G values were used for the calculations, namely 15 V for Si, 20 V for SiC and diamond, and 6 V for GaN and AlN. As can be seen in Figure 6, SiC has a BHFFOM value 25 times higher than Si and GaN has a value more than 40 times higher than Si.

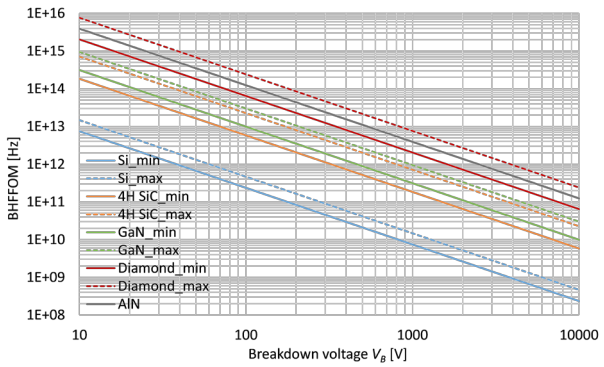


Figure 6: BHFFOM for five semiconductor materials, taking into account the minimum and maximum values of the material properties.

The total losses on the power FET can be calculated by using BHFFOM and assuming I_{rms} in the conduction direction

$$P = I_{\text{rms}}^2 \cdot \frac{R_{\text{on}}}{A} + \frac{A \cdot V_G^2}{R_{\text{on}}} \cdot \frac{f}{\text{BHFFOM}}. \quad (4)$$

The situation for the switching transistor is optimal with minimum losses, which are obtained by deriving eq. (3) on the area of A (dP/dA=0)

$$P_{\text{min}} = 2 I_{\text{rms}} V_G \cdot \sqrt{\frac{f}{\text{BHFFOM}}}. \quad (5)$$

Finally, the required minimum area of the die is determined by

$$A_{\text{min}} = I_{\text{rms}} \cdot \frac{R_{\text{on}}}{V_G} \cdot \sqrt{\frac{f}{\text{BHFFOM}}}. \quad (6)$$

The power loss ratios for the materials under consideration are shown graphically in Figure 7 and for the area ratios in Figure 8. The superiority of wide bandgap materials over Si is clear in Figure 7, but even more evident in Figure 8. It can be seen that the theoretically required active material area of the WBG dies is less than 3 % of the Si material area. In practice, the physical implementation of dies with extremely small areas is difficult due to the implementation of physical contacts and the efficient dissipation of waste heat.

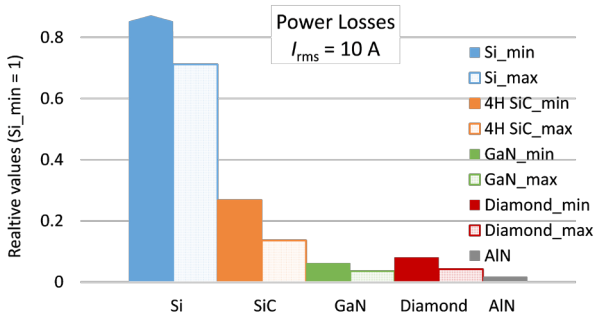


Figure 7: Power loss ratios for various semiconductor materials, taking into account minimum and maximum values of the material properties.

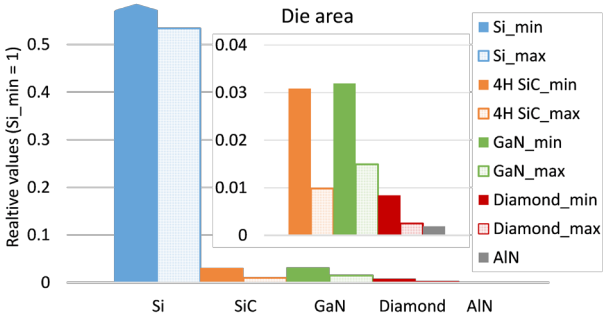


Figure 8: Die area ratios for various semiconductor materials, taking into account minimum and maximum values of the material properties.

3.2 System advantages and market overview

3.2.1 System benefits of using wbg devices

Figure 9 outlines the advantages of WBG semiconductors over traditional silicon-based devices, tracing the impact from material properties to system-level benefits. WBG semiconductors possess a low intrinsic carrier concentration and a high critical electric field, leading to beneficial device properties (Table 2), such as breakdown voltage $V_{\text{B,DSS}}$, Figure of Merit (FOM), thermal conductivity coefficient λ, gate threshold voltage $V_{\text{G,th}}$, and reverse recovery charge Q_{rr}. Low on-resistance reduces power loss during operation, while high blocking voltages improve suitability for high-power applications.

The combination of low on-resistance and high blocking voltage reduces conduction and switching losses. This enhancement not only improves device efficiency but also allows for higher switching frequencies compared to traditional silicon-based devices. Consequently, it enables the use of smaller passive filter components and cooling solutions, significantly reducing both the size and weight of the overall system. Overall, WBG semiconductors have become the first choice for high-power and high-frequency applications.

Table 2: Comparison of main characteristic parameters for Si, SiC and GaN HEMT technologies [21].

Technology	Si-MOSFET (SJ)	SiC-MOSFET	GaN HEMT Cell	Unit
$V_{\text{B,DSS}}$	> 1200	> 1200	650	V
Avalanche capability	YES	YES	NO	-
Short circuits	YES	YES	NO	-
RDS(A) FOM	10	2-3	3-7	mohm·cm^2
λ	1.5	5	1.3	W/cm^{2}K
$V_{\text{G,th}}$	3.5	2.8	1.3	V
Normalized die area	5x	1x	1.5x	-
Q_{rr}	10,000	76	~0	nC
Reverse diode effect V_{forward}	~1.5	~4	1.3-6	V

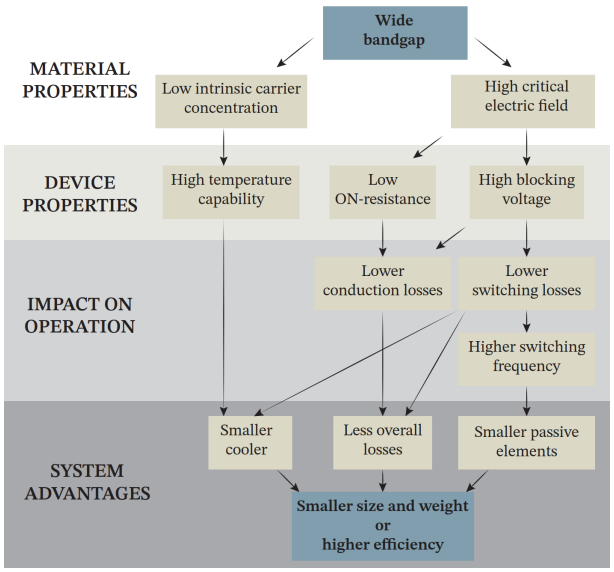


Figure 9: Impact of WBG semiconductor properties on system performance.

3.2.2 WBG market presence: SiC and GaN devices

SiC and GaN dominate the commercial market for wide bandgap (WBG) power devices, each offering distinct advantages over traditional silicon in power electronics. The commercialization of SiC devices began with the first SiC Schottky barrier diodes (SBDs) introduced to the market by Infineon in 2001 and the first SiC MOSFETs in discrete packages by Cree and Rohm in 2010–2011. SiC devices are now commercially available in the voltage class of 650–3300 V [22]. The principal benefits of SiC devices are most evident in applications within the automotive and energy sectors, where their high efficiency and high-voltage blocking capability are required.

The market introduction of GaN power devices dates back to 2010 when International Rectifier released the first GaN-based power transistor. The commercially available GaN devices are primarily classified as lateral GaN HEMTs, which have brought significant benefits to applications that demand high frequency and efficiency, particularly in RF and power supply sectors. GaN devices are currently available primarily in the voltage class of 100–650 V.

Figure 10 compares typical values of key material properties of GaN, SiC and Si. GaN devices, with their high electron mobility, inherently support much higher switching frequencies. They operate effectively at relatively high voltages due to their high critical electric field and exhibit lower leakage currents. In contrast, SiC devices have significantly higher thermal conductivity, enabling better heat dissipation. This advantage is particularly beneficial as it compensates for the relatively

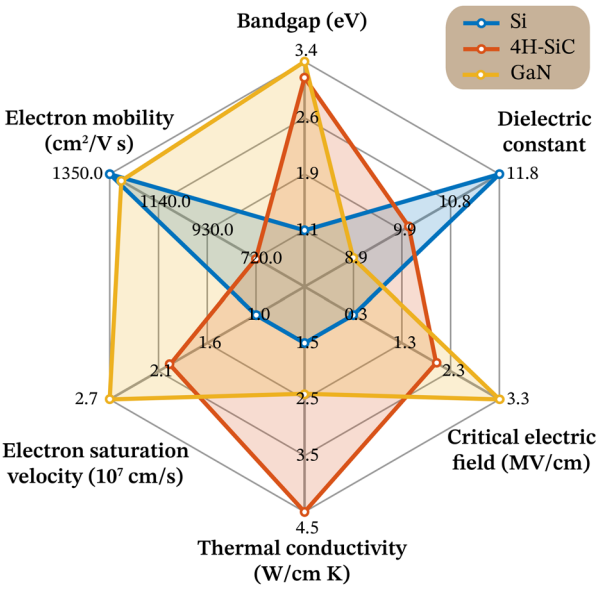


Figure 10: Graphical visualization of material characteristics using typical values for Si, SiC and GaN.

higher specific losses compared to GaN, thus improving overall system performance and reliability.

4 Packaging: electrical and thermal challenges

The use of bare semiconductor dies is uncommon due to handling and reliability concerns. Therefore, semiconductor dies are typically enclosed in various packages containing critical components, such as the semiconductor dies, substrates, baseplate, die bonding, and encapsulant (Figure 11).

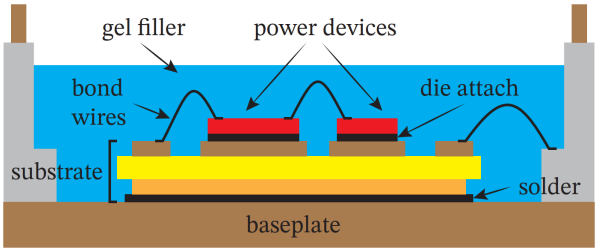


Figure 11: Mockup view of the package cross section showing the power devices (dies with die attachment and bond wires), soldered onto a baseplate. Adapted from [23].

The primary function of the baseplate is to mechanically support the substrate. This is usually a ceramic (alumina, aluminum nitride or silicon nitride) with a metallization of copper (DBC – Direct Bonded Copper) or aluminum (DBA – Direct Bonded Aluminum) on the top and bottom. The top side of the DBC is attached to

the semiconductor power die and supports heat dissipation and electrical conduction, similar to bond wires. The bottom of the DBC is soldered to the baseplate to provide a path for semiconductor chips to dissipate heat, while the core of the DBC provides electrical isolation. The power terminals, including bond wires, provide the electrical connection between the die and the external circuit.

Environmental effects have a significant impact on the performance of the power module and make protective measures necessary. In conventional packaging, an encapsulant covers the surfaces of power devices and bond wires to protect against adverse environmental conditions such as exposure to chemicals, humidity, and gases. Consequently, all elements, except the bottom side of the baseplate, are encased in a plastic covering.

4.1 Power and gate drive commutation loop parasitics

The package structure and applied materials significantly influence the electrical and thermal performance of the device. Specifically, they introduce additional stray resistance, inductance, and capacitance into the power and gate drive loops. These interact with the inherent capacitances of the semiconductor device, which are the key factors in turn-on/off switching behaviour, impacting switching losses, voltage and current oscillations, and resulting in thermal stress [24], [25]. The effect of these parasitics varies on the type of packaging used, as illustrated in Figure 12, and varies on the source contact configurations inside the package, as shown in Figure 13.

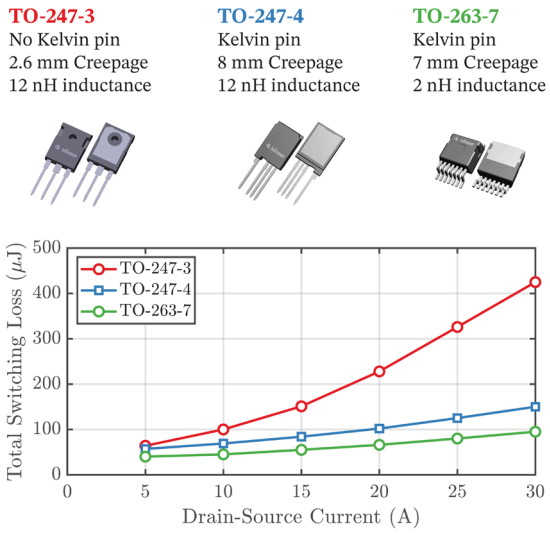


Figure 12: Comparison of parasitic inductance values and switching energy loss for different package types. Adapted from [26].

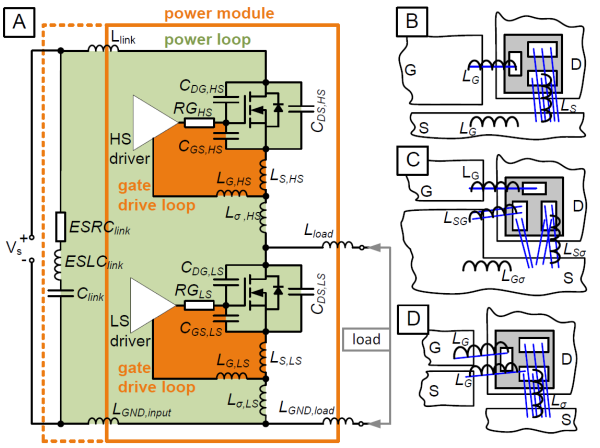


Figure 13: Equivalent circuit of a transistor leg containing structurally introduced parasitic inductances in power and gate drive loop interacting with die capacitances of the MOSFET (**A**). Subfigures (**B**)-(**D**) show various source contact configurations [27].

Furthermore, it is essential to understand that the causes leading to the deteriorated switching performance extend beyond the boundaries of the device package. They encompass all high-frequency current commutation paths (Figure 13), including components like the DC link capacitor, the interconnected traces on printed circuit boards (PCBs), as well as stray capacitances between the power and the gate drive and towards the heatsink (not depicted in Figure 13).

With the increased switching speeds of WBG devices, the circuit experiences higher induced voltages due to the inductance (L_σ). This results in drain-source voltage overshoot and significantly elevates the voltage stress on MOSFETs compared to their (Si) counterparts. Additionally, the L_σ can during the switching transients resonate with various capacitors, such as the MOSFET output capacitor and the body diode junction capacitance. This resonance can couple into the gate drive loop through the Miller capacitor, affecting the driver signal [28]. As a result, this interaction increases switching losses [23] and generates high-frequency electromagnetic interference (EMI).

4.2 Thermal aspects of packaging

In addition to electrical considerations, the design and materials used in packaging are critical for determining heat dissipation capabilities, which in turn affect the overall mechanical design of the converter. As modern WBG devices become more efficient, their physical footprint decreases. Consequently, the heat flux is concentrated over a smaller die area, and the reduced dimensions of the packaging limit heat spreading and dissipation, leading to hotspots within the device. In-

creased temperatures can also compromise the reliability of bonding, interconnections, and insulation layers.

To prevent power derating and improve power density, packaging design must address both electrical and thermal aspects simultaneously [23], [28].

5 Mitigating parasitic effects and thermal challenges in packaging

To fully leverage the advantages of WBG materials [Vecchia, 2019], which are capable of operating efficiently at high temperatures, frequencies, and voltages, traditional packaging designs used for Si-based semiconductors are no longer adequate.

Key drivers for optimizing packaging designs for power devices include:

- **High-speed switching and short current paths**: This necessitates advancements in bonding techniques such as using new materials, employing copper clips instead of wires, and adopting ribbon bonding.
- **High current carrying capability**: Achieved by integrating copper layers with thickness of up to 300 micrometers.
- **Die attachment methods**: Incorporating advanced techniques such as sintering and soldering, whether single-sided or double-sided.
- **Enhanced cooling efficiency**: Techniques such as double-side cooling, thermal vias, microchannels for liquid cooling, and the use of high thermal conductivity substrate materials (such as Al_2O_3, AlN, and Si_3N_4) [29] are crucial. Considerations also include managing the coefficient of thermal expansion (CTE) mismatch and integrating of heat-spreading materials.
- **High-temperature capability:** Ensuring reliability at temperatures exceeding 200 °C.
- **Cost-effective production**: Focusing on precision and reliability in the manufacturing processes.

The importance of these factors varies by application, such as in automotive systems or custom electronic chargers, highlighting the need for specialized packaging solutions tailored to specific voltage, current, and power requirements in different contexts.

5.1 Die attach

For silicon devices, the dies are generally attached to the substrate using lead (Pb)-based solders. These solders have lower thermal conductivity compared to the much higher thermal conductivity of WBG devices. Consequently, WBG devices are usually attached using sintering processes performed under controlled temperature and pressure conditions. Another commonly used method is transient liquid-phase bonding [30], [31]. When selecting materials, factors such as melting temperature, thermal conductivity, and CTE must be considered, as they influence performance degradation during thermal cycling.

However, many current materials and designs are not suitable for operating temperatures above 250 °C. Silver (Ag) sintering is becoming a preferred alternative due to its benefits, including lower thermal resistance

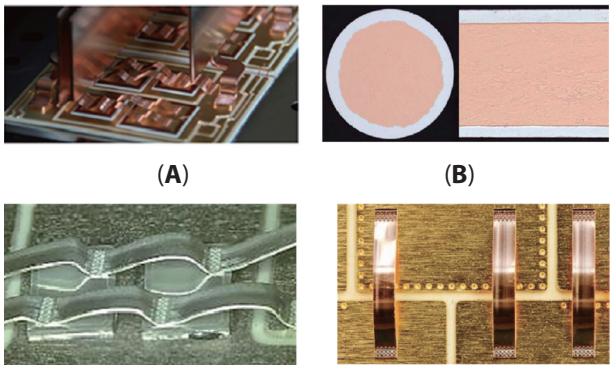
Table 3: New innovative die attach techniques for SiC [26].

Die attach technology	Thermal conductivity	Advantages	Risks
Semi Ag sinter	75-100 W/mK	- Lower R_{th} - Thinner BLT - HVM - Enables 200 °C	- Volatiles - Ag migration - New die/LF interface - Die size limitation
Full Ag sinter	150-300 W/mK	- Lower R_{th} - Better BLT control - Better surge - Higher power density - Enables 200 °C	- Ag migration - High thermo-mechanical stresses - Voiding/porosity - No HVM at assembly vendor
Cu sintering	150-250 W/mK	- Lower R_{th} - Better surge - Higher power density - Lower cost - Enables 200 °C	- Process challenges - Storage challenges
AuSn eutectic (80/20) die backside	57 W/mK	- Lower R_{th} - Thinnest BLT - Better BLT control - Non-Pb	- High thermo-mechanical stresses - Die size limitation - Voiding

(R_{th}), reduced bond line thickness (BLT), and support for higher operating temperature of up to 200 °C (Table 3). Despite these advantages, concerns about Ag migration and increased thermo-mechanical stresses remain. Pressureless Ag sintering, which uses a polymer matrix for densification is a viable option but may offer inferior R_{th} compared to pressure-assisted methods. While copper (Cu) sintering is cost-effective and provides lower R_{th}, its use is limited by the lack of a film-based format and the need for an inert atmosphere. Gold-tin (Au-Sn) eutectics offer a significant advantage with a notably reduced BLT of just 3-4 µm, compared to the more than 50 µm typical of other materials.

Mechanical stresses resulting from power and thermal cycling can lead to cracks between the substrate and die. As a result, self-healing die attachment has become a notable area of interest. However, this emerging technology is still in its developmental stages and may present risks to improving package reliability [32].

5.2 Topside-bonding



(**A**) (**B**)

(**C**) (**D**)

Figure 14: Top: wire-bonding: (**A**) Cu wire-bonding, (**B**) Cu-Al wire bonding. Bottom: Ribbon bonding: (**C**) Al ribbon, (**D**) Cu ribbon [35].

The prevalent use of conventional wire bonding in commercial SiC power module packaging is attributable to its compliance with stringent testing standards, such as successfully passing power cycle tests exceeding 20 million without failure [33], [34]. Aluminum (Al) wires, typically 20 mils in diameter, are predominantly used for wire bonding, despite their limitations on pad size and bonding throughput. Alternatives like heavy Cu wires (Figure 14 A) offer better current capacity and superior thermal conductivity compared to aluminum, as well as enhanced reliability, although they require additional processing steps such as die top system integration or plated topside Cu layers [35]. These challenges are effectively addressed by novel composite materials that combine Al and Cu (Figure 14 B), aiming to optimize bonding processes without changing chip metallization. Moreover, Al and Cu ribbon bonding (Figure 14 C, D) provide a compelling solution for higher current carrying capabilities and improved power cycling performance [31], [36].

5.2.1 Mitigating the magnetic field in the commutation loop

Traditional wire-bonding methods have inherent drawbacks, such as increased parasitic inductance and impeded power module switching speeds. Additionally, predominant material failures like bond wire lift-off and heel cracks, caused by thermomechanical stress, elevate bonding failure to a critical operational concern during power and thermal cycling. In 2002, Nexperia introduced Cu clip bonding technology (Figure 15), marking a significant advancement in power module assembly. Replacing conventional wire bonds with flat Cu clips not only reduces parasitic inductance but also improves heat dissipation from the die's surface. While this approach has been initially introduced for Si technology it has since been transfered to WBG devices [37].

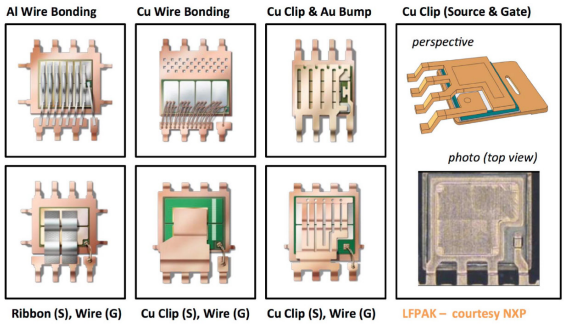


Figure 15: Example of bond-wire and clip-lead power SOP-8 leaded packages [38].

ONSEMI reported a 14 % reduction in junction-to-case thermal resistance for a single-sided PQFN package compared to its conventional wire-bonded counterpart. Nexperia's LFPAK88 package, on the other hand, boasts a source inductance that is five times smaller than that of the D2PAK package [39] (Figure 16).

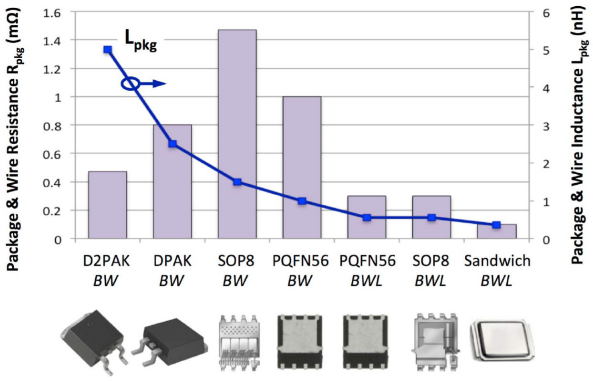


Figure 16: Power package parasitic resistance (bars) and inductance (line) [38].

In 2011, Semikron-Danfoss introduced SKiN technology, a concept designed to minimize stray inductance in their 750 V/1200 V six-pack compatible package. Instead of a solid Cu clip, they utilized a two-layer flex foil tightly positioned over the top and bottom transistors, creating three-layer current paths with minimal loop area. This approach is also employed in standard power stage modules [40], where Ag sintering is used to connect one side of the power chip to the DBC and the other to a flexible circuit board for current conduction. This design achieves remarkably low stray inductance, measuring as low as 2.5 nH per module, including overlapping terminals (DC+ and DC-, Figure 17). In comparison, the equivalent SEMITRANS module exhibits 15 nH stray inductance. The reduction in inductance in structures with close-fitting parallel traces is due to the cancellation of the magnetic field by having opposite current paths. Additionally, a separate study highlights that a significant portion of this reduction is attributable to the overlapping terminals alone. However, replacing Al material with flexible circuit boards imposes limitations on packaging reliability at high temperatures.

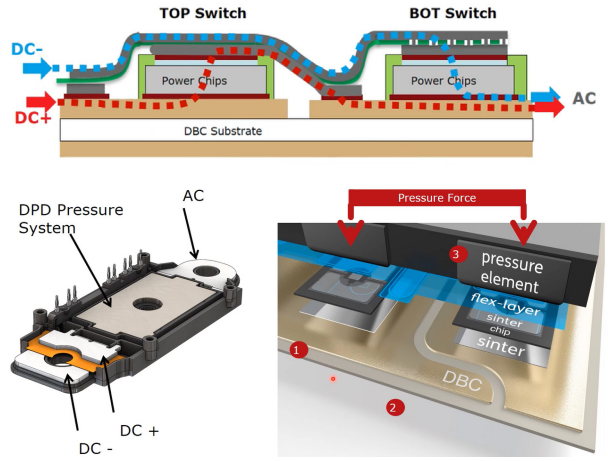


Figure 17: Concept of stray inductance reduction in eMPack package. Adapted from [41] and [42].

The design also incorporates the following features: (1) a ceramic substrate with DSS (Double-Side Sintering) sintered chips, (2) the absence of a rigid joint between the substrate and the cooler, resulting in a low thermal and mechanical stress on the substrate, and (3) a DPD (Direct Pressed Die) pressure system that flattens out cavities downward, ensuring low thermal resistance R_{th}.

5.2.2 Bonding within double-sided cooling structures

A concept similar to SKiN technology has been widely adopted across various packaging designs, with a primary focus on double-sided cooling structures. These configurations are common in high-power-density automotive applications exposed to elevated temperatures from liquid coolants. A notable example is Infineon's HybridPACK DSC (Double Sided Cooling) Power Module featuring SiC MOSFETs. Since the DSC module utilizes indirect cooling, optimizing the thermal interface material (TIM) becomes crucial. Remarkably, the R_{th} of a DSC module can be reduced by 40 % compared to a single-sided cooled module of the same footprint operating under identical conditions [43].

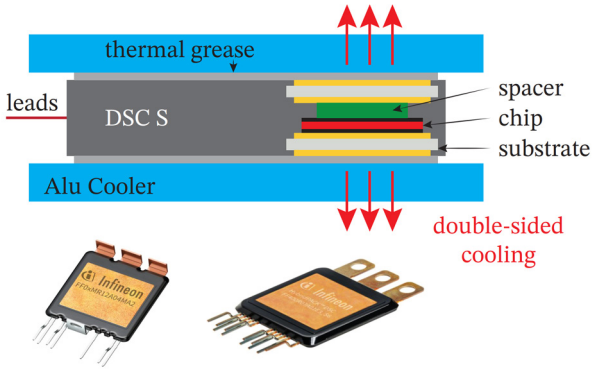


Figure 18: DSC package and its thermal stack

A refined thermal stack configuration, illustrated in Figure 18, showcases improved efficacy. In this design, dies are attached and electrically interconnected on both the top and bottom of DBC. Instead of using traditional spacers, which mainly offer structural support and, in some stack configurations, apply sufficient pressure on current pads to form spring-interconnected stacked power modules, this configuration replaces solder bumps or advanced alternatives with a gold-plated pin-fin-based copper connector (Figure 19). This substitution enhances reliability and addresses common issues such as void formation and cracking that occur in extensive soldering processes.

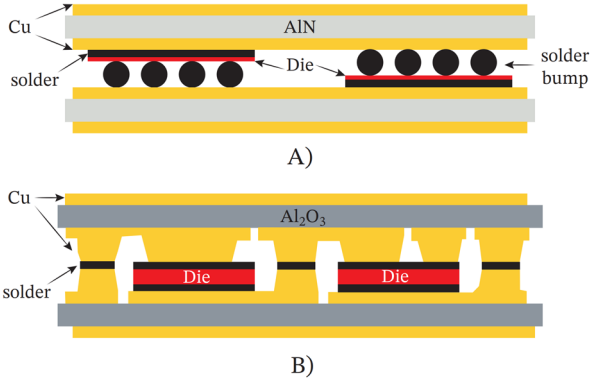


Figure 19: The cross section with (**A**) simple flip-chip technology implementing solder bumps vs (**B**) double-side sintered chips employing gold-plated pin-fin-based copper connection. Adapted from [44].

Consequently, this enhanced structure facilitates an even higher current-carrying capacity. In contrast, the

impact of parasitic capacitances (between the die and baseplate), particularly those subjected to high d*v*/d*t* during switching transients, has a much more significant effect on electromagnetic interference (EMI) and switching performance compared to single-sided configurations [25], [45]. In flip-chip technology (Figure 19), where the die of the bottom MOSFET is mounted opposite to the substrate, reducing the surface with high d*v*/d*t*, alternative methods such as increasing the thickness of the DBC substrate, incorporating an additional copper layer within the DBC for shielding, and introducing low permittivity materials into the thermal stack are found to be less advantageous due to the associated increase in thermal resistance within the power modules.

5.2.3 Kelvin-source connection

Power terminals in higher current-carrying packages are typically designed in blade terminal configurations. Conversely, gate-loop terminals often maintain internal connectivity through wire bonding in many designs. Due to fabrication constraints or safety considerations, the gate drive circuitry is usually kept separate from the power modules on distinct substrate boards. Therefore, it is crucial to minimize gate loop inductance by positioning the gate driver circuitry close to the power device. In three-terminal packages, the gate-loop also includes parasitic inductance L_s, which is placed in series with the source terminal.

As a result, the voltage at the die level may substantially differ from the voltage measured at the terminals due to voltage drops caused by the large current flowing through the power loop [46]. To mitigate the adverse effects of L_s, especially as switching frequencies increase, it is crucial to isolate the gate-loop from the effects of the switch power-loop current. This can be accomplished by implementing a Kelvin-source connection. Given the rising switching speeds of WBG devices, this approach is becoming increasingly important, both in discrete components and in packages containing multiple dies [46]. However, in multi-die modules, the layout of the Kelvin-source connection requires careful consideration, as it significantly impacts current sharing among the dies [47], [48].

6 Comprehensive integration in power modules

One of the prominent trends in power converter design over the past decade has been the increasing level of integration. At the device level, packaging has evolved to minimize stray inductance, facilitate Kelvin-source connections, enhance thermal coupling between the die and the package, and support cooling from both sides.

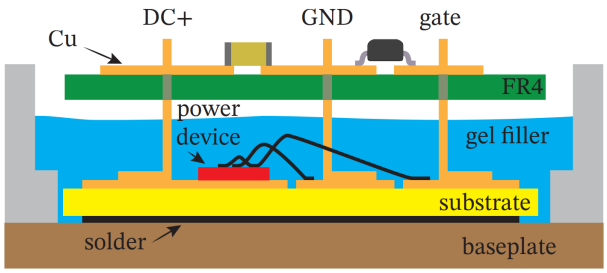
At the package level, integration began with transitioning from discrete devices to power modules, where multiple dies are attached to the same substrate to create the desired circuit topology [49]. This shift significantly simplifies power connections and streamlines converter manufacturing.

6.1 Integration of gate driver

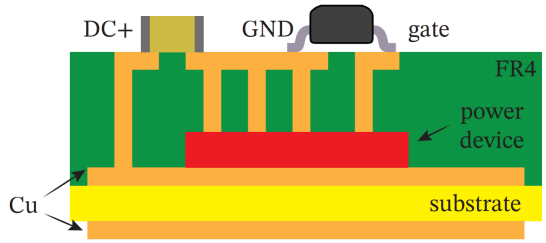
Both the power and gate drive commutation loops significantly affect the dynamics of semiconductor switches, driving extensive efforts to minimize their loops and reduce parasitic parameters. Various methods have been proposed, including the use of new packaging techniques, the addition of Kelvin pins, and the adoption of advanced bonding technologies, as presented in Sections 4 and 5. However, these approaches have their limitations and do not always yield the desired improvements in performance. Studies highlight that while these strategies contribute to reduced parasitic effects, they cannot fully overcome the inherent challenges posed by high-speed switching and the complexity of modern semiconductor devices.

The ultimate step in integration involves incorporating gate driver circuitry [50], [51] directly into the power module. This approach not only simplifies the signal routing for the converter but also substantially reduces stray inductances between the gate driver and the transistor. As a result, it decreases gate voltage overshoots and minimizes ringing [52]. This integration is particularly beneficial for converters using GaN devices, which have stricter gate terminal specifications.

Integrated gate drive GaN products can deliver superior efficiency, increased power density, and reduced magnetic component size across various applications, such as data center power supplies and solar inverters. Specifically, the Texas Instruments' LMG3522R030-Q1, which is automotive-qualified, can switch at 650 V with a frequency of 2.2 MHz and achieve high slew rates of up to 150 V/ns. This combination enables a significant 59 % reduction in the size of power magnetics [53]. Research demonstrates that positioning gate driver integrated circuits and their coupling capacitors on the direct-bonded copper substrate within the power module, rather than on the PCB, can achieve up to 45 % reduction in the gate driver's thermal resistance from junction to ambient. Incorporating an auxilliary source bond wire used as a Kelvin connection for the gate circuitry allows for effectively decoupling of the gate and power loops, achieving gate-source and drain-source loop inductances of 4.6 nH and 6.3 nH, respectively [54].



(**A**) Conventional



(**B**) Integrated

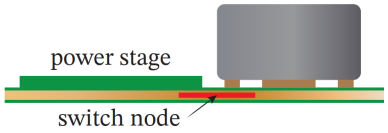
Figure 20: Packaging technologies. (**A**) presents a conventional power module structure. (**B**) demonstrates a PCB/DBC hybrid power module structure. Adapted from [55].

Another option is integrating all components of the switching device into a multilayer PCB, which further optimizes performance by embedding the semiconductor die directly into the PCB, with copper planes connecting peripheral units. This design eliminates bond wires, reducing power loop parasitic inductance to 2.8 nH [55]. However, the use of FR4 PCB material increases thermal impedance, potentially impacting thermal and electrostatic performance. This shortcoming can be addressed with a PCB/DBC hybrid power module structure (Figure 20), where a ceramic substrate is attached to the multilayer PCB with integrated semiconductor die [55]. Gate loop inductance is particularly critical in parallel-connected high-current WBG semiconductors, where synchronized gate voltages are essential to avoid timing mismatches. This synchronization requires low-inductance switching cell designs and equal gate loop parasitics, achieved through PCB layouts with length-matched signal traces connecting drivers to power switches [56].

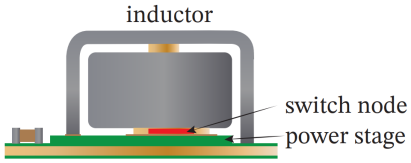
6.2 Integration of passive devices

The increased switching speeds associated with WBG devices make the effects of stray inductances and capacitances more pronounced. To address these issues, some power modules incorporate decoupling capacitors [57]. By positioning the capacitor closer to the transistor leg (Figure 13), voltage oscillations during switching events are significantly reduced, which in turn decreases the required voltage margin.

Integrating an inductor also proves advantageous [58]. As illustrated in Figure 21, this integration offers several benefits. When placed on top of the power stage, the integrated solution has a smaller footprint. It also reduces the capacitive coupling at the switching node, leading to lower electromagnetic interference (EMI). Additionally, if the inductor losses are minimal, it aids in extracting heat from the top side of the power stage.



(**A**) Discrete



(**B**) Module

Figure 21: Integration of inductor with the power module. Adapted from [58] and [59].

6.3 Integration of sensors

The integration of sensors into power modules began with simple inclusion of NTC thermistors. This approach allows for more dynamic measurement of substrate temperature, enabling the converter to operate with a reduced temperature margin. To enhance thermal coupling between the transistor and the temperature sensor, some manufacturers prefer to use a diode as a temperature sensor, which can be mounted on the same die as the power transistor [60].

Another commonly integrated sensor, especially in modules with gate drivers, is the current sensor [61], primarily used for overcurrent protection. Utilizing current mirroring based on sense MOSFETs, as suggested in [61], offers advantages by significantly reducing temperature dependence compared to the $R_{DS,on}$ method.

6.4 Complete control system integration

The complete integration of power devices, gate drivers, current and temperature sensors, and all control logic, including a processing unit (MCU), represents the culmination of integration efforts. Initial attempts, such as IR's PIIPM devices from two decades ago (Figure 22), succeeded in miniaturizing the control electronics to within the power module. However, rapid advance-

ments in silicon technology quickly rendered these devices obsolete.

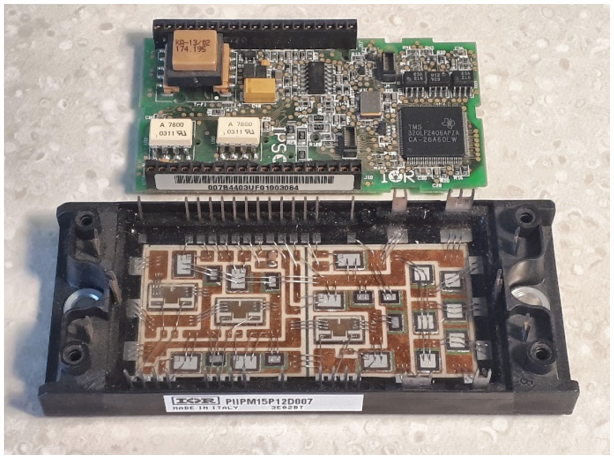


Figure 22: PIIPM power module with corresponding signal electronics including current/voltage sensing, gate drivers and processing unit

Recent examples include the "System in a Package" ST-SPIN32F0, which integrates an MCU along with complete sensing and gate-driving circuitry into a single chip (Figure 23) [62]. DRV10983 takes this a step further by also incorporating a low-power output stage, thereby delivering a complete power system within a single package.

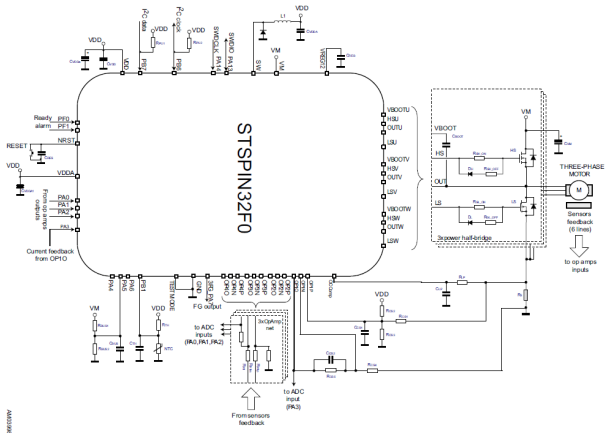


Figure 23: System in a package including processing unit, sensing and gate drivers [62].

Although this level of integration is currently limited to Si-based designs, it is anticipated that similar solutions will soon be available for GaN and SiC power devices.

6.5 Integration of cooling body

Even though the theoretical operating temperature for WBG devices can reach up to 500 °C, leading manufacturers currently offer these devices with a maximum operating temperature of 175 °C. This limitation is primarily due to reliability concerns, specifically the failure rates at the die level, which are further exacerbated by packaging constraints [63].

At the package level, a key focus is on thermo-mechanical reliability, which is particularly well-addressed by double-sided structures due to the robust interconnections between individual dies and their substrates.

Further improvements in reliability can be achieved by integrating the semiconductor die and cooling body into a single component, typically featuring liquid cooling (Figure 24). An advanced example of this integration is seen in embedded designs, where these components are integrated into the printed circuit board [64].

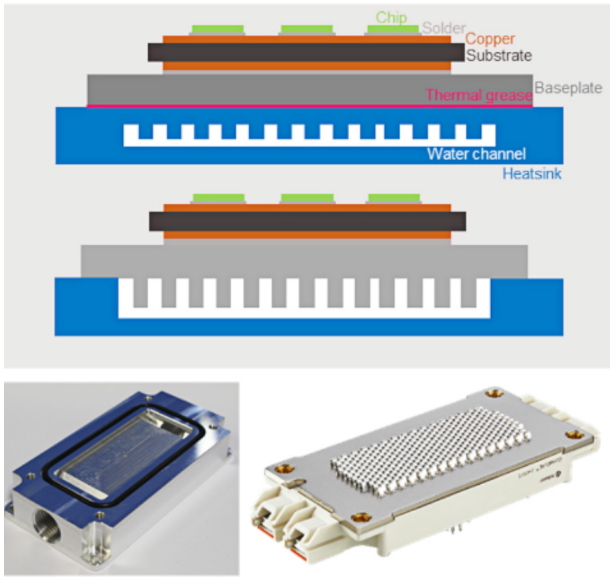


Figure 24: Schematic of power modules (upper section) with both closed (top) and open (bottom) liquid heat sink solutions. Photograph of the wave technology applied to the power module baseplate, along with the open heat sink (lower section) [65].

7 Advanced techniques in power electronics design optimization

The approach to designing power electronics systems has evolved significantly in recent decades. Traditional methods, based on experience and analytical techniques, are now heavily supplemented by multi-domain simulations, including electromagnetic, thermal, and mechanical analyses, and lately also by machine learning and artificial intelligence concepts. The focus has shifted towards accelerating prototyping and optimizing parameters such as efficiency, compactness, and EMC/EMI characteristics. The rise of WBG semiconductors, with their higher switching frequencies and dynamics, has made parasitic parameters of PCBs, pow-

er modules and even integrated circuits – inductances, capacitances, and resistances – critical to performance.

Accurate modeling of parasitic elements is essential for WBG modules, as small deviations can significantly affect converter operation. For instance, errors exceeding 10 % in loop inductance modeling can impact performance notably, highlighting the need for precise electromagnetic simulations [66].

Three main methods are used to estimate parasitic parameters: numerical simulations, analytical approaches, and experimental measurements.

7.1 Numerical simulations

Numerical tools such as Ansys Q3D, which uses finite element analysis (FEA) and the Method of moments (MOM), accelerated by the Fast multipole method (FMM) help analyze parasitics and optimize designs by accounting for proximity effects and skin effects, dielectric and resistive losses, and frequency dependencies [67]. Such tools have been validated for both discrete and module-level analyses [68], [69], improving designs by reducing the inductance and optimizing current distribution.

Authors in [70] demonstrate reduction of power loop inductance by 70 % by changing the design from lateral to vertical. A similar method was also presented for a 135 kW SiC-based traction inverter [71]. The authors in [72] significantly reduced the inductance by using multiple PCB layers for improved current distribution and magnetic field cancellation.

Sun et al. emphasized the importance of evaluating parasitic inductances for estimating the oscillation challenges during the hard switching process [73], while Liu et al. show through LTSpice simulations that the common-source inductances can increase the converter losses by up to 20 % [74].

The common-source inductance is affected by several parameters (leakage inductances of the common conductive path between power and gate loop, coupling factor of power and gate loop, presence of Kelvin source connection, internal bond structure, number of bond wires, gate loop area, submount size), which have different effects as shown by the analysis using the CST studio software [75].

As operating frequencies approach 1 MHz, the design of passive components becomes increasingly complex. Novel high-frequency GaN converters sometimes employ PCB inductors, where FEMM simulations are essential for accurate design and evaluation of parasitic elements [76].

7.2 Analytical methods

Analytical methods, though often more complex to derive, can offer speed and accuracy. Traditional inductance calculations using the Biot-Savart law may overestimate values when PCB trace dimensions are small. To address this, updated analytical methods [77] provide more accurate estimates and are validated through FEA analyses (program package Magnet) and experimental results. Simplified parasitic models are also employed to reduce the complexity of numerical simulations, streamline parameter sweeps, and improve design efficiency [73].

7.3 Experimental measurements

Parasitics can also be estimated through experimental measurements, either indirectly through transient signals and ringing characteristics [78], [79] or directly through impedance measurements. The latter are particularly useful for the characterization of decoupling capacitors [78], SMD resistors, and ferrite beads [79].

The extraction of parasitic parameters and characteristics of packaged SiC [80] and GaN [81] power transistors can also be done by measurements using the S-parameters. A similar approach using S-parameters is also useful for verifying the results of simulation models using Advanced Design Systems (ADS) software [82].

7.4 Design Optimization through Co-Simulation

In addition to parasitic inductances and capacitances [83], optimizing thermal performance is a critical aspect of the design process. Tools like Ansys Icepak, combined with Ansys Q3D and Maxwell, facilitate electro-thermal co-design by balancing inductance, capacitance, and thermal management [78]. Parasitic RLC parameters estimated by simulations are often used in combination with SPICE models of devices in conjunction with other simulation packages, such as COMSOL Multiphysics to evaluate electro-thermal properties and improve designs of power modules [79].

Overall, the integration of these advanced techniques into the design process is crucial for maximizing the performance and reliability of modern WBG-based power electronics systems.

7.5 Machine learning and artificial intelligence concepts

Machine learning and artificial intelligence concepts are rapidly transforming the field of power electronics and semiconductors by addressing challenges across design, control, and maintenance life-cycle phases [84]. These technologies excel in tasks, such as optimization, classification, regression, and data structure explora-

tion. For instance, ML facilitates the discovery of novel semiconductor materials through classification and predicts their physical, electrical, magnetic, or chemical properties [85]. Such materials are essential for the design of integrated circuits and power module packages, where advanced ML methods like deep learning and reinforcement learning are widely implemented in electronic design automation (EDA) for tasks such as placement, routing, and performance prediction [86]. Furthermore, AI enables reliability-focused design by mitigating the computational burden of finite element method simulations through dataset-driven predictions applied across functional design, reliability design, manufacturing, and testing phases [87].

AI and ML further enhance the design and prognostics of power modules, particularly in thermal management and material selection [88], [89], [90]. Combined approaches using genetic algorithms and FEM simulations have demonstrated significant optimizations, including a 27 % reduction in heat sink volume and a 6 °C decrease in junction temperature [91]. Similarly, multi-objective genetic algorithms have been applied to optimize Al ribbon loop dimensions, minimizing plastic strain and temperature [88]. ML also improves manufacturing processes by increasing wafer yield, optimizing die pickup procedures [85], [88], [92], and enabling fault diagnosis for wire-bonding equipment [93]. Conventional power converter design, often iterative and time-consuming, is now accelerated using genetic algorithms and artificial neural networks for multi-objective circuit parameter design with reduced computational time, as demonstrated in a 1 kW GaN inverter prototype [94], [95]. AI-driven digital twin modeling enables the prediction of transient behaviours and failure mechanisms, such as bond wire lift-off and junction temperature estimation in wide bandgap semiconductors [96], [97]. A new class of intelligent systems, called cognitive power electronics [98], integrates AI with embedded sensors and real-time analytics, demonstrating the transformative potential of these technologies. As computational capabilities continue to advance, ML and AI are expected to play an increasingly critical role in shaping the future of power electronics design and optimization.

8 Conclusions

WBG semiconductor switches such as SiC and GaN offer significant advantages compared to traditional Si-based counterparts.

The rise of WBG materials demands advanced packaging and design strategies to fully exploit their high-temperature and high-frequency capabilities. Traditional Si-based packaging techniques are insufficient, necessitating innovations in die attach methods, bonding techniques, and module integration.

High switching speeds necessitate a substantial reduction in parasitic parameters. This process is supported by accurate modeling and advanced design optimization techniques, such as multi-model co-simulation, novel analytical methods, and extensive experimental measurements. Moreover, machine learning and artificial intelligence concepts are playing an increasingly important role in supporting these design and optimization processes in power electronics, leading to reducing design times and improved performance. As computational power continues to grow, the impact of ML and AI in these areas is expected to expand further.

In summary, leveraging these innovations and design techniques will drive the next generation of power electronics, improving efficiency, compactness, and reliability in a wide range of applications.

9 Acknowledgments

The authors gratefully acknowledge the financial support of the Slovenian Ministry of Higher Education, Science, and Innovation, as well as the Slovenian Research and Innovation Agency (Grant: P2-0258).

10 Conflict of interest

The authors declare no conflict of interest.

11 Author contributions

Henrik Lavrič: Investigation, writing. Peter Zajec: Conceptualization, writing. Klemen Drobnič: Visualization, writing. Andraž Rihar: Conceptualization, writing. Vanja Ambrožič: Group supervision, writing. Danjel Vončina: Funding acquisition, writing. Mitja Nemec: Conceptualization, writing. All authors read, reviewed, edited, and approved the final version of the manuscript.

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Arrived: 25. 09. 2024
Accepted: 04. 12. 2024