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0.18 µm CMOS power amplifier architecture comparison for a wideband Doherty configuration

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Abstract: This paper presents a comparison between a classical and a self-biased two stage CMOS power amplifier (PA) suitable for a wideband Doherty (DPA) configuration. Both PAs are fully differential and have been implemented in IBM 7RF 0.18 µm CMOS process and are supplied from 1.8 V. Classical PA input impedance is shown to be matched from 1.6 GHz to 2.7 GHz @ S_{11} = -10 dB with external matching components. Self-biased PA his matched from 800 MHz to 1.75 GHz without any additional matching components and the bandwidth can be further increased to 2.15 GHz. Self-biased PA average PAE is 25.3 % which is 4.2 % higher than that of the classic PA. Both power amplifiers have an average output power of 10.5 dBm. The latter results show, that a self-biased PA architecture has more potential to be implemented in a wideband DPA configuration, compared to the classic PA arrangement. The active area for both on-chip PAs is 800 µm^2, whereas the full IC chip size is 1.5 mm^2. The dual PA ASIC has been designed to be enclosed in a 20-pin QFN package.

Keywords: CMOS; Power amplifier; Self-biased; Doherty; Wideband

Primerjava 0.18 µm CMOS arhitektur močnostnih ojačevalnikov za širokopasovno Doherty konfiguracijo

Izvleček: Članek predstavlja primerjavo med klasičnim in samonastavljivim dvostopenjskim CMOS močnostnim ojačevalnikom (PA) za širokopasovno Doherty (DPA) konfiguracijo. Oba sta popolnoma diferencialna in izvedena v 0.18 µm IBM 7RF CMOS tehnologiji. Napajana sta z 1.8 V. Vhodna impedanca klasičnega ojačevalnika se ujema od 1.6 GHz do 2.7 GHz @S_{11} = -10 dB z zunanjimi ujemalnimi komponentami. Samonastavljivi ojačevalnik je ustrezen od 800 MHz do 1.7 GHz brez dodatnih zunanjih komponent. Njegovna pasovna širina se lahko razširi do 2.15 GHz. Povprečen PAE je 25.3%, kar je 4.2% več kot pri klasičnem ojačevalniku. Oba ojačevalnika imata izhodno moč 10 dBm, kar nakazuje, da je samonastavljivi ojačevalnik bolj primeren za širokopasovne DPA konfiguracije. Površina obeh je 800 µm^2, pri velikosti čipa 1.5 mm^2. Dvojni PA ASIC je bil dimenzioniran, da ustreza 20 pinskem QFN ohišju.

Ključne besede: CMOS; močnostni ojačevalnik; samonastavljiv; Doherty; široki pas

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1 Introduction

Over the past decade, the number of papers published on power amplifier (PA) research has been increasing exponentially. Since then different PA efficiency enhancement techniques and architectures have been proposed and the Doherty power amplifier (DPA) arrangement is one of the most promising [1]. The vast majority of published papers present single-ended or differential Doherty power amplifiers designed using a classical PA topology. Only classical, cascode PAs with either common inductors, slab inductors or baluns implemented in a DPA have been researched [3-14]. This article presents a comparison between a classical two stage power amplifier and a self-biased PA approach both suitable to be implemented in a wideband DPA. This paper is arranged as follows: DPA design challenges and a performance comparison between the published DPAs are presented in the second chapter. The proposed classical and self-biased PA architectures are presented and thoroughly analyzed in the next chapter. Simulation results and full ASIC layout are presented in the following chapter. Finally conclusions are made and references are given.

2 Doherty power amplifier design challenges

Multiple power amplifier architectures have been published in research papers over the last decade, including classic, cascode, self-biased PA configurations employing different parameter improvement techniques such as feedback, feedforward or/and linearization circuits. One of the most promising advanced PA architecture – Doherty power amplifier (DPA) presented in Figure 1 – provides a combination of high linearity and sufficient PAE at input powers ranging from back-off power to P1dB. Although DPAs prove to be very efficient at a certain frequency, there are several drawbacks in the architecture which restrict performance over wide bandwidth. The first drawback is the bandwidth of the classical output impedance inverter, which enhances the DPA to utilize loadpull in order to achieve high efficiency. This has been addressed in [2] and it has been proven, that the proposed impedance inverter can be designed in such a way that has more than 83 % of fractional bandwidth. Another DPA drawback is the inevitable result nonlinear nature of the peak amplifier. The peak amplifier is typically biased in class *C* [15] and requires harmonic termination. A harmonic termination circuit is essentially a series *LC* circuit (resonator) connected as a shunt to the output of the peak amplifier. Consequently for a larger DPA bandwidth several switchable harmonic terminations may be used.

Table 1 summarizes published CMOS DPA parameters. The latter table reveals, that the scaling of CMOS process does not improve the main design criterion for the always power hungry PA – power added efficiency (PAE). According to Table 1 CMOS processes in the range from 0.18 µm to 0.13 µm provide the largest DPA efficiency. Moreover, the latter processes are have been around since 1999-2001, therefore the relation between the performance and price per chip area can be very attractive for DPA designers and researchers.

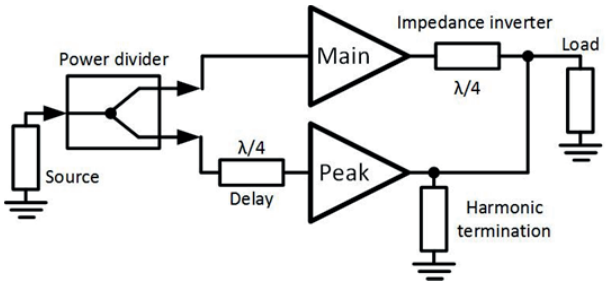


Figure 1: Classic Doherty power amplifier block diagram

3 Power amplifier architectures for wideband Doherty configuration

The simplified single-ended classic two-stage cascode PA is presented in Figure 2. The latter PA input and output stages are biased from internal sources for AB class operation. Cascoding in both stages has been chosen in order to reduce the influence of Miller effect and improve both isolation and stability. Gain control has been implemented to toggle the cascode transistors in both stages through on-chip buffers.

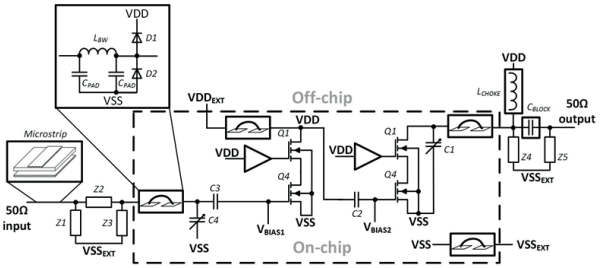


Figure 2: Classic two stage single ended power amplifier simplified schematic

Table 1: CMOS Doherty power amplifier performance comparison

Ref.	Process	VDD, V	Frequency, GHz	P1dB, dBm	Overall PAE, %	Power back-off, dB
3	0.18 µm CMOS	3.7	3.5	24.4	36.1	6.0
4	0.18 µm CMOS	3.3	2.4	29.5	22.0	5.0
5	0.18 µm CMOS	3.0	2.4	22.6	31.0	7.0
6	0.18 µm CMOS	-	0.89	25.0	43.6	5.0
7	0.13 µm CMOS	3.3	2.4	31.9	30.1	5.0
8	0.13 µm CMOS	3.3	1.7	31.7	33.0	5.0
9	0.13 µm CMOS	3.0	2.4	22.0	45.0	7.0
10	90 nm CMOS	3.3	2.4	30.0	24.0	5.0
11	90 nm CMOS	2.4	2.4	24.8	26.0	5.0
12	65 nm CMOS	5.5	2.535	23.4	25.0	8.5
13	65 nm CMOS	3.3	2.4	33.5	20.0	5.0
14	65 nm CMOS	2.5	2.4	23.4	24.7	7.0

The simplified single-ended self-biased two stage PA is presented in Figure 3. The main difference between the latter PA and the classic architecture is the type and the biasing of the first stage. The first stage is inverter based and is biased at *VDD*/2 via diodes Q_2 and Q_5. In order to widen input S_{11} response, R_1 and C_2 components should be designed with caution. One of the main drawbacks of an inverter based input stage is that the input saturates at 5 dB to 10 dB lower input powers than the classic input stage. The output stage is biased for an *AB* class operation from an internal source.

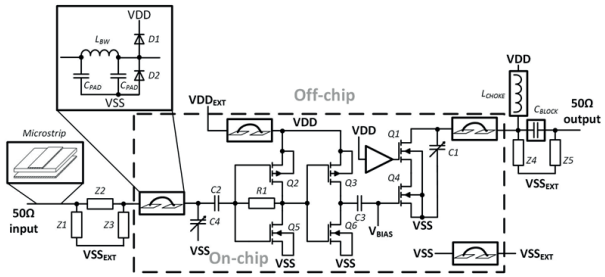


Figure 3: Self-biased two stage single-ended power amplifier simplified schematic

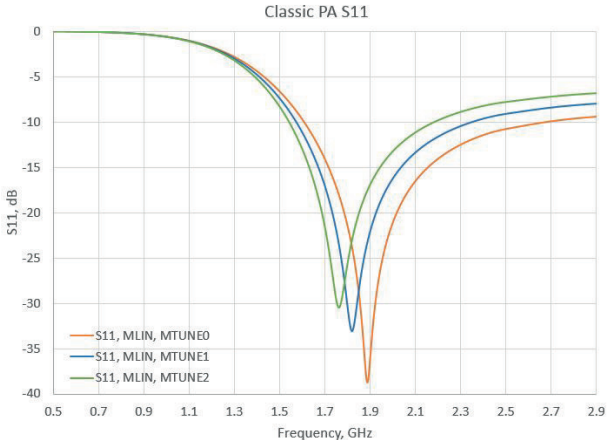
In both PA architectures, capacitors C_4 and C_2 act as DC blocks and also influence the overall PA stability. Digital varactors C_1 and C_4 are used to tune input and output impedances in order to achieve optimal power and gain matching respectively. In order to get more accurate impedance matching results, bondwire models with ESD protection diodes and microstrip feed lines (as *S*-parameter *nPort* elements) are also introduced. Both input (Z_1, Z_2, Z_3) and output (Z_4, Z_5, C_{BLOCK} and L_{CHOKE}) impedance matching networks are placed off-chip due to the lack of chip area. External component package parasitics were also taken into account during calculations.

4 Simulation results

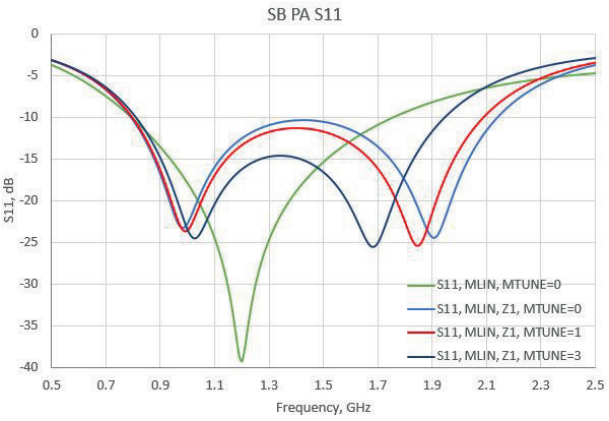
This chapter presents simulation results for the proposed PAs. It should be noticed, that the presented results correspond to the fully differential power amplifier configurations, whereas Figure 2 and Figure 3 present only the simplified single-ended schematics. Both PAs operate at 1.8 V supply voltage and were designed to provide a power gain of 20 dB and output power of 11 dBm to a 50 Ω load.

Input impedance matching results for both PA architectures are presented in Figure 4. Figure 4 (a) presents S_{11} response for the classic PA configuration with an external impedance matching network Z_2 and Z_3. External matching component Z_2 has been designed to be a 1.5 pF capacitor and Z_3 – a 4.2 nH shunt inductor. The matched frequency can be altered either by changing internal C_4 capacitor control *MTUNE* value or by varying the off-chip shunt inductor Z_3. In both cases the S_{11} notch response bandwidth does not top 1.1 GHz at S_{11} = -10 dB.

In comparison, Figure 4 (b) presents input impedance matching results for the self-biased PA architecture. Taking into account package parasitics and a cautious R_1 (ref. Figure 3) resistor value tuning leads a naturally matched bandwidth of 1 GHz without any additional matching components ("S11, MLIN, MTUNE = 0" plot in Figure 4 (b)). The matching bandwidth can be further increased by introducing a series (Z_2 in Figure 3) 6.2 nH inductor and altering *MTUNE* value.



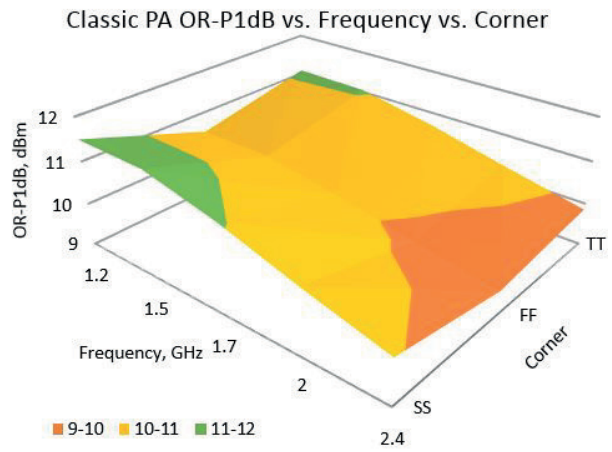
a



b

Figure 4: Classic PA (a) and self-biased PA (b) *S11* response control

Figure 5 presents output referred 1 dB compression point (P1dB) over frequencies and corners for both PA architectures. Both power amplifiers have been designed to output an average power of 10.5 dBm.



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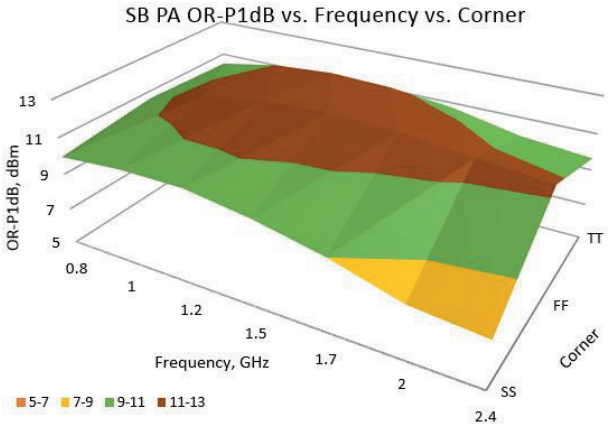
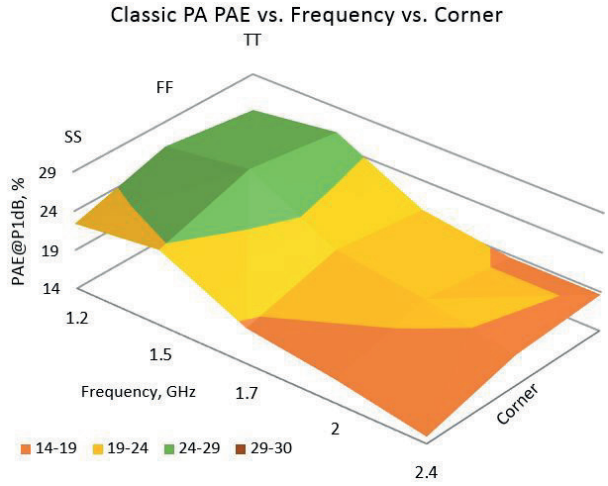


b

Figure 5: Classic PA (*a*) and self-biased PA (*b*) output referred 1 dB compression point at different frequencies and corners

Power added efficiency is presented in Figure 6. Self-biased PA average PAE is 25.3 % which is 4.2 % higher than PAE of the classic PA.

Table 2 presents the raw simulation data for surface plots in Figure 5 and Figure 6. The results presented in Table 2 depict that the self-biased PA architecture has a



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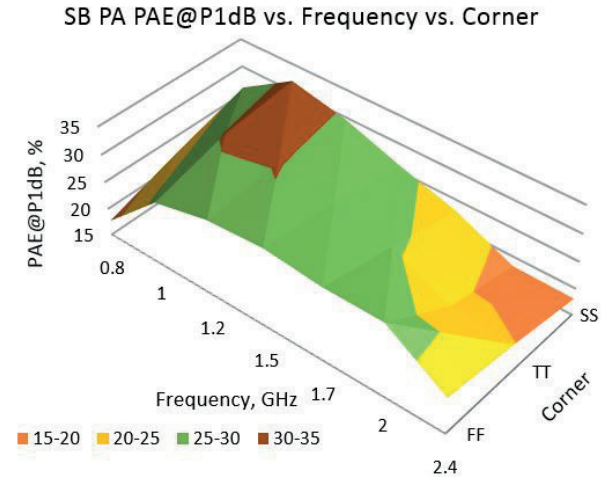

b

Figure 6: Classic PA (*a*) and self-biased PA (*b*) power added efficiency at different frequencies and corners

25 % vantage in bandwidth and 1.4 % – 5.8 % efficiency at all corners and frequencies.

The layout of the designed dual differential power amplifier, implemented in IBM 7RF 0.18 µm CMOS process,

Table 2: Classic and self-biased CMOS power amplifier performance comparison at different frequencies and corners

SS		Classic PA OR-P1dB			SB PA OR-P1dB			Classic PA PAE@P1dB			SB PA PAE@P1dB		
		FF	TT	SS	FF	TT	SS	FF	TT	SS	FF	TT	
Frequency, GHz	0.8	-	-	-	9.9	10.6	10.4	-	-	-	26.0	17.6	22.1
	1.0	-	-	-	10.2	11.5	11.0	-	-	-	31.9	26.5	30.3
	1.2	11.5	10.5	11.1	10.3	12.0	11.3	22.4	25.8	24.3	29.6	28.8	30.1
	1.5	11.5	10.5	11.0	9.8	12.2	11.1	23.7	27.4	25.8	26.1	29.5	28.3
	1.7	11.1	10.2	10.7	9.0	12.1	10.7	18.5	21.7	20.2	23.0	28.5	25.8
	2.0	10.5	9.8	10.3	7.9	11.7	10.0	17.0	20.2	18.7	18.3	28.5	20.9
	2.4	10.0	9.5	9.9	7.6	11.4	9.6	14.9	17.9	18.7	18.1	21.7	20.1

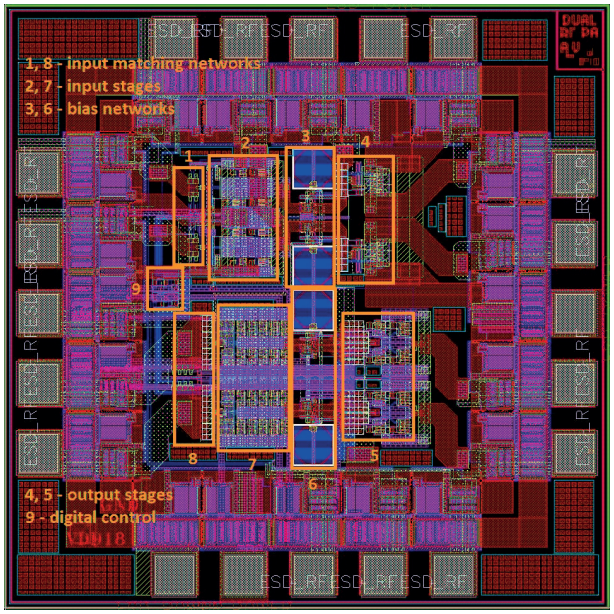

Figure 7: Dual differential power amplifier IC layout

IC is presented in Figure 7. PA implemented in classic architecture is presented on the top of the latter figure, and the self-biased PA – on the bottom. On-chip input matching network tuning circuits are marked 1 and 8. Active input stages are marked 2 and 7. Output stage bias networks are marked 3 and 6. Active output stages are marked 4 and 5 whereas digital control block is marked 9. The active area for both on-chip PAs is 800 μm^2, whereas the full IC chip size is 1.5 mm^2. The dual PA ASIC has been designed to be enclosed in a 20-pin QFN package and is prepared to be send to fabrication.

5 Conclusion

A comparison between a classical and a self-biased PA architectures was presented in this article both suitable for a wideband Doherty configuration. Both PAs are fully differential have been implement in IBM 7RF 0.18 μm CMOS process and are supplied from 1.8 V. Classical PA architecture has a notch type S_{11} response and a bandwidth up to 1.1 GHz (from 1.6 GHz to 2.7 GHz @ S_{11} = -10 dB) with external matching components. Self-biased PA his matched from 800 MHz to 1.75 GHz without any additional matching components and the bandwidth can be further increased to 2.15 GHz by introducing an external matching network and by tuning the on-chip capacitance. Self-biased PA average PAE is 25.3 % which is 4.2 % higher than that of the classic PA. Both power amplifiers have an average output power of 10.5 dBm. The latter results show, that a self-biased PA architecture has more potential to be implemented in a wideband DPA configuration, compared to the classic PA arrangement. The active area for both on-chip differential PAs is 800 μm^2, whereas the full IC chip size is 1.5 mm^2. The dual PA ASIC has been designed to be enclosed in a 20-pin QFN package and is prepared to be send to fabrication.

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