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High-performance Current-Controlled Quadrature Oscillator Using an optimized CCII

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Abstract: This paper proposes two structures of current-controlled quadrature Sinusoidal oscillator in CMOS technology (Voltage mode "VM" and Voltage/Current mode "VCM"). Thanks to its high degree of controllability, the translinear second-generation current conveyor is used as a basic block for our oscillator. The proposed circuit employs three optimized translinear second-generation current conveyors (CCII). The oscillation condition and the oscillation frequency are independently controllable by bias current. The proposed Quadrature Oscillator frequency can be tuned in the range of [285 MHz – 844 MHz] by a simple variation of a DC bias current. ADS (Advanced Design System) simulation results are performed using CMOS 0.18 µm process of TSMC.

Keywords: Voltage Mode Current-controlled Oscillators; Standard CMOS current conveyor; Voltage/Current Mode Current Controlled Oscillators; CMOS 0.18 µm process of TSMC; optimized CCII.

Visoko učinkovit tokovno krmiljen kvadrantni oscilator z optimiziranim CCII

Izvleček: Članek predlaga dve strukturi tokovno krmiljenega kvadrantnega sinusnega oscilatorja v CMOS tehnologiji (napetostni – VM in napetostno tokovni – VCM). Zaradi velike zmožnosti nadzorovanja je za osnovni blok oscilatorja uporabljen translinearen tokovni krmilnik druge generacije (CCII). Frekvenca oscilacije je neodvisno določljiva z enosmerno komponento toka v območju od 285 – 844 MHz. Simulacijski rezultati so narejeni v CMOS 0.18 µm tehnologiji TSMC

Ključne besede: napetostni tokovno krmiljen oscilator; standardni CMOS tokovni krmilnik; napetostno tokovni oscilator; CMOS; CCII.

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1 Introduction

Variable-frequency quadrature Oscillators are basic signal-generating blocks frequently needed in communication systems. The LC or RC quadrature oscillator presents many problems in the literature such as problems of integration, limitations of Surface Acoustic Wave, impedance matching, tuning, linearity, phase noise, … etc. For this reason, the voltage and current-controlled resistors (VCR and ICR) are widely used to replace floating or grounding resistors. The literature abounds with approaches implementing VCR and ICR [2-3]. Some structures use the OTA (Operational Transconductance Amplifier) [1], circuit-based on MOS transistors operating in saturation region [4]. Nevertheless, these circuits suffer from their dependence to absolute temperature and their small input voltage range and complexity of control. Second-generation current-conveyor (CCII) based resistor blocs provide a working solution to solve these problems [5-6].

In order to enhance the performance, minimize the noise effect provoked by the floating and grounding resistor, get controllable characteristics for the proposed Quadrature oscillator, translinear second-generation, current-controlled conveyor based structures seem to be the most efficient [7-8]. These structures

present a higher degree of CCII characteristics control [9-10]. This family of CCII is first proposed in bipolar technology [9-11]. Recently, the translinear CCII family was extended to MOS submicron technologies going towards VLSI design. Reaching submicron technologies, the MOS transistor becomes able to achieve high transit frequencies [12-15]. These CCII's structures are used in different radio frequency (RF) controllable applications such as oscillators, quadrature oscillators and filters [10-15].

This paper is organized as follows: In section II, we present the characteristics of optimized translinear Second Generation Current Conveyors. Simulation results of an optimized translinear second generation current conveyor are highlighted in section III (implemented in 0.18µm CMOS technology). In section IV, we present the CCII based quadrature oscillator architecture. We introduce the proposed Controlled Quadrature Oscillator in section V. Finally, the proposed structure is designed and simulated using ADS (Advanced Design System) software.

2 The optimized transinear loop-based ccii configurations

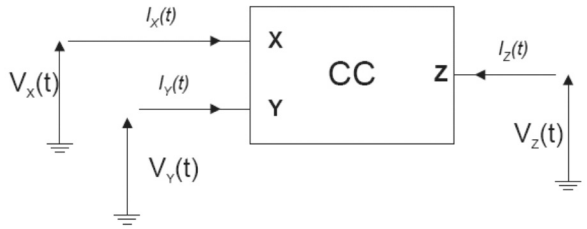


Figure1: General representation of a current conveyor

The CCII is a three-terminal active block. Its general representation is shown in Figure 1. The CCII ensures two functionalities between its terminals:
A Current follower between terminals X and Z.
A Voltage follower between terminals X and Y.

In order to get ideal transfers, a CCII should be characterized by low impedance on terminal X and high impedance on terminals Y and Z.

An implementation of the second-generation translinear loop-based current conveyor with a positive current transfer from X to Z terminal (CCII+) is shown in Figure 2 [10]. In this configuration, the relation between terminal voltages and currents can be expressed in the following matrix:

$$\begin{pmatrix} I_Y(s \\ V_X(s) \\ I_Z(s) \end{pmatrix} = \begin{pmatrix} \frac{1}{\mathrm{R_Y//C_Y}} & 0 & 0 \\ \beta(\mathrm{s}) & \mathrm{R_X} & 0 \\ 0 & \alpha(\mathrm{s}) & \frac{1}{\mathrm{Rz//Cz}} \end{pmatrix} \begin{pmatrix} V_Y(s) \\ I_X(s) \\ V_Z(s) \end{pmatrix} \quad (1)$$

Where R_Y , C_Y and R_Z, C_Z are respectively parasitic resistances and capacitances at port *Y* and *Z*. R_X is the series parasitic resistance at port *X*. α and β are the current and the voltage transfer gains of the CCII, respectively.

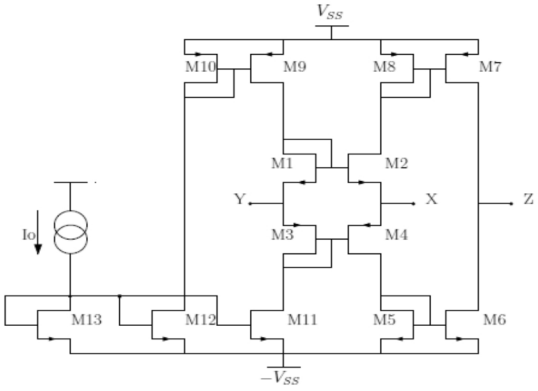


Figure2: Translinear loop MOS-based implementation of CCII

In this configuration, the voltage follower function between Y and X nodes is ensured by means of one mixed translinear loop formed by transistors M1, M2, M3 and M4. Transistors M9-M13 allows the mixed loop to be DC-biased. The output NMOS and PMOS current mirrors duplicate the current flowing from X to Z ports. For later optimization of this configuration, we should dispose of a process dependent explicit model of the different parasitic impedances on X, Y and Z ports. The parasitic effects in this CCII are to be modeled in a 0.18µm CMOS technology. Assuming the same static transconductance factors for the NMOS and PMOS transistors, a simple small signal analysis of the proposed circuits leads to the following expressions:

$$R_X \approx \frac{1}{g_{m2}+g_{m4}} = \left[\frac{1}{\sqrt{2k_P(\frac{W}{L})_P}+\sqrt{2k_N(\frac{W}{L})_N}}\right]\frac{1}{\sqrt{I_o}} = \frac{V_{xy}}{I_x} \quad (2)$$

$$R_z = \frac{1}{g_{ds6}+g_{ds7}} = \frac{1}{\lambda_{N6}Io+\lambda_{P7}Io} \quad (3)$$

$$R_Y \approx \frac{1}{g_{ds1}+g_{ds3}} = \frac{1}{\lambda_{N1}Io+\lambda_{P3}Io} \quad (4)$$

where λ_n and λ_p are channel length modulation factors for NMOS and PMOS transistors, μ_n and μ_p are electrons and hole mobility and g_{mi} and r_{oi} are transconductance

and output resistance of M_i transistor, respectively, with:

$$g_{mi} = \sqrt{2k_{NorP}(\frac{W}{L})_i(1+\lambda_i V_{DS})I_o} \approx \sqrt{2k_{NorP}(\frac{W}{L})_i I_o} \quad (5)$$

$$\frac{1}{r_{oi}} = g_{dsi} = \frac{\lambda_i I_o}{(1+\lambda_i V_{DS})} \approx \lambda_i I_o \quad (6)$$

We can see from the above equations that entire translinear loop-based CCII parasitic impedances can be controlled by means of I_o. Moreover, parasitic resistance on the X (R_X) port was used in many high-frequency tuning applications. Getting lower values of this resistance can lead to higher frequency operations. In this light, we try below to ameliorate the performance of the CCII by optimization approach. This strategy consists in minimizing the X port input resistance value, maximizing the resistance values of Y and Z ports, maximizing high cut-off current (F_{ci}) and voltage (F_{cv}) frequencies, minimizing noise effect ($\overline{i_{T,out}}^2$) and silicon area (S), minimizing the deviation between F_{ci} and F_{cv} and minimizing the deviation between α (current static gain) and β (voltage static gain). To obtain good performance we will maximize the objective function. The objective function can be expressed as follows:

$$F_o = a_1 * F_{ci} + a_2 * F_{cv} + \frac{a_3}{\overline{i_{T,out}}^2} + a_4 * (Ry + Rz) + \frac{a_5}{Rx} + \frac{a_6}{S} + \frac{a_7}{|F_{cv} - F_{ci}|} + \frac{a_8}{|\alpha - \beta|} \quad (7)$$

Where $a_1,...,a_8$ are positive coefficients used for normalization.

The static current and voltage gains are given by the following equations:

$$\beta = \left|\frac{V_X}{V_Y}\right| = \frac{E}{F+E} \quad (8)$$

$$\alpha = \left|\frac{I_Z}{I_X}\right| = \frac{G}{K} \quad (9)$$

Where:

$$E = g_{m8}g_{m5}(g_{m2} + g_{m4}) + g_{m8}g_{m2}(g_{ds4} + g_{ds5})$$

$$F \approx g_{m8}g_{m5}(g_{ds2} + g_{ds4})$$

$$G = g_{m4}g_{m6}(g_{m8} + g_{ds8} + g_{ds2}) + g_{m7}(g_{m2}g_{m5} + g_{ds2}g_{m5} + g_{m2}g_{ds4})$$

$$K = g_{m4}g_{m5}(g_{m8} + g_{ds8} + g_{ds2}) + g_{m8}(g_{m2}g_{m5} + g_{ds2}g_{m5} + g_{m2}g_{ds4} + g_{m5}g_{ds4} + g_{m2}g_{ds5}) + g_{m8}g_{m4}g_{ds5} + g_{m2}g_{m5}g_{ds8}$$

The current bandwidth is given by:

$$H_i(s) == \frac{A}{B * s^2 + C * s + D} \quad (10)$$

Where:

$$A = -(1 + g_{m4} \cdot r_{04})(1 + g_{m6} \cdot r_{06})/r_{06}$$

$$B = C_{gs4} \cdot r_{04}(C_{gd4} + C_{gs6} + C_{gs5})$$

$$D = g_{m4} \cdot r_{04} \cdot g_{m5} + g_{m5}$$

and

$$C = (((C_{gd4} + C_{gs6} + C_{gs5}) \cdot g_{m4} + C_{gs4} \cdot g_{m5}) \cdot r_{04} + C_{gd4} + + C_{gs4} + C_{gs5} + C_{gs6})$$

To optimize the CCII, we use a Heuristic methodology [15-16]. The Heuristic optimization approach follows the plot depicted in Figure 3. It starts with an initialization of the parameters vector which includes the sizing of the different transistors interfering in the above expressions. A random choice of the variables vector is then done followed by a verification of the preliminary conditions. These conditions are imposed to ensure that the different transistors are in the inversion mode of operations. If these conditions are fulfilled, the vector parameters are candidates for the following steps, otherwise we do another choice. Next, we compute the objective function. If it is decreasing, when compared to the previous iteration, the parameter vector is saved; otherwise, we keep this vector unchanged. After a series of trials with the randomly chosen parameters, the parameter vector corresponding to the minimal objective function is obtained. When the number of trials is important, this solution corresponds to an optimal solution. This method does not suffer from any divergence problems seen when applying gradient-

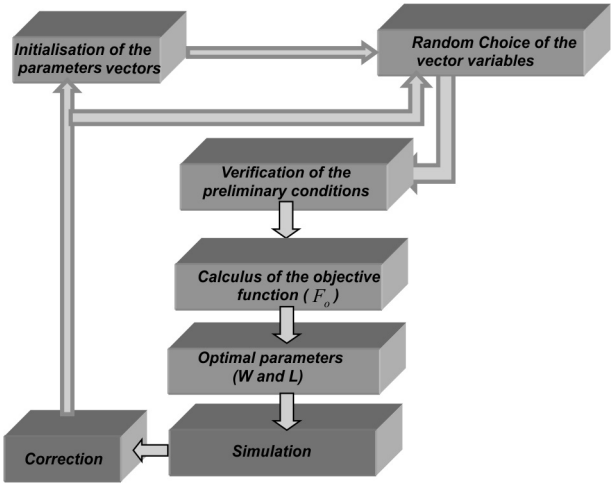


Figure 3: The optimization approach.

based methods, but its efficiency is closely related to the number of iterations. Indeed, with a high number of trials, we manage to explore in a simple random way all the proposed tuning range of the different parameters and good performances are ensured. Finally, we simulate the performances of the optimized CCII. If it is correct we take the optimal parameters else we go to the correction phase.

We notice that the optimization process can be done with a ±1.5V supply voltage and 100µA bias current (table 1). The obtained optimal transistor sizes are reported in table 2.

Table 1: Simulation conditions

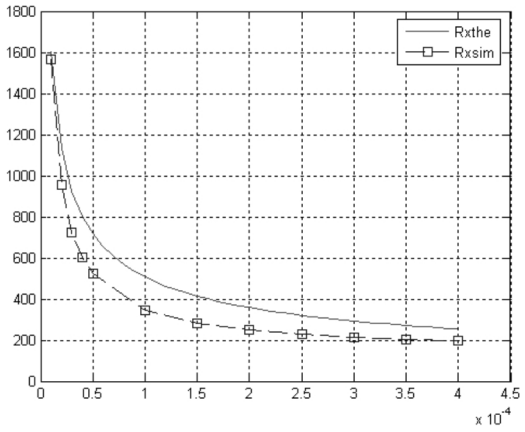
Technology	0.18 µm CMOS TSMC
Supply voltage	1.5 V
Bias current	100 µA

Table 2: Optimal device sizing

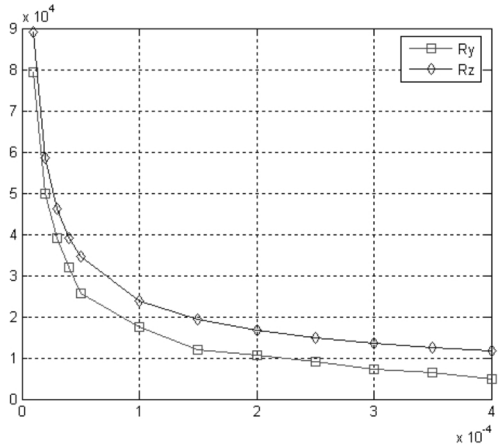
Device Name	Aspect ratio W/L (µm)
M1, M2	6.1/0.18
M3, M4	27.45/0.18
Mxx (in PMOS current mirrors)	13.725/0.18
Mxx (in NMOS current mirrors)	3.05/0.18

3 Simulation results

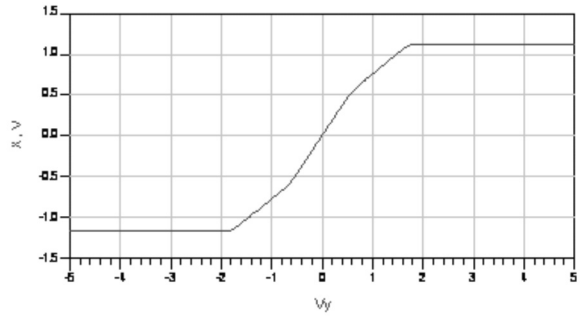
The optimized current conveyor was simulated with ADS software. The main results obtained are represented in Figure 4



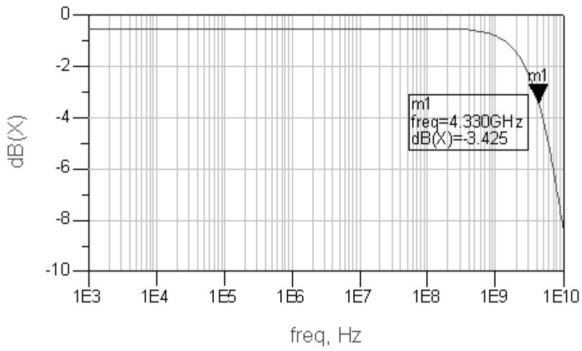
A. Parasitic resistance at x terminal (Rx(Ω)) relative to Io(A)



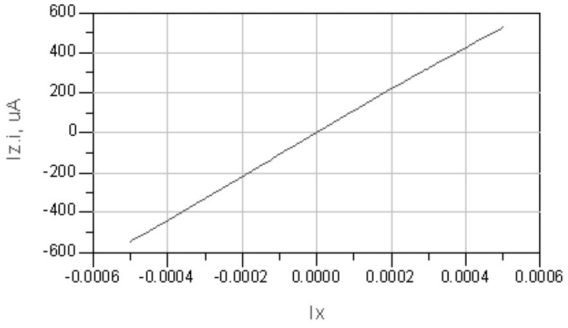
B. Parasitic resistance at Y and Z terminals (Ry(Ω) and Rz(Ω)) relative to Io (A)



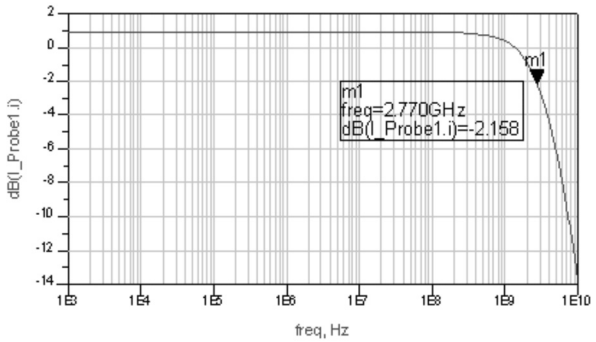
C. Voltage DC transfer characteristic of the CCII



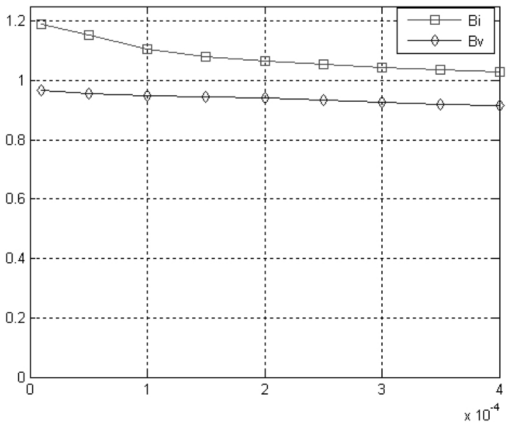
D. Frequency response of the voltage follower Vx/Vy



E. Current DC transfer characteristic of the CCII



F. Frequency response of the current follower Iz/Ix



G. current and voltage gains versus Io (Bi and Bv present respectively αand β)

Figure 4: Performance of the optimized CCII

ADS software simulations of the translinear loop based CCII in Figure 2 were conducted under the optimal parameters. The parasitic resistance at port X is represented in Figure 4.A versus I_o. It is obvious that R_X can be controlled in the range [200Ω, 1.6kΩ] by varying I_o in the range [1μA, 400μA]. The fact that should be underscored is that, even though this structure has a lower R_X when compared to the value given in [11, 15]. Figure 4.A depicts results obtained from both simulations (R_X) and MAPLE theoretical calculus of (R_{Xthe}). We notice a good agreement between both characteristics. Figure 4.B depicts the parasitic resistance values R_Z and R_Y versus the bias current I_o. Accordingly, tunable characteristics can be obtained while higher values of these parasitic resistances are preserved.

Figure 4.C and Figure 4.E display the DC transfer characteristics of the optimized CCII. The voltage transfer can be linear between -0.7V and 0.7V. Moreover, the bandwidths of output terminals are shown in Figure 4.D and Figure 4.F. The −3dB bandwidths of I_z/I_x and V_x/V_y are located at 4.33GHz and 2.77GHz, respectively. Figure 4.G indicates that α and β (current and voltage gains) are close to unity. The remaining other static and dynamic characteristics of the optimized translinear configuration are summarized in table 3.

Table 3: Performance characteristics of the optimized CCII with Io = 100μA and 1.5 supply voltage

Voltage gain β	0.943
Current gain α	1.1
Fci	2.7GHz
Fcv	4.33GHz
Relative current Error	0.15%
Relative Voltage Error	0.093%
Input Impedance(RY//CY)	18KΩ//87fF
Input Impedance(Rz // Cz)	24KΩ//25fF
Input Resistance Rx	380Ω
The offset current	-2.2μA
The offset voltage	13mV

It is noticeable that the optimized configuration yields a high current and voltage cut-off frequencies. This structure is a promising building block for the design of RF blocs such as the controlled quadrature oscillator.

4 Quadrature Oscillator based on the CCII

This architecture of the oscillation structure of Figure 5 [17-18] uses only three optimized CMOS CCIIs, one floating resistor along with the grounded resistors and capacitors. Taking into account these passive connections, we get the following characteristic equation of the oscillator:

$$s^2C_1C_5 + sC_5\left(\frac{1}{R_4} - \frac{1}{R2}\right) + \frac{1}{R_4R_{X3}} = 0 \qquad (12)$$

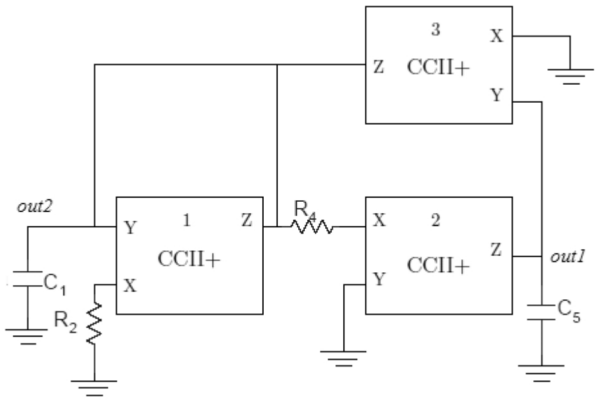


Figure 5: Variable Frequency Oscillator Implementation

This leads to the following oscillation condition and oscillation frequency, respectively:

$$R_4 \geq R_2 \tag{13}$$

$$f_0 = \frac{1}{2\pi\sqrt{C_1 C_5 R_{X3} R_4}} \tag{14}$$

In the reality R_2 and R_4 are respectively given by these relations: $(R_2 + R_{x1})$ and $(R_4 + R_{x2})$. If one of the values varies after implementation, we can recover the correct value by I_{o1} or I_{o2}.

From the above equations, a variable frequency oscillator is obtained. The oscillation frequency can be adjusted independently without modification of the oscillation condition by varying R_{X3}. In this case, the oscillator will be controlled by means of a current source I_{o3}. The confirmed performance of the oscillator is reported in Figure 6, showing the responses of the oscillator where $C_1=C_5=0,3pF$, $R_2=R_4=300\Omega$, $I_{03}=230\mu A$ and $I_{01}=I_{02}=400\mu A$. Figure 7 reveals that the phase and amplitude noise for 10MHz (offset frequency) are -115.5dBc and -145.2dBc, respectively.

A sensitivity analysis of the quadrature oscillator shows that:

$$S_{C_1}^{w_o} = S_{C_5}^{w_o} = S_{R_{x3}}^{w_o} = S_{R_4}^{w_o} = -\frac{1}{2}$$

Therefore, all of the passive-element sensitivities of the quadrature oscillator parameters are low.

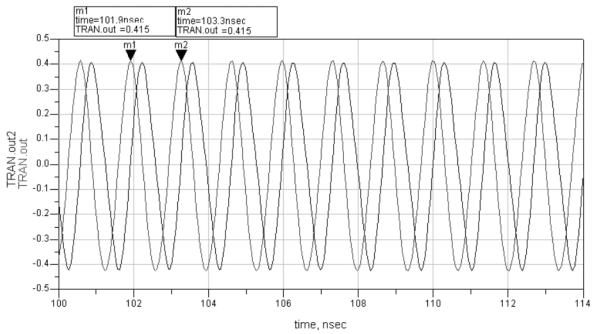


Figure 6: The simulation results of current waveforms of oscillator

The quadrature oscillator is simulated for different CCII bias currents. Simulation results are shown in Figure 8. When varying the current I_{o3} between 30 µA and 400 µA, the oscillation frequency is tuned in the range [285–844 MHz].

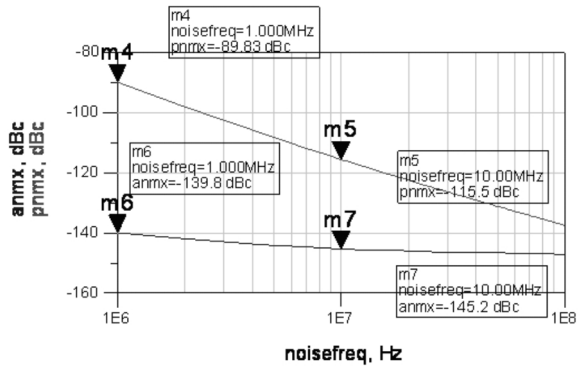


Figure 7: Phase and amplitude noise

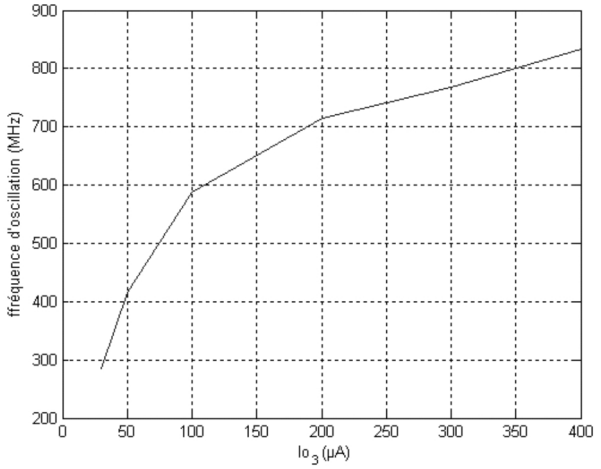


Figure 8: Oscillation Frequency versus Control Current (I_{o3})

The major drawback of this structure is the existence of floating resistance (R_4). The dispersion of manufacturing processes and the temperature variation contribute to the absolute error value of the resistance. In VLSI technology, a resistor is implemented on silicon wafer. However, resistors of practical values on silicon wafer suffer from limited values and high variability due to process variations. Moreover, its resistance values are not variable after integration. The same phenomenon can degrade the value of R_4 and R_2 after integration. Therefore, the basic idea is to replace these resistances

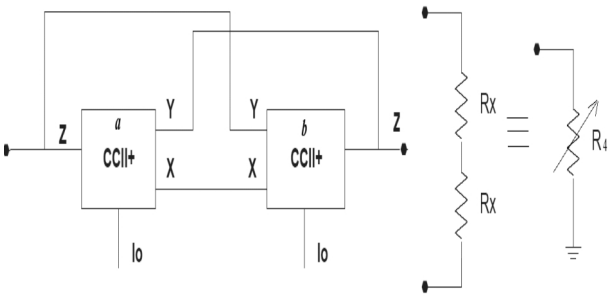


Figure 9: The active floating resistance Req=R_{Xa}+R_{Xb}=R_4

by active resistors bloc. To address this problem, we present in Figures 9 and 10 a solution to eliminate the use of floating resistance and replace the grounding resistor.

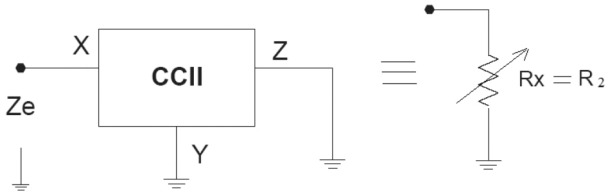


Figure 10: The active grounding resistance Req=R_X=R_2

5 The new Voltage Mode (VM) Current controlled quadrature Oscillator:

The basic idea in the proposed VM quadrature oscillator consists in replacing the resistance R_4 by the active floating resistance given in Figure 9 and the resistance R_2 by the parasitic resistance on port *X* (Figure 10). To realize these blocs, we use this implementation of optimized CCII. The new structure of the quadrature oscillator is shown in Figure 11.

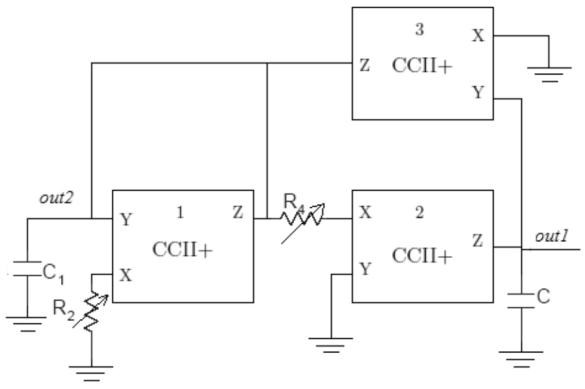


Figure 11: The proposed quadrature oscillator implementation

The advantages of this circuit are the following:

- The circuit enjoys simple controlled optimized structure which can be easily configured to realize quadrature oscillator using the minimum number of passive components.
- The circuit uses grounded capacitors with no externally connected resistors; this should be very convenient for integration.
- The circuit possesses independent controls of the oscillation frequency. Thus, the latter can be controlled by adjusting a bias current of $CCII_3$ without disturbing the condition of oscillation while this condition can be met without disturbing the frequency of oscillation by the bias current of $CCII_4$; this should pave the way for electronic tunability.

The proposed oscillator is simulated for different CCII polarisation currents. The responses of the quadrature oscillator where C_1=*0,3pF*, C_5=*0,3pF*, R_4=R_{Xa}+R_{Xb}=R_2=R_X=*600Ω* (I_{oa}=I_{ob}=*130μA* and I_{o4}=*40μA*), I_{o3}=*230μA* and I_{o1}=I_{o2}= *400μA* are given in Figure 12. The oscillation frequency is equal to 625MHz.

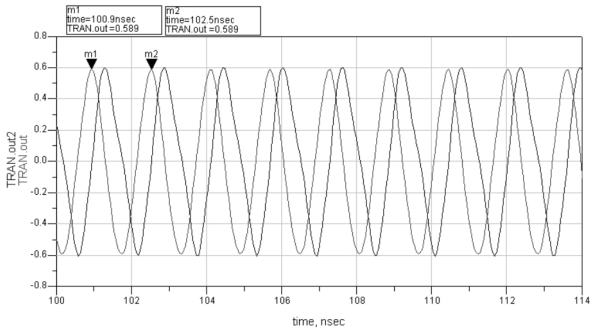


Figure 12: The simulation result of Voltage waveforms of oscillator

To verify and validate the good functionality of the proposed structure, we simulated the two structures (i.e. basic quadrature oscillator and proposed structures) under the same simulation conditions (R_2 = R_4 = 600Ω for the first structure and R_4=R_{Xa}+R_{Xb}=R_2=R_X=600Ω for the proposed structure). Figure 13 illustrates the oscillation frequency versus control bias current of $CCII_3$ (I_{o3}). The maximum relative difference between the frequencies determined for the two structures is less than 0.05%.

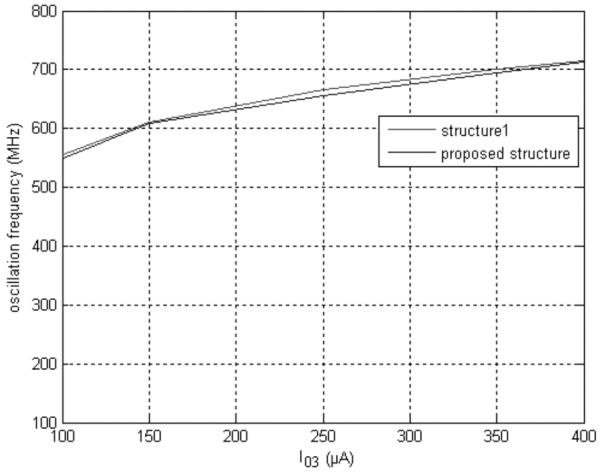


Figure 13: Oscillation Frequency versus control bias current (I_{03})

6 The new Voltage/Current Mode (VCM) current controlled quadrature Oscillator:

The evaluation of the high frequency circuits requires a voltage/current mode design. To transfer the Voltage-mode (VM) quadrature oscillator to a Voltage-Current-mode (VCM) quadrature oscillator, it is necessary to add two voltage/current conversion circuits shown in Figure 14 at the output stage. The voltage/current conversion uses one current conveyor (CCII). Figure 15 shows the ameliorated structure of the Voltage/Current mode quadrature oscillator.

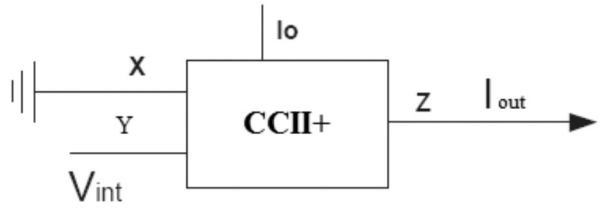


Figure 14: Voltage/current conversion

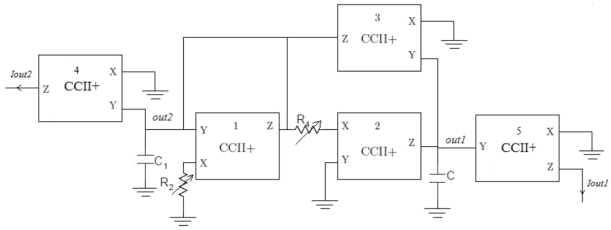


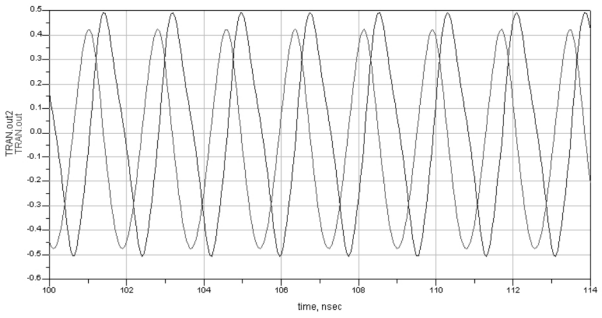
Figure 15: Proposed Voltage/Current mode Quadrature oscillator

The Voltage and Current responses of the VCM quadrature oscillator where C_1= C_5=0.3pF, R_4=R_{xa}+R_{xb}=R_2=Rx=600Ω (I_{oa}=I_{ob}=130μA and I_{o4}=40μA), I_{o3}=230μA and I_{o1}=I_{o2}= 400μA are given in Figure 16. The oscillation frequency is equal to 625MHz.

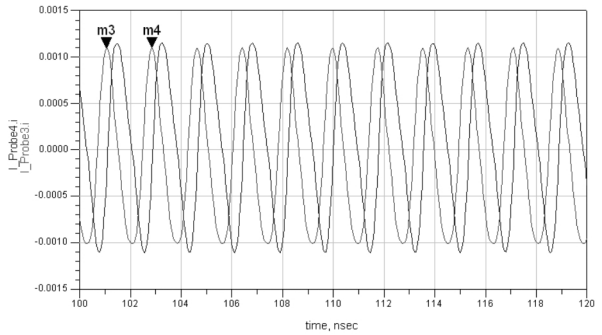
To verify and validate the good functionality, we simulated the VCM quadrature oscillator and the VM quadrature oscillator. Figure 17 illustrates the oscillation frequency versus control bias current of $CCII_3$ (I_{o3}). We notice a good agreement between both characteristics. From this Figure, we see that when varying the control current I_{o3} between 100μA and 400μA, the oscillation frequency is tuned in the range [555 MHz –714.2MHz].

7 Conclusion

In this paper, a new design of variable-frequency, current-controlled quadrature oscillator was proposed.



(a)



(b)

Figure 16: The simulation result of Voltage (a) and current (b) waveforms oscillator

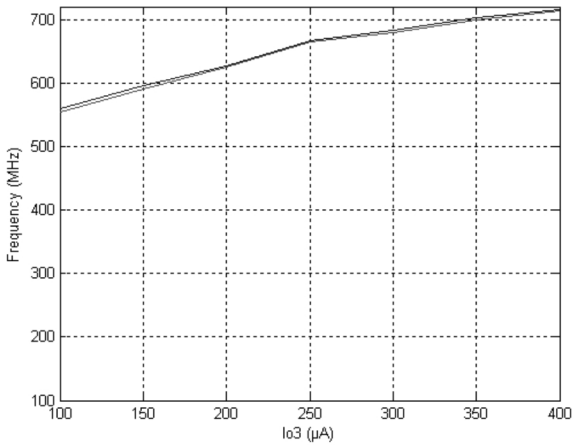


Figure 17: Oscillation Frequency versus control bias current (I_{03})

In order to get higher frequency performance of the quadrature oscillator, a translinear CCII structure is optimized in 0.18μm CMOS process of TSMC. Simulation results show that this oscillator provides an independent control of oscillation frequency and oscillation condition in the range [285MHz - 844MHz] by varying the control current in the range [30μ-400μA]. To validate these results, a comparison between both the proposed and the basic structures is performed. This study demonstrates that the maximum relative difference between the frequencies determined for the two

structures is less than 0.05%. Finally we have proposed a Voltage-Current mode quadrature oscillator. Simulation results show that the proposed VCM oscillator presents a control oscillation frequency between [555 MHz –714.2MHz] by varying the control current in the range of [100µ-400µA]

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