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Advanced gate control system for power MOSFET switching losses reduction with complete switching sequence control

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Abstract: To meet strict EMC requirements for power electronics applications driving an inductive load, it is often necessary to mitigate current and voltage transition slopes. Using the conventional MOSFET control method, the slope mitigation is commonly performed by modifying a series gate resistance, which results in high switching losses, long turn-on and turn-off delays and long final gate charging and discharging durations affecting the overall application efficiency. In order to improve this, a novel MOSFET control method is developed and presented in this paper. It enables a complete control over all intervals of the switching sequences utilizing the gate current shaping principle. Switching losses, delays and final gate charging and discharging durations can be kept as low as possible, as the method allows to mitigate only the critical transition. The design of the system allows its implementation in a broad spectrum of applications regardless of the current or voltage rating and with a minimal impact on the application design. The paper presents the detailed description of the proposed system operation and its realization as an integrated circuit. The efficiency measurements of the conventional and the advanced gate control methods are reported as well, showing significant advantages of the proposed system.

Keywords: Power MOSFET switching behavior; advanced gate control; gate current shaping; switching losses reduction; EMC in power electronics

Napredno krmiljenje vrat močnostnih MOSFET tranzistorjev za zmanjševanje preklopnih izgub z nadzorom nad celotno preklopno sekvenco

Izvleček: Za doseganje elektromagnetne skladnosti moramo v močnostni elektroniki pri napravah z induktivnim bremenom pogosto zmanjšati naklon toka ali napetosti med preklopi. Pri konvencionalni krmilni metodi to storimo s spreminjanjem serijske upornosti v vratih MOSFET tranzistorja. Slednje se odraža v povečanju preklopnih izgub, podaljševanju zakasnitev vklopa in izklopa ter podaljševanju trajanja končnega polnjenja in praznjenja vrat. Našteto zmanjšuje zmogljivost celotne naprave. Navedene pomanjkljivosti konvencionalne metode ublažimo z uporabo nove napredne krmilne metode, ki je predstavljena v tem članku. Deluje na principu spreminjanja toka, ki teče v vrata MOSFET tranzistorja ter omogoča nadzor nad dogajanjem v vsakem intervalu preklopne sekvence. Ker lahko na tak način omilimo le kritični naklon, sistem omogoča vzdrževanje minimalnih preklopnih izgub, zakasnitev in trajanj končnega polnjenja in praznjenja vrat. Sistem je zasnovan tako, da ga lahko vgradimo v širok spekter naprav, ne glede na napetostno ali tokovno zmogljivost in z minimalnim poseganjem v zasnovo same naprave. V članku je detajlno opisano delovanje predstavljenega sistema ter njegova realizacija v obliki integriranega vezja. Predstavljene so tudi meritve učinkovitosti konvencionalne in napredne kontrole vrat. Rezultati so občutno boljši v primeru uporabe predstavljenega sistema.

Ključne besede: Preklopi močnostnega MOSFET tranzistorja; napredno krmiljenje vrat; oblikovanje toka v vrata tranzistorja; zmanjševanje preklopnih izgub; EMC v močnostni elektroniki

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1 Introduction

The tradeoff between switching losses and electromagnetic emissions is often of great concern during the design of power electronic applications with an inductive load. Fast transitions of voltage and current at power switch (in this paper we are focusing on power MOSFETs) cause excessive emissions and oscillations, while slow transitions cause significant switching losses. To meet strict EMC requirements, slopes must often be limited, which is obviously done at the expense of increased switching losses.

Power MOSFETs are commonly driven via series gate resistor (R_g). Transition slopes are adjusted by changing R_g value but such approach is not the most effective. The problem is that changing R_g resistance influences all intervals of the switching sequence instead of mitigating only the critical transition that is responsible for emissions. This produces excessive switching losses, introduces long turn-on and turn-off delays and extends final gate charging and discharging durations. To improve this process, a different gate control method should be used to allow control over transition in each interval of the switching sequence independently.

Several papers [1–10] report improvements of the conventional control method with a gate resistor or propose entirely new control approaches that differ in functionality, complexity, efficiency and cost.

For example, the methods presented in [1], [2], [4], [7] focus only on the mitigation of turn-off voltage overshoot and the following oscillations, which are often an issue especially among IGBT circuits. Papers [5], [8] introduce the combined control over turn-off voltage and turn-on current transition. The latter is usually of great concern, as the current slope impacts reverse recovery severity, it may induce oscillation and it strongly impacts the emissions rate. The method [9] focuses on the acceleration of turn-on voltage fall and minimization of the turn-off delay. The most comprehensive approaches are reported by Rose [3], Park [6] and Lobsiger [10] demonstrating current and voltage transition control during the turn-on and the turn-off. None of the presented methods, however, addressed control over the whole duration of the switching sequence.

The presented control methods are based on significantly different principles for the operating point detection of the controlled MOSFET (or IGBT), which is an essential part of any advanced control method. Certain methods [2], [6], [7], [10] use capacitor or special differentiator circuit connected to the transistor drain (or collector) terminal. Despite being simple and low-cost, such approach may be susceptible to noise [4] and oscillations that potentially mask the actual voltage transition resulting in an inappropriate control procedure. On the other hand, methods [3], [4], [6], [10] exploit intrinsic inductances from the physical circuit to detect the current transitions. Such system may be found difficult to implement, taking into account diverse layout topologies, current slopes and ratings.

Gate control approach as presented in this paper aims to enable control over transitions in all intervals of the switching sequences and to use such operating point detection principle that allows system implementation in various applications regardless of voltage or current ratings and with a minimal impact on the circuit layout design.

Presented system is also a subject of PCT patent application.

Paper is organized in the following order: section 2 presents the inductive load switching sequence, switching losses and EMC overview and provides an explanation about the conventional gate control drawbacks; section 3 describes the concept of the proposed gate control system; section 4 presents system realization as an integrated circuit; section 5 presents system measurements, results and discussion, while section 6 concludes the paper.

2 Switching sequences, switching losses and EMC

A short insight into a well known switching behaviour of a MOSFET with a clamped inductive load is given first in order to present switching losses and electromagnetic emission (EM) generation and to underline the importance of the advanced gate control introduction.

A clamped inductive load circuit, presented in Figure 1, is comprised of MOSFET M_1, inductive load (L_{load}), freewheeling diode (D_{fwd}, which is the intrinsic diode of permanently closed MOSFET M_2), driving circuit (V_{gg} and R_g), MOSFET M_1 intrinsic capacitances (C_{gs} and C_{gd}) and supply voltage source V_{bat}. The corresponding switching waveforms of M_1 turn-on and turn-off sequences are shown in Figure 2 [11]. Just before the t_0, the initial conditions in the circuit are as follows: v_{gg}=0 and v_{gs}=0, so M_1 is switched-off (i_d=0); due to previous excitations, inductor L_{load} drives current I_0 through D_{fwd} (i_{fwd}=I_0), and since D_{fwd} is forward-biased, v_{ds} equals V_{bat}.

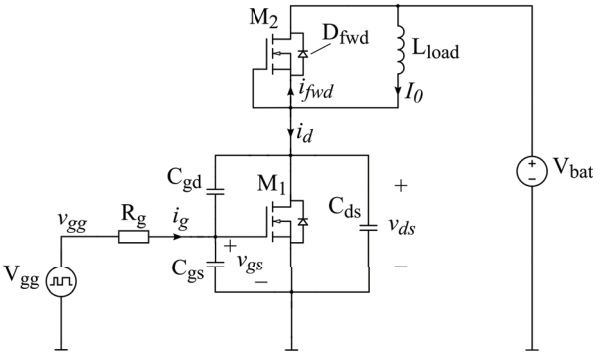

Figure 1: Clamped inductive load circuit

The turn-on sequence starts with the interval T_1 (turn-on delay) at $t=t_0$, when V_{gg} turns-on ($v_{gg}=V_{gg}$) and starts charging C_{gs} (Figure 2a). As v_{gs} reaches the threshold voltage V_{th} at the beginning of the interval T_2, M_1 starts conducting (Figure 2b) and taking over the load current I_0 from D_{fwd}. When i_d rises to I_0, i_{fwd} falls to zero, so D_{fwd} can be reverse-biased; the reverse-recovery process takes effect manifesting as M_1 drain current overshoot. During the whole interval T_2, the forwardly biased D_{fwd} clamps v_{ds} to V_{bat} level. In the interval T_3, v_{ds} drops as C_{gd} is discharged (Figure 2c). The total current from V_{gg} is now diverted to C_{gd}, causing v_{gs} to remain constant at the Miller plateau (V_μ). After v_{ds} drops to $V_{ds,on}$ (a consequence of M1 channel resistance), C_{gs} starts charging again and v_{gs} is rising again towards V_{gg} in T_4. The turn-on is thus accomplished [11] [12].

The turn-off occurs in a similar manner. It begins with V_{gg} going low at $t=t_0'$, followed by a turn-off delay interval T_4', in which v_{gs} falls to Miller plateau, as C_{gs} is discharged (Figure 2e). Beyond $v_{gs}=V_\mu$, further C_{gs} discharging requires drain current reduction, which is impossible at that moment, since D_{fwd} is reverse biased ($V_{bat}>v_{ds}$) and cannot take over load current (I_0) yet. Therefore, v_{ds} rises first in T_3' (Figure 2g). When v_{ds} meets V_{bat}, I_0 can eventually be diverted to D_{fwd}, so M_1 drain current (i_d) falls in T_2' (Figure 2f). At $v_{gs}=V_{th}$, M_1 closes ($i_d=0$, $i_{fwd}=I_0$) and only v_{gs} remains to drop to zero in T_1', thus terminating turn-off sequence [11].

The review of the switching sequences shows that the current (i_d) transitions in T_2 and T_2' occur at the full voltage (v_{ds}) on M_1. Similarly, voltage (v_{ds}) transitions in T_3 and T_3' occur at the maximum drain current. This results in high power dissipation, $p_{sw}=i_d \cdot v_{ds}$. The integrals of p_{sw} over T_2 and T_3 for turn-on (1) and over T_2' and T_3' for turn-off (2) determine the turn-on ($E_{sw,on}$) and turn-off ($E_{sw,off}$) switching losses (Figure 2d and h) [11] [12].

$$E_{sw,on} = \int_{T2,T3} p_{sw}(t)\,\mathrm{dt} = \frac{1}{2} I_0 V_{bat} (T_2 + T_3) \qquad (1)$$

$$E_{sw,off} = \int_{T2',T3'} p_{sw}(t)\,\mathrm{dt} = \frac{1}{2} I_0 V_{bat} (T_2' + T_3') \qquad (2)$$

The dissipated energy, manifested as heat, is the root cause of several engineering challenges. Most importantly, it is necessary to provide adequate heat sinking, which often results in a bulky and expensive design and presents a limit for the application implementation. Moreover, elevated application temperature results in increased degradation rate of assembly components and impact general system reliability. As switching losses may present an important source of heating, their minimization is of great concern [13].

It is also well established that current and voltage transitions in T_2, T_2' and T_3, T_3' are the main source of electromagnetic emissions in power applications. High *di/dt* and *dv/dt* rates in conjunction with inductive and capacitive coupling cause conducted (and indirectly also radiated) differential (DM) and common mode (CM) emissions. Moreover, *di/dt* and *dv/dt* could excite oscillations and overshoots in resonant circuits (formed by parasitic inductances and capacitances), producing additional emissions and affecting the system reliability. There are several mechanisms available to mitigate emissions and oscillations (to meet EMC standards), each with its own trade-offs. One possibility is obviously to decrease *di/dt* and *dv/dt* rates (i.e. extend intervals T_2, T_3, T_2' and T_3') and eliminate the emissions origin, but at the expense of additional switching losses. We can furthermore tweak layout or insert additional components, such as snubber circuits or blocking capacitors, which usually involves a lot of prototyping and has only limited effect. Another possibility is the implementation of CM and DM filters, which is an effective but bulky and expensive solution. Most designs require to utilize all of the above, each in the scope of its own trade-offs and affected application characteristics [13][14]. On the other hand, any improvement of the described mechanisms eases the application design and boosts its efficiency.

This paper presents one of such improvements, which deals with the MOSFET control circuit and increases slope adaptation mechanism efficiency. The main drawback of the conventional method employing a series gate resistor R_g is that increasing the gate circuit resistance in order to reduce critical current or voltage slopes prolongs all intervals in corresponding switching sequence. First, it causes excessive switching losses in T_2, T_2', T_3 or T_3', as it extends both current and voltage transitions. Moreover, an extension of T_1 and T_4' has a negative impact on applicability of some control algorithms, as it requires longer dead-times and in turn also produces higher diode D_{fwd} losses [12]. Extension of T_4 or T_1' affects the system reliability in terms of the unintentional turn-on / turn-off immunity.

Introduction of the advanced gate control system presented in this paper, which allows setting the duration of each interval of the switching sequence separately, extends the margins where slope adaptation effectively improves the application efficiency.

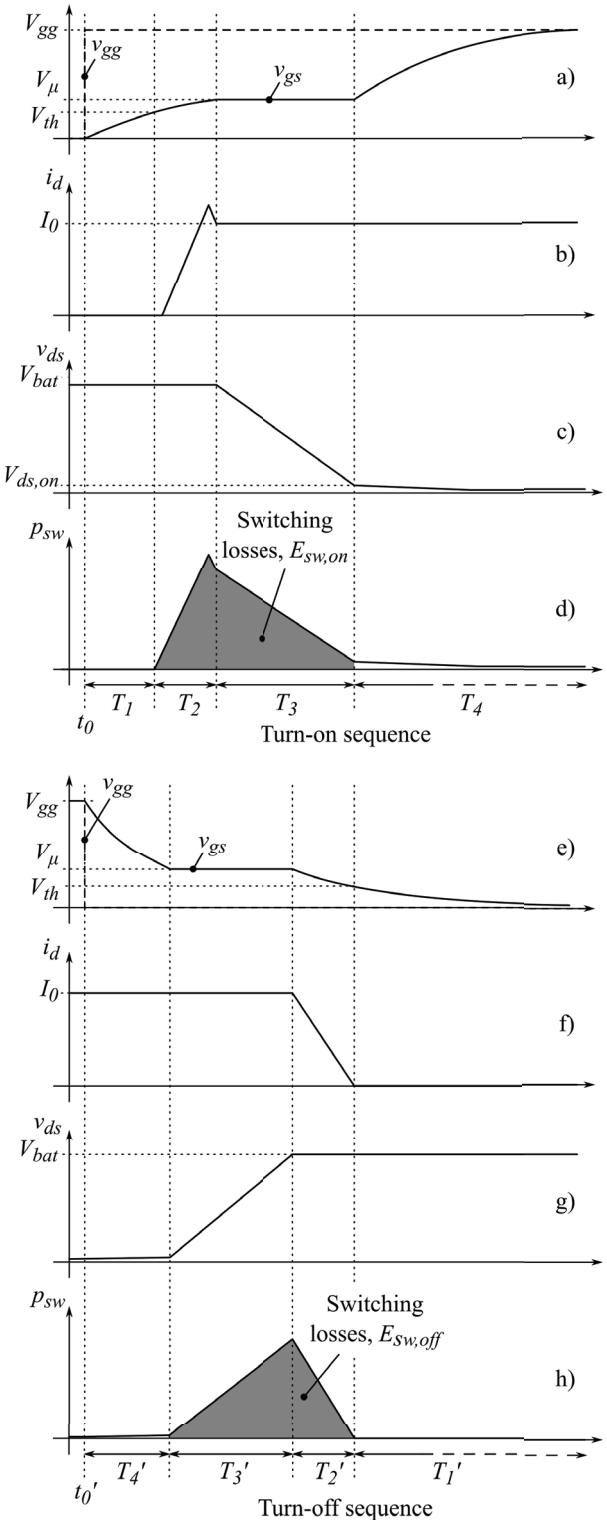

Figure 2: Switching sequence waveforms

3 Advanced gate control system

Figure 3 depicts the block diagram of the advanced gate control system presented in this paper. The system is constructed of two main units, namely the current sources unit and the control circuit unit. The role of the first is to feed the power MOSFET gate, while the second unit monitors the power MOSFET operating point, detects the ongoing switching sequence interval and produces control signals for the current sources unit. Each unit operation is explained in detail in the following sections.

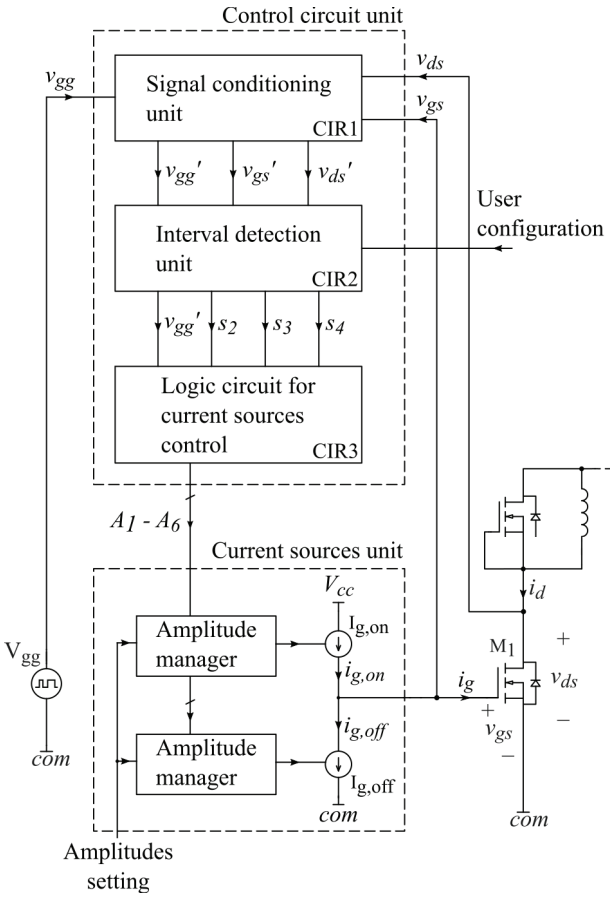

Figure 3: Advanced gate control system block diagram

3.1 Current sources unit

The advanced gate control system (Figure 3) is based on the power transistor gate current shaping (i_g) principle, implemented using two controlled current sources ($I_{g,on}$ and $I_{g,off}$) that charge and discharge the transistor input capacitance during its turn-on and turn-off. Each source amplitude can be individually set in each interval of the switching sequences.

By adjusting the gate current (i_g) in each interval, the charge flow rate to the gate is governed and hence the rate of change of each interval transition can be indi-

vidually controlled. We can therefore adjust each current and voltage slope (*di/dt* and *dv/dt*) in intervals T_2, T_3, T_2' and T_3' and also minimize turn-on and turn-off delays in T_1 and T_4' and the duration of the final gate charging and discharging in the intervals T_4 and T_1'. An example of the advanced gate control operation is shown in Figure 4.

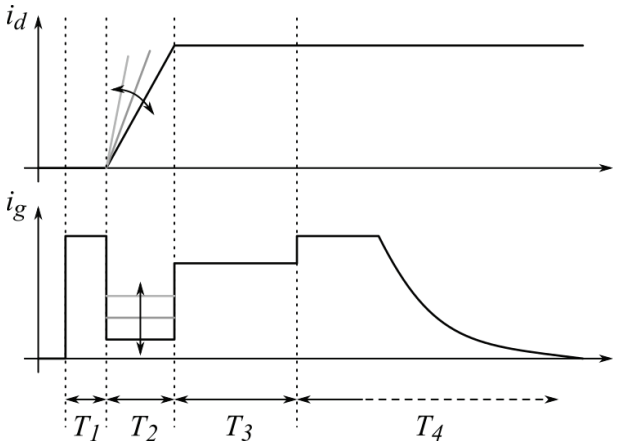

Figure 4: By shaping gate current ig drain current slope is being controlled

The presented gate control approach can improve the conventional gate control drawback where all interval transitions are influenced simultaneously with R_g adaptation. Determining the optimal point of the trade-off between switching losses and electromagnetic emissions is thus much more effective. In most situations, less switching losses are produced for the same rate of electromagnetic emissions. Delays and final gate charging and discharging durations can also be minimized.

The i_g amplitude adjustment throughout the switching intervals is performed by the amplitude manager system. It enables the user to set the desired interval amplitude levels and control the $I_{g,on}$ and $I_{g,off}$ current sources. The operation of the amplitude manager is based on the information about the ongoing interval, which is obtained from the control circuit unit. Amplitude managers and current sources are implemented as current mirrors, described in detail in section 4.

The current sources are supplied with voltages (V_{cc}) equal to gate-source voltage (v_{gs}) required for power transistor full turn-on (typically 12V for common power MOSFETs).

3.2 Control circuit unit

The role of the control circuit unit is to detect borders between the intervals of the switching sequence and to subsequently send information about the ongoing interval to the current sources block. It consists of three subunits, namely the signal conditioning unit (CIR1), interval detection unit (CIR2) and logic circuit for the current sources control (CIR3).

3.2.1 Signal detection and Signal conditioning unit

The signal conditioning unit (CIR1) accepts signals v_{ds} and v_{gs} from the MOSFET and the control signal v_{gg} (usually from a microcontroller). To understand why it is necessary to monitor v_{ds} and v_{gs}, we must first take a look at the interval detection principle. The interval borders are associated with specific events, marked with points N_0, N_2, N_3 and N_4 for turn-on and F_0, F_4, F_3 and F_2 for turn-off in Figure 5 and explained in Table 1. As evident from Figure 5, the points are located on v_{ds}, v_{gs} and v_{gg}, which means that these signals provide full information about the ongoing interval. It should be emphasized that the points are located exclusively on the voltage signals that are commonly present in each inductive load circuit. This is an important advantage of the presented system, as it enables an implementation in various power applications regardless of voltage or current rating.

Table 1: Interval border points explanation

Point	Start of interval	Associated event
N_0	T_1	Start of TURN-ON sequence, vgg starts rising
N_2	T_2	vgs reaches threshold voltage Vth
N_3	T_3	vds starts falling
N_4	T_4	vds drops to the final value
Power transistor is ON		
F_0	T_4'	Start of TURN-OFF sequence, vgg starts dropping
F_4	T_3'	vds starts rising
F_3	T_2'	vds rises to the final value
F_2	T_1'	vgs drops to the threshold voltage
Power transistor is OFF		

Before point sensing and interval detection, the input signals v_{ds} and v_{gs} are processed by the signal conditioning unit (Figure 6). Signals must be filtered first to eliminate high-frequency oscillations that commonly occur during the power transistor switching. The filters must be carefully designed to keep their time constant small compared to the switching sequence interval durations. The control signal v_{gg}, which is a logic signal, must be voltage-matched to meet the comparator input requirements.

3.2.2 Interval detection unit

After filtering, the signals are passed to the interval detection unit (CIR2) that outputs the signals s_2, s_3 and s_4

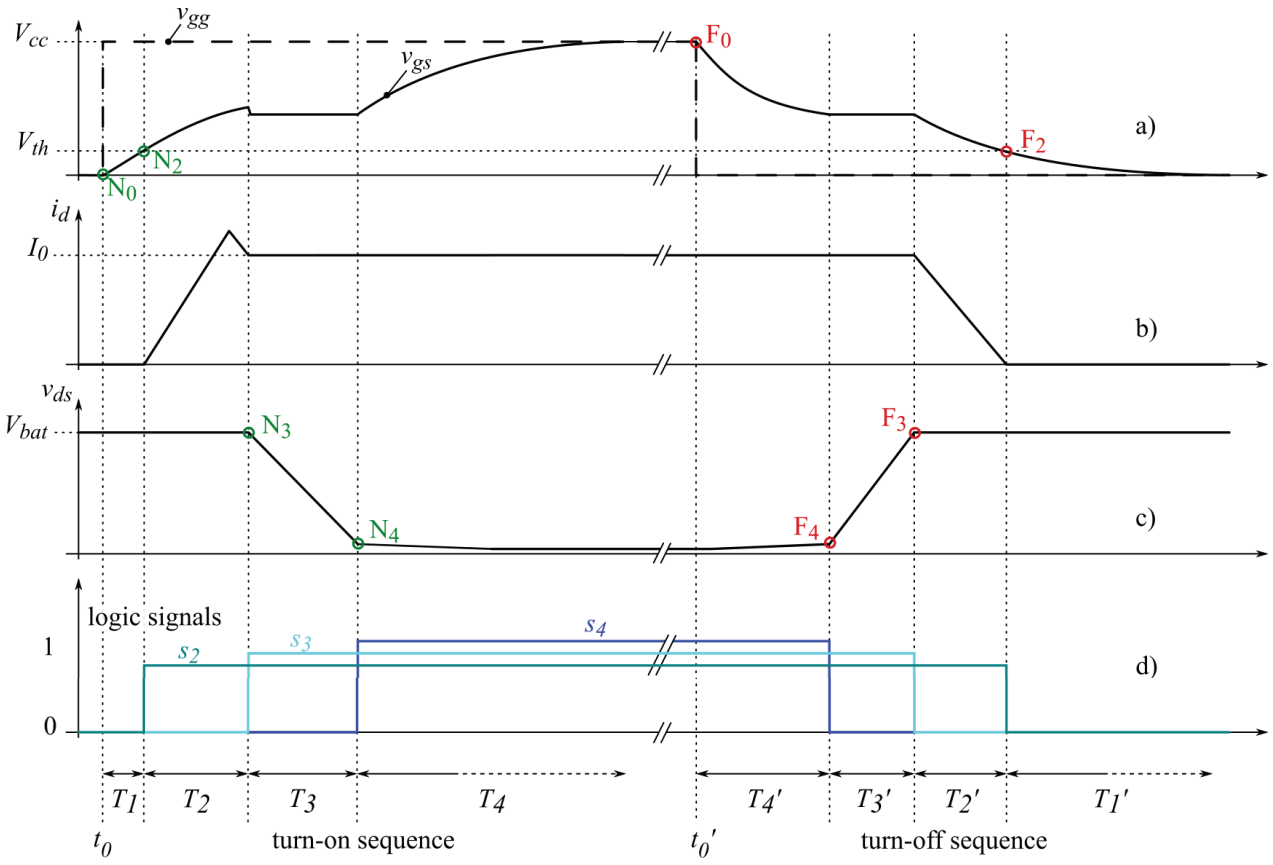

Figure 5: Switching sequence with N and F points

(Figure 5 d), which provide full information about the ongoing interval (by forming a unique combination in each interval) in conjunction with v_{gg}. Each of the three signals is set high and then low at two points: s_2 at N_2 and F_2, s_3 at N_3 and F_3, and s_4 at N_4 and F_4 respectively (Figure 5). Since each point pair detection and corresponding output signal generation follows the same principle and utilizes an identical circuit (depicted in Figure 7), a common explanation is applicable hereafter, where the input signal stands for v_{gs}' and v_{ds}' and the output signal for s_2, s_3 and s_4. For s_2, the input signal is v_{gs}', while for s_3 and s_4 generation, the input signal is v_{ds}'. Since v_{gg}' is a logic signal, the detection of points N_0 an F_0 does not require utilizing the circuit from Figure 7. The v_{gg}' transition detection is carried out in the logic circuit for current sources control unit (CIR3).

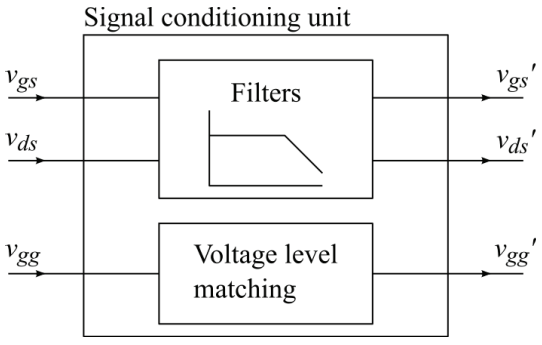

Figure 6: Signal conditioning unit (CIR1)

As evident from Figure 7, the input signal v_{gs}' or v_{ds}' crossing a certain level at points N_i or F_i is sensed by the comparator (U_1 and U_2). The point levels are user-configured by adapting the input voltage dividers (R_1-R_2) and (R_3-R_4). In case that a voltage signal at a compara-

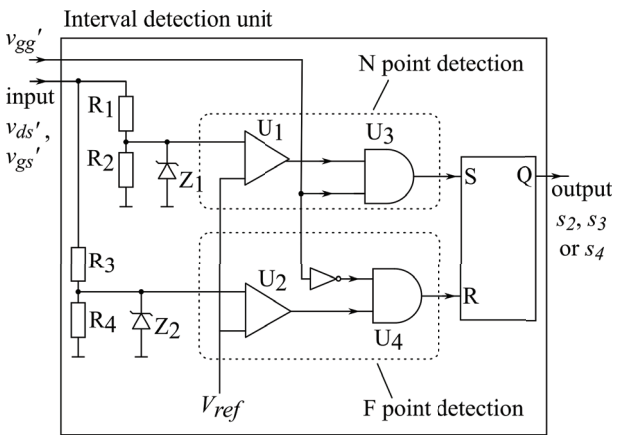

Figure 7: Interval detection unit (CIR2) – one out of three identical circuits is depicted.

tor input exceeds its rating, the Zener diodes Z_1 and Z_2 start clamping to protect the comparator inputs. To ensure that N_i and F_i points are detected exclusively during turn-on and turn-off sequences and to prevent flip-flop mistriggering, the AND gates U_3 and U_4 with applied v_{gg}' and $\overline{v_{gg}}'$ inputs are inserted to generate a sequence-matching window for passing comparator output signal. When a point crossing is detected, a SR flip-flop input is triggered: *S* input at N_i and *R* input at F_i point detection, which generates a *Q* signal that matches the desired output signal waveforms s_2, s_3 or s_4, Figure 5.

Using flip-flops for the interval detection is also important to ensure the immunity to oscillations, as SR flip-flops react only on the first input triggering. Therefore, comparator input signal oscillation around V_{ref} (which results in comparator output alternating) has no effect on the s_2, s_3 or s_4 waveforms.

3.2.3 Logic circuit for current sources control

The signals s_2, s_3 and s_4 are passed to the logic circuit CIR3 (Figure 3) that together with the signal v_{gg}' produces the controlling signals A_1 to A_6 for the current sources unit. The operation of this unit follows the selected current sources control scheme, which is described in detail in the next section.

4 System implementation

The system is implemented as an IC in a 250 nm TSMC technology (Figure 10). The circuit integration is essential for an efficient system embodiment. First, it enables short propagation delay of the controlling circuit, which is crucial to be small in comparison to the interval durations allowing the management of switching transients. To make our system implementable in applications with expected switching transient durations of 100ns, it is considered that signal propagation delay must not exceed 10 ns, which is likely unachievable using discrete components. Furthermore, the integration allows an efficient realization of current sources and amplitude managers in the form of integrated current mirrors. An important integration benefit is also minimization of the system physical dimensions.

The purpose of the system implementation presented in this work is to prove the concept of the described system. In order to simplify the system development and future research, only the crucial parts are integrated. According to Figure 3, these are the current sources unit with the exception of resistors the R_{ref1} to R_{ref6} (Figure 8), logic circuitry for controlling current sources and the interval border detection unit with the exception of input voltage dividers (R_1, R_2 and R_3, R_4 in Figure 7). The system is supplied with two voltage levels, 5 V for the controlling circuit and 12 V (V_{cc}) for the current sources unit.

4.1 Current sources unit realization

Figure 8 presents a realization of the current sources unit with integrated current mirrors. The transistors M_{h0} and M_{l0} present a physical implementation of the current sources $I_{g,on}$ an $I_{g,off}$ (from Figure 3), while the rest of the circuit embodies the corresponding amplitude managers. The unit is divided into a high-side and low-side subcircuit, each consisting of three channels (two of them depicted dimmed) that enable setting different $i_{g,on}$ and $i_{g,off}$ amplitude levels and shape the gate current (i_g) during switching sequence intervals.

The amplitude levels are user-defined by adjusting the R_{ref1} to R_{ref6} resistor values (not part of IC) that determine current mirror reference currents for each channel (i_{r1}, i_{r2}, i_{r3} and i_{r4}, i_{r5}, i_{r6}). The reference currents are mirrored to i_{h2}, i_{h2}', i_{h2}'' and i_{l2}, i_{l2}', i_{l2}''. A single mirror is required for the high side subcircuit, while the low side requires two mirroring stages for the $I_{g,on}$ and $I_{g,off}$ source and sink realization. The mirrored currents are then combined into i_{h1} and i_{l1} ($i_{h1}=i_{h2}+i_{h2}'+i_{h2}''$ and $i_{l1}=i_{l2}+i_{l2}'+i_{l2}''$) that present the reference currents for the M_{h1}-M_{h0} and M_{l1}-M_{l0} current mirrors and in turn determine the $i_{g,on}$ and $i_{g,off}$ waveforms. Each output current therefore consists of three components and can be defined as (3) and (4), where *M* indicates the total current mirror multiplication factor. In this design, *M* equals 1000.

$$i_{g,on}(t) = M \cdot i_{r1}(t) + M \cdot i_{r2}(t) + M \cdot i_{r3}(t) \quad (3)$$

$$i_{g,off}(t) = M \cdot i_{r4}(t) + M \cdot i_{r5}(t) + M \cdot i_{r6}(t) \quad (4)$$

To set the i_g amplitude in each interval separately, the transistors M_{h3}, M_{h3}', M_{h3}' and M_{l3}, M_{l3}', M_{l3}'' are utilized, controlled by the A_1 to A_6 signals from the logic circuit for current sources control CIR3 (Figure 3). The transistors act as switches and take over the reference currents i_{r1} to i_{r6} from M_{h2}, M_{h2}', M_{h2}'' and M_{l2}, M_{l2}', M_{l2}''. This causes zero current mirroring in the corresponding channels and consequently zero i_{h2}, i_{h2}', i_{h2}'', i_{l2}, i_{l2}' or i_{l2}'' contribution in the formation of the i_{h1} and i_{l1} currents, which, as presented, impact the $i_{g,on}$ and $i_{g,off}$ amplitudes.

To put it briefly, the gate current i_g shaping is embodied by the switching signals A_1 to A_6 throughout intervals which define the appropriate current components from the expressions (3) and (4) to form the $i_{g,on}$ and $i_{g,off}$ currents at a given time. The $i_{g,on}$ and $i_{g,off}$ amplitude levels are set by adjusting the reference currents by the external R_{ref1} to R_{ref6} resistors.

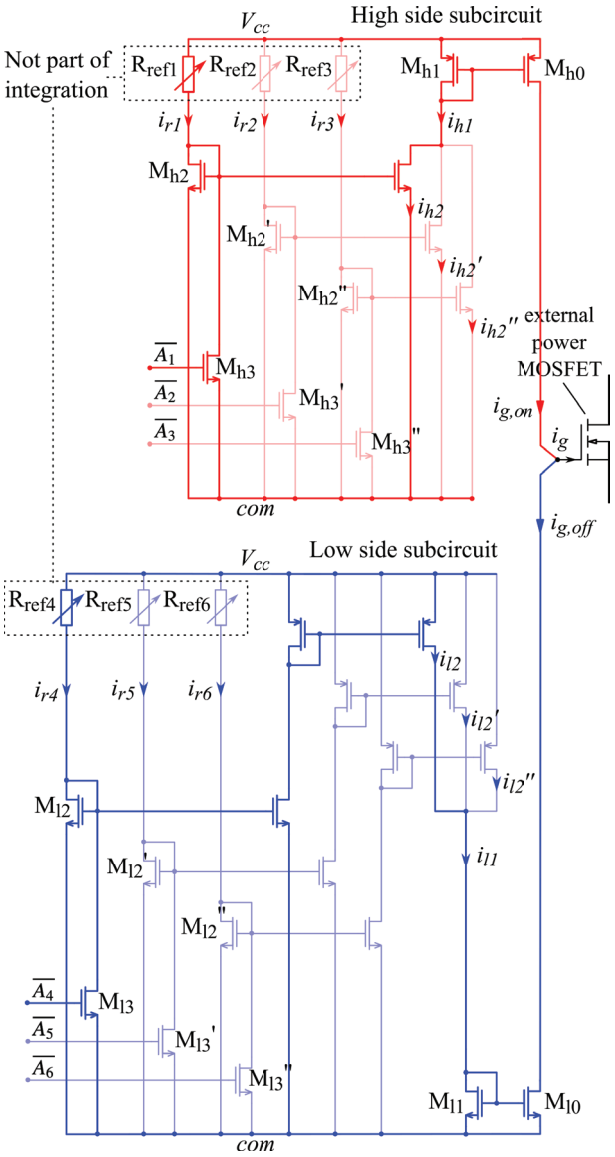

Figure 8: Schematic of current sources unit and corresponding amplitude managers (High side subcircuit for $I_{g,on}$ and Low side subcircuit for $I_{g,off}$)

4.2 Current sources controlling scheme

In each interval, a particular A_1 to A_6 signal combination is provided by logic circuit for current sources control (CIR3) to ensure fast and smooth current shaping. The resulting $i_{g,on}$ and $i_{g,off}$ current composition of multiplied reference currents ($M{\cdot}i_{r1}$ to $M{\cdot}i_{r6}$) is presented in Figure 9.

As evident, the $i_{g,on}$ and $i_{g,off}$ components $M{\cdot}i_{r2}$ and $M{\cdot}i_{r6}$ are present during the whole turn-on and turn-off sequences. Regarding the turn-on, in the intervals T_1 and T_4 $M{\cdot}i_{r1}$ is added to $M{\cdot}i_{r2}$ to minimize the delay and final gate charging duration. During T_2, only $M{\cdot}i_{r2}$ is available – the power transistor current slope is usually the one requiring the strongest mitigation and therefore requires the lowest gate current. The voltage slope in T_3 is managed by $M{\cdot}i_{r2}$ and $M{\cdot}i_{r3}$.

A similar operation refers to the turn-off: $M{\cdot}i_{r6}$ and $M{\cdot}i_{r4}$ in T_4' minimize the turn-off delay, and $M{\cdot}i_{r6}$ and $M{\cdot}i_{r5}$ determine the voltage slope in T_3'. Only $M{\cdot}i_{r6}$ component is present during the current transition in T_2'. Since the duration of the input capacitances discharging in T_1' is already limited by the low power transistor v_{gs} voltage and intrinsic resistances, only the $M{\cdot}i_{r6}$ component is provided.

During the turn-on sequence, $i_{g,off}$ equals zero, and similarly, $i_{g,on}$ equals zero during the turn-off.

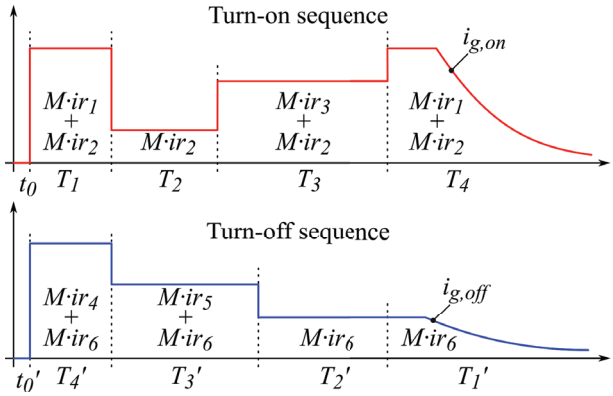

Figure 9: composition of $i_{g,on}$ and $i_{g,off}$ currents

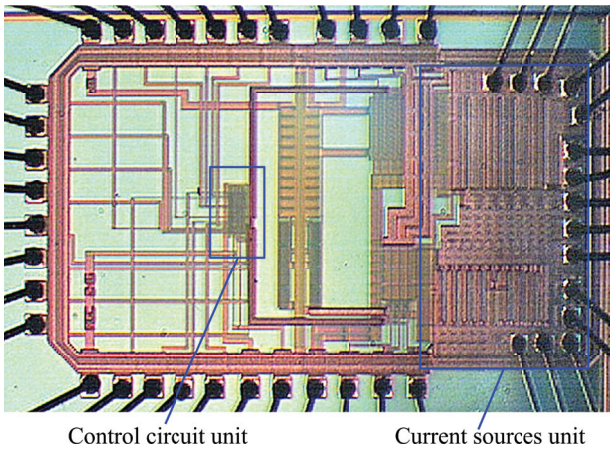

Figure 10: A microphotograph of the advanced gate control ASIC. IC dimensions approx. 1502 um x 2430 um

5 Testing, results and discussion

5.1 Test setup

To investigate the efficiency, the advanced gate control system is compared to the conventional control method with the series gate resistance. The test is carried out using a common inductive load circuit, as depicted

in Figure 11 (the circuit basic operation is already described in Section 1). Between the gate and the source terminals of MOSFET M_1, a 10 kΩ resistor and a 10 nF capacitor are inserted to emulate realistic conditions. The two components are often inserted in power circuits to improve immunity against unintentional turn-on and to mitigate the Miller effect consequences. MOSFET M_1 can be driven with the advanced or conventional control method, while the drain-source voltage (v_{ds}), the gate-source voltage (v_{gs}) and the drain current (i_d) are monitored with the oscilloscope. To measure the i_d current, a Rogowski coil is utilized. The MOSFETs M_1 and M_2 are both Infineon IPB010N06N.

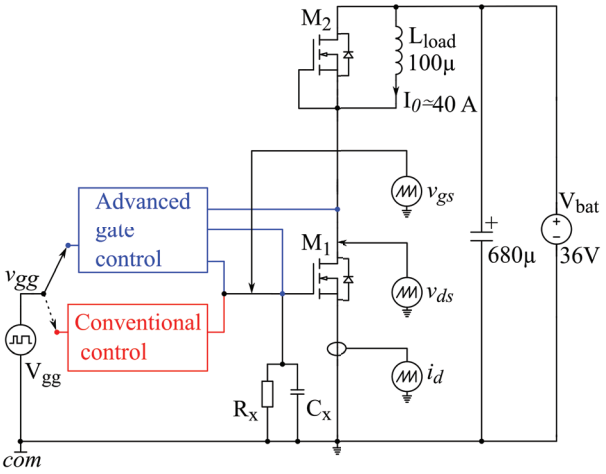

Figure 11: The test circuit schematics

The waveform generator V_{gg} (Agilent 33500B) is programed to produce a pulse shown in Figure 12. During the interval T_{charge}, M_1 is open. In this interval, the current through L_{load} rises up to the desired value I_0, in this case 40 A. After that, M_1 is switched off and i_d is diverted into M_2's diode, which produces the required initial conditions to observe the turn-on and turn-off switching sequences at the following v_{gg} fronts. The time between the last three changes of v_{gg} is kept low (20 us) to produce only minimal change in i_d.

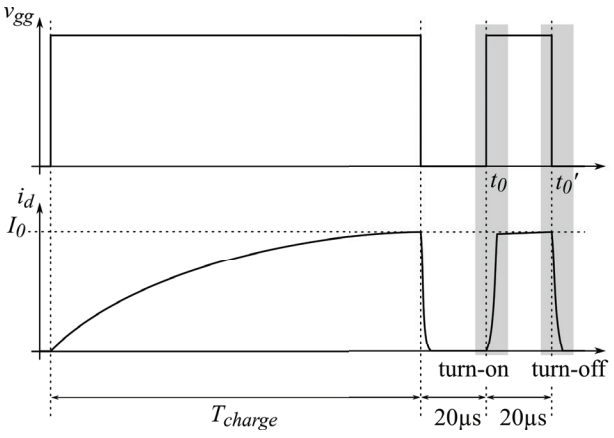

Figure 12: v_{gg} and corresponding i_d waveforms

The advanced gate control from Figure 11 as such is described in previous sections. In the signal conditioning unit, first order low-pass filters are employed comprising of 10 kΩ resistor and 1 pF MLCC capacitor. Resistors R_{ref1} to R_{ref6} are trimmer potentiometers with 2 MΩ track resistance. The conventional control is composed of a special driver (IR AUIRS2191S) and the series gate resistor R_g.

The efficiency of the two methods is observed by comparing turn-on and turn-off switching losses, delays, and final charging / discharging durations at different values of the drain current rise or fall time. This figure of merit is chosen, as the current transitions are considered the most critical, since they are usually faster than voltage transitions and their mitigation produces greatest amount of surplus switching losses. Moreover, the comparison of current rise and fall times are more accurate, since the current transitions are not affected by parasitic elements in such extent as the voltage transitions.

Definitions of the observed parameters are shown in the Table 2.

Table 2: Parameters definitions

Parameter	Definition
Current rise time ($t_{id,rise}$)	i_d=10% I_0 to i_d=90% I_0
Current fall time ($i_{d,fall}$)	i_d=90% I_0 to i_d=10% I_0
Voltage rise time ($v_{ds,rise}$)	v_{ds}=10% V_{bat} to v_{ds}=90% V_{bat}
Voltage fall time ($v_{ds,fall}$)	v_{ds}=90% V_{bat} to v_{ds}=10% V_{bat}
Turn-on delay	v_{gs}=10% V_{cc} to i_d=10% I_0
Turn-off delay	v_{gs}=90% V_{cc} to v_{ds}=10% V_{bat}
Turn-on final charging	v_{ds}=10% V_{bat} to v_{gs}=90% V_{cc}
Turn-off final discharging	i_d=10% I_0 to v_{gs}=10% V_{cc}
Turn-on switching losses ($E_{sw,on}$)	$E_{sw,on} = \int_{t_1}^{t_2} i_d v_{ds} dt$ t_1 when i_d=10% I_0 t_2 when v_{ds}=10% V_{bat}
Turn-off switching losses ($E_{sw,off}$)	$E_{sw,on} = \int_{t_1}^{t_2} i_d v_{ds} dt$ t_1 when v_{ds}=10% V_{bat} t_2 when i_d=10% I_0

5.2 Measurements and results

Figure 13 first shows an example of the advanced gate control operation. The graphs present three turn-on switching sequence waveforms (i_d, v_{ds} and v_{gs}). Each time a different setting for i_{ref3} is applied (by adjusting R_{ref3} trimmer resistor) in order to manipulate v_{ds} fall time. Specifically, the i_{ref3} current is set to 1.7 mA, 706 µA and 63 µA, while the currents i_{ref1} and i_{ref2} are constant in all three cases and set to 370 µA and 39 µA respectively. It should be noted that the voltage drop that occurs during the current transition (while $M{\cdot}i_{r2}$ is active) is a consequence of the voltage induction on parasitic inductances due to the relatively high *di/dt* rate being present and cannot be manipulated with the advanced gate control system. However, the last part of v_{ds} drop that can be influenced clearly underlines the system key advantage. While keeping the drain current rise time constant (at around 200 ns), the voltage drop rate could be boosted (in regards to the emission generation) thus reducing switching losses.

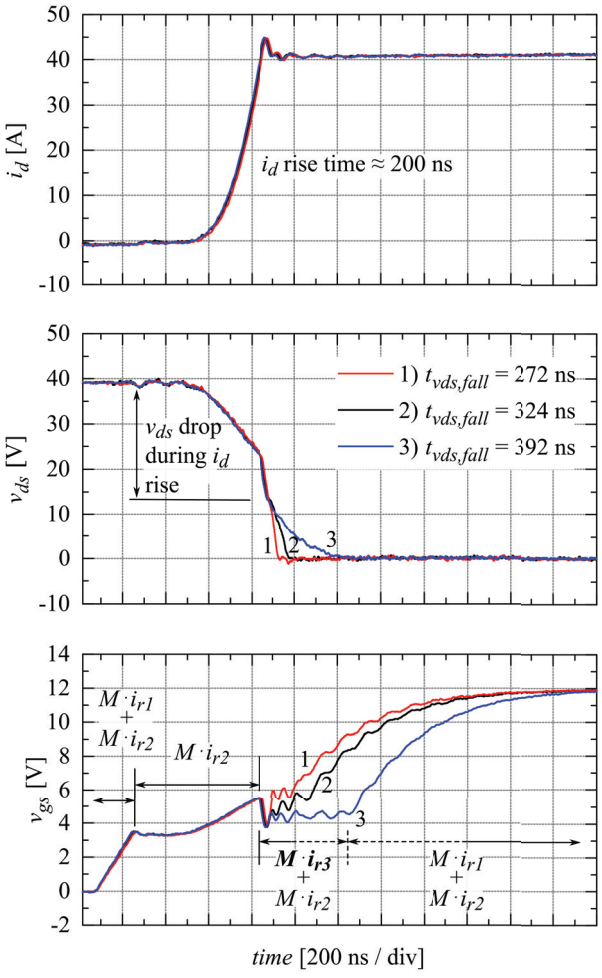

Figure 13: Advanced gate control operation, turn-on sequence oscillograms. Different $t_{vds,fall}$ are applied at the same $t_{id,rise}$.

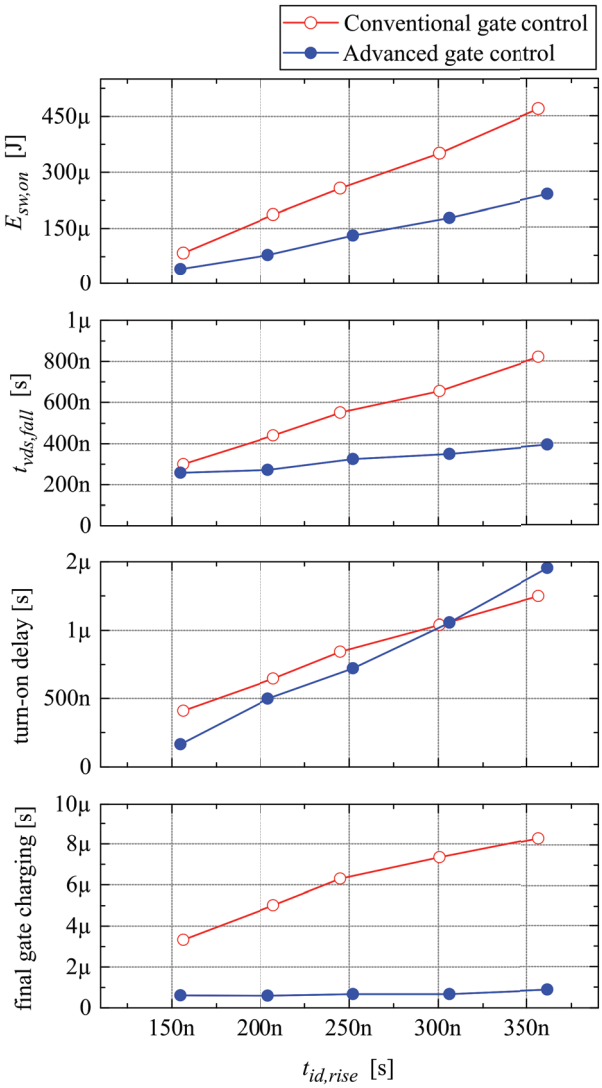

Figure 14: Comparison of the conventional and the advanced gate control methods, turn-on

To compare the two methods, the efficiency measurements are performed first with the conventional gate driving method using different gate resistor R_g values. For the turn-on, 39 Ω, 68 Ω, 90 Ω, 120 Ω and 150 Ω are used, which results in the following i_d rise times: 156 ns, 208 ns, 245 ns, 300 ns and 357 ns respectively. Similarly, for the turn-off, 47 Ω, 82 Ω, 100 Ω, 120 Ω and 150 Ω R_g values are applied, producing 141 ns, 201 ns, 246 ns 277 ns and 346 ns i_d fall times. The corresponding turn-on and turn-off parameters from Table 2 are obtained by processing waveforms acquired from the oscilloscope.

Similar measurement is carried out using the advanced gate control system. This time, trimmer resistors R_{ref1} to R_{ref3} for the turn-on and R_{ref4} to R_{ref6} for the turn-off from Figure 8 are adjusted to manipulate switching sequence transitions. Such resistor values are chosen that v_{ds} rise and fall times, delays and final charging and dis-

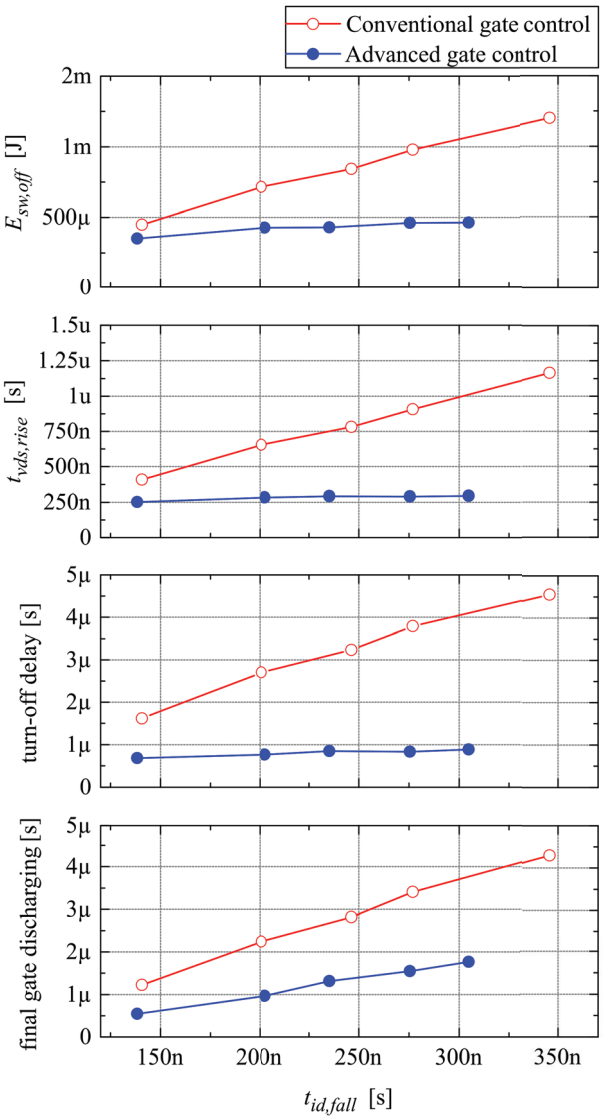

Figure 15: Comparison of the conventional and the advanced gate control methods, turn-off

charging durations are kept as low as possible, while i_d rise and fall times are matched to the values obtained using R_g control method. Again, turn-on and turn-off parameters from Table 2 are obtained by processing waveforms acquired from the oscilloscope.

The results of the comparison of the two methods are presented in Figure 14 and Figure 15.

Figure 14 and Figure 15 show that the extending drain current (i_d) rise and fall times produce notably less switching losses, shorter turn-off delay and shorter final charging and discharging durations when using the advanced gate control. Switching losses reduction is in this case a consequence of keeping v_{ds} rise and fall time as small as possible.

The only parameter without a significant improvement is the turn-on delay, where the results of both methods are comparable. The reason for the advanced control method to be inefficient in this case is presumably the fact that the low reference current i_{r2} must first charge parasitic capacitances formed by connections on the test PCB and bond pads**.** This delays the establishment of adequate conditions in current mirrors in interval T_2 for proper mirroring (in which only $M{\cdot}i_{r2}$ is supposed to form $i_{g,on}$). This causes that the current $i_{g,on}$ to equal zero for a period of time, resulting in i_d current rise delay. The described effect is also evident in Figure 13. Just after $M{\cdot}i_{r1}+M{\cdot}i_{r2}$ are active, there is a period of v_{gs} stagnation, which is a consequence of zero $i_{g,on}$. It is considered that the full integration of the amplitude manager (by using a different method for reference current setting instead of external R_{ref1} to R_{ref6} resistors) would eliminate the described problem.

6 Conclusion

The presented advanced gate control method efficiently reduces switching losses, as well as enables the minimization of the turn-off delay and final charging and discharging durations. This conclusion is obtained by comparing the advanced gate control with the conventional method. For illustration, in case of setting MOSFET drain current rise and fall times to 250 ns, the switching losses reduction is approximately 50% for turn-on and turn-off. Furthermore, the delays are reduced for 15% (turn-on) and 240% (turn-off), the turn-off final gate discharging duration is reduced for 50% while the turn-on final gate charging is as much as 10 times shorter. The system effectiveness increases with the current or voltage slope mitigation rate. The novel gate driving approach is thus proven effective.

The described method is applicable in a broad spectrum of applications, since it requires only to monitor the drain-source and gate-source voltages of the controlled MOSFET. The applications which would most significantly benefit from using the presented system are those where the switching losses dominate in the overall system losses, i.e. the applications with high switching frequency and/or high voltage and current ratings.

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