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Design and Characterization of a 130 nm CMOS Ultra-Wideband Low-Noise Amplifier

Aleksandar Pajkanović[1,2], Mirjana Videnović-Misić[2], Goran M. Stojanović[2]

[1]Faculty of Electrical Engineering, University of Banja Luka, Bosnia and Herzegovina
[2]Faculty of Technical Sciences, University of Novi Sad, Serbia

Abstract: The design of an ultra-wideband low noise amplifier is presented in this paper. Schematic level design is described, as well as integrated circuit layout techniques applied and post-layout simulation results. After fabrication using the standard 130 nm CMOS process node, on-chip characterization has been performed. The simulation and characterization results are presented analyzed and discussed in detail.

Keywords: CMOS integrated circuits (IC); analog/radio-frequency (RF); ultra-wideband (UWB); low-noise amplifier (LNA); on-chip characterization

Načrtovanje in karakterizacija 130 nm CMOS širokopasovnega ojačevalnika z nizkim šumom

Izvleček: Članek obravnava ultra širokopasoven ojačevalnik z nizkim šumom. Predstavljena je shema, uporabljene tehnike integracijskega vezja in rezultati simulacij. Po izdelavi v standardni 130 nm CMOS tehnologiji je bila opravljena karakterizacija na nivoju čipa. Predstavljeni so simulacijski in karakterizacijski rezultati.

Ključne besede: CMOS integrirana vezja; analogna radio frekvenca (RF); ultra široki pas (UWB); ojačevalnik z nizkim šumom (LNA); karakterizacija na čipu

** Corresponding Author's e-mail: aleksandar.pajkanovic@etf.unibl.org*

1 Introduction

Different applications employing ultra-wideband (UWB) systems are under investigation in the lower frequency range of radio-frequencies (RF), which is around 1-10 GHz [1]. Such applications of interest include high resolution radars [2], medical imaging [3], communication systems [4] and many more. Physical layer in common for all these implementations employs UWB signals which are characterized with high relative bandwidths, wider than in any other standard commercialized until now [5]. This possesses plenty of new challenges for the RF integrated circuit (IC) designers in an already complex engineering environment [6, 7].

UWB signal is defined in [1] as either a signal of absolute bandwidth (B) larger than 500 MHz, or a signal of relative bandwidth larger than 20 %, where relative bandwidth (B_r) is calculated as follows:

$$B_r = \frac{f_u - f_d}{f_c} \quad (1)$$

where f_u, f_d and f_c represent upper and lower band limit, and a central frequency, respectively. Documents defining frequency ranges, emissions and other UWB regulations were released in the United States first in 2002 [8] and in EU, Japan, Korea, Singapore and China since. UWB technology may, thus, utilize a frequency range of up to of 3.1-10.6 GHz. The whole range of 7.5 GHz is used only in the USA. In EU, the UWB band is divided in two sub-bands: lower (3.168-4.752 GHz) and higher (6.336-8.976 GHz). In Japan the sub-bands are given as: lower (3.696-4.752 GHz) and higher (7.392-10.032 GHz), while Korea and China have their own specifications. Other important UWB technology regulations

include its applications' definitions, such as indoor, outdoor, portable, fixed installed; data speeds of up to 480 Mb/s; and maximum emission levels, i.e. power spectral density (PSD) measured in terms of equivalent isotropically radiated power (EIRP). Moreover, in some of the mentioned sub-bands, e.g. lower EU sub-band, interference mitigation techniques are obligatory. As a consequence of such stringent regulations, total emitted power allowed is very low, and equal to -41.3 dBm/MHz. In the case of the full allowed specter (3.1-10.6 GHz), this means that the total transmitted power may not be greater than 0.56 mW. Therefore, commercial UWB transmission is limited to short range applications [1, 5].

To exploit these frequency ranges, there are two approaches to the design of UWB communication systems: impulse radio (IR), which is shown in Figure1a, and orthogonal frequency division multiplexing (OFDM), which is shown in Figure 1b. In the former case, the transmission is based on ultra-short pulses, thus covering the whole available band or sub-band. In the latter case, the available UWB bandwidth is divided into a set of wideband OFDM channels [1]. IR-UWB technique is more appropriate for applications where simple modulation schemes, such as on-off keying, provide enough signal integrity and offer higher energy efficiency and lower cost [9].

Regardless of the system architecture, the front-end wideband low noise amplifier (LNA) is obligatory as the first stage of the receiver [5], Fugure 1. Such amplifier must meet several stringent requirements, e.g. broadband input matching, sufficient gain with wide bandwidth, low noise figure, etc. [5, 10]. For the past decade CMOS represents standard technology in the RF IC domain [11, 12, 13].

For the design presented in this paper, a standard eight-metal layer, 130 nm CMOS technology node was chosen. A variety of MOS devices are available, including low- and high-threshold versions, devices operating at higher supply voltages (3.3 V) and devices intended for RF application. For circuit implementation presented within this paper RF MOS transistors are chosen, their nominal supply voltage (VDD) and transition frequency (ft) being 1.2 V and 105 GHz, respectively. In general, the transistors are capable for appropriate performance at frequencies up to 10 % of ft [14]. This means that UWB applications are feasible utilizing the MOS devices available within the selected process node. Additional advantage of this particular process node, in the context of RF IC design, is the availability of standard inductors. These are implemented in metal layer 8 and are all of spiral topology, either circular or rectangular, their inductance ranging from 100 pH up to 10 nH.

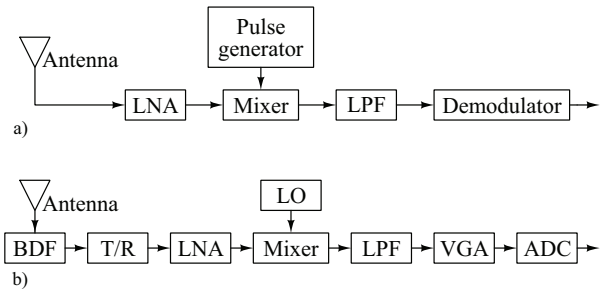

Figure 1: Two UWB communication system architectures [5]: *a)* IR and *b)* OFDM

In section 2 we provide a short introduction on figures of merit utilized within this paper for the LNA performance characterization. Then, in section 3 a brief overview of the related work is given. In the sections that follow, we present an LNA designed to operate in the EU UWB upper sub-band (69 GHz). The schematic level design procedure is described in section 4. The characterization procedure and the results obtained are presented in section 5. In section 6 the results characterized and simulated are analyzed and discussed, whereas in section 7 a conclusion follows.

2 Figures of Merit

In order to specify design requirements of an UWB amplifier, one is to use similar notions to those used when specifying a narrowband amplifier [14], such as gain, noise figure and input matching. However, the main difference is that these features must be achieved over a bandwidth of up to 10 GHz [1]. For example, according to Bode-Fano criterion [15], it is not possible to achieve arbitrary low reflection coefficient Γ(ω) in the arbitrary wide bandwidth, if there is a reactive component in the load. That is the reason why wideband amplifiers must show higher reflection coefficient than their narrow band counterparts with the same transistor dimensions. This means that the information on any of those specifications in the context of RF IC is complete only if given over a range of frequencies. Furthermore, since these frequencies in the case of UWB applications extend well into microwave spectrum, we employ some figures of merit used in microwave engineering [11, 16] to precisely specify and, later on, characterize the LNA performance. Of course, different parameter values represent a standard in UWB case [17].

2.1 Scattering parameters

For a high frequency and broad bandwidth characterization of a two port network a two-by-two scattering (S) parameters matrix is used [11, 16]:

$$S = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix}. \quad (2)$$

Each of the matrix members in equation (2) has physical meaning:
S_{11} – input reflection coefficient,
S_{12} – reverse transmission,
S_{21} – a sort of gain [16], as it relates output wave to input wave,
S_{22} – output reflection coefficient.

Normally, in the case of a LNA, the reflection coefficients and the reverse transmission coefficient should be as low as possible, whereas the gain should be as high as possible.

2.2 Noise factor

Three main sources of electrical devices noise are thermal, Schottky and flicker noise [16]. As opposed to the well known signal-to-noise ratio, *S/N* in the domain of RF IC design a parameter mostly used to present the information on internal noise are the noise factor, *F*, and the noise figure, *NF*. Noise factor represents the ratio of signal-to-noise ratio at the input and signal-to-noise ratio at the output:

$$F = \frac{(S/N)_{input}}{(S/N)_{output}}. \quad (3)$$

Noise figure is a dB representation of noise factor, obtained as follows:

$$NF = 10 \log F. \quad (4)$$

2.3 Linearity

Two parameters are used to characterize an amplifier in the aspect of linearity: 1-dB compression point, P_{1dB}, and input-referred third-order intermodulation (IM) intercept point, *IIP3*. The former represents the upper limit of the input signal power for which the LNA provides the expected output. This limit is defined as the input signal power which causes the real output to be less than expected output by exactly 1 dB [11, 16].

The latter figure of merit, *IIP3*, is required to take into account the influence of IM products; namely, the existence of two signals of frequencies close to each other at the input, gives rise to IM products. Second-order IM products can be easily filtered out, but third-order products can rise at frequencies within the information signal bandwidth and, thus, cause linearity issues [11].

The number associated with *IIP3* is obtained by bringing two signals of close frequencies and of equal amplitudes to the circuit input. Then, both output signal power and output third-order IM product power are plotted versus input power signal. Extrapolation of those two curves yields an intercept point. The P_{in} at which the extrapolated intercept point appears is actually the *IIP3*.

These two figures of merit are related as follows [11]:

$$IIP3 - P_{1\mathrm{dB}} = 9.6\,\mathrm{dB}, \quad (5)$$

under the condition that all nonlinearities of the order higher than 3 can be neglected.

2.4 Stability

Another working mode which amplification circuit may not enter during normal operation is oscillation. A figure of merit that needs attention in this context is circuit stability. It is possible to maintain the circuit stability at arbitrary input signal magnitudes (unconditional stability). There are multiple parameters defined as stability factors, but those used within this paper are the μ and μ′ factor. The former represents the distance from the Smith chart center point to the area where instability occurs caused by the load. It is calculated as follows [15]:

$$\mu = \frac{1 - |S_{11}|^2}{|S_{22} - \Delta S_{11}^*| + |S_{12} S_{21}|}, \quad (6)$$

where:

$$\Delta = S_{11} S_{22} - S_{12} S_{21}. \quad (7)$$

The latter is the distance from the center point to the area where instability occurs caused by the source. It is obtained in similar fashion:

$$\mu' = \frac{1 - |S_{22}|^2}{|S_{11} - \Delta S_{22}^*| + |S_{12} S_{21}|}. \quad (8)$$

A two-port network is unconditionally stable if μ >1 and μ′ >1.

3 Related Work

Achieving broadband gain is a fundamental requirement in an UWB receiver, which means that this is also necessary for any LNA – as it is the first stage of a receiv-

er in any of the cases mentioned in section 1. Depending on the system architecture, the approximate band covered by the LNA in most cases is either of the three frequency ranges: (*i*) from 3.1 to 5 GHz (low band), (*ii*) 6 to 10.6 GHz (high band) or (*iii*) 3.1 to 10.6 GHz (full band).

LNAs present in literature can also be classified according to the circuit topology applied to meet the requirements for each of the figures presented in section 2. Those can be broadly categorized into four types, as follows [18]:

- distributed amplifier,
- input reactive networks,
- resistive-feedback, and
- common-gate circuits.

These possible implementations are shown in Figure 2 at the highest level of abstraction.

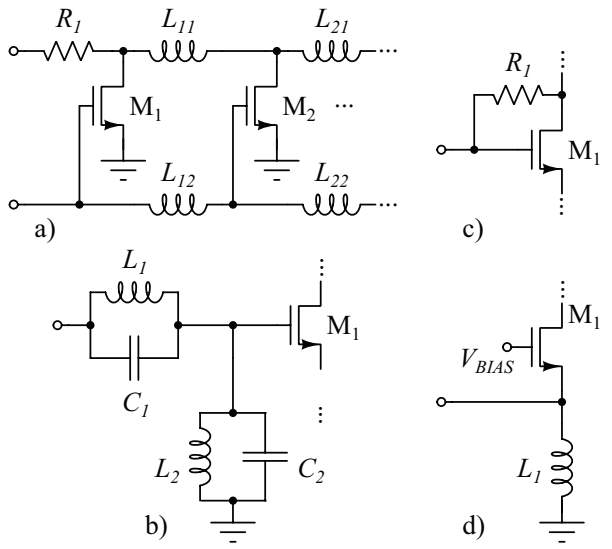

Figure 2: The standard wide bandwidth input matching techniques: *a)* distributed amplifiers, *b)* input reactive network, *c)* resistive-feedback and *d)* common-gate circuit

Distributed amplifiers, 0a, provide wide bandwidth characteristics, but tend to consume large DC currents due to the distribution of multiple amplifying stages which makes them unsuitable for low-power applications. Besides, such implementations contain a number of on-chip inductivities, so the whole circuit demands a larger area. In 0b, a topology which adopts a bandpass LC filter at the input of the LNA for wideband input matching is shown. The bandpass-filter-based topology incorporates the input impedance of the amplifier as a part of the filter, and shows good performances while dissipating small amounts of DC power. However, the inclusion of LC filter at the input demands a number of reactive elements, which introduce additional noise and increase the chip area needed. In 0c and 0d, resistive-feedback and common-gate topologies principles are shown, respectively. The resistive feedback based amplifiers provide good wideband matching and flat gain, but the noise figure deteriorates due to additional resistive element and power dissipation increases. The common-gate input characteristic depends on the transistors geometry and the inductance in the source circuit. These parameters can be set in such a way that the circuit provides wideband input matching [18].

In [18] an LNA is designed applying the RC feedback topology, employing a gain enhancement technique and containing only one inductor. A frequency selective broadband LNA is presented in [19], where a topology of either a global or local feedback or the combination of both is investigated. In [20] a two-stage common-source (CS) LNA that utilizes forward-body-bias (FBB) technique in n-type MOS devices is presented. The authors in [21] also employed the FBB technique along with the current-reuse scheme and active shunt-feedback towards their goal of ultra-low power consumption. In [22] an UWB LNA with operating frequency range from 50 MHz to 10 GHz with resistive feedback and π-matching network is presented.

From the papers mentioned in the previous paragraph and keeping in mind the dates of those publications (2014-2017), we can conclude that UWB is an active research area interesting from the design of RF IC point of view. Designers [18-22] are utilizing different technologies, topologies, techniques and approaches while trying to optimize performance over a large number of, often opposing each other, requirements. Those requirements differ from case to case, thus no general way of comparing LNA performance is possible. Therefore, no figure of merit can be used on its own, rather the whole design must be considered within the context of specific application.

4 Low Noise Amplifier Design

In the following subsections, we present a UWB LNA, designed using the Cadence Design Systems® toolchain and fabricated using the standard 130 nm CMOS process. First the topology choice is presented, where each stage is thoroughly discussed. Then physical design details are presented, describing the circuit layout. Finally, simulation results after parasitic extraction (postlayout simulation) are presented.

4.1 Topology Considerations

UWB circuits and systems must deal with numerous trade-offs [11]. For example, to design a highly linear

amplifier, large values of transistor overdrive voltages (V_{OD}=$V_{GS}V_T$) are required; which causes the increase in drain currents and, consequently, in power consumption. This means that high linearity and low power consumption are opposed design goals. Analogous to this conclusion, when other LNA design goals mentioned in sections 1 and 2 are considered, similar facts can be derived; i.e. it is a matter of trade-off between figures of merit how well the circuit will perform overall.

In that context, the most interesting topologies out of those discussed in section 3 are resistive-feedback (Figure 2c) and common-gate (Figure 2d). Both of them satisfy input matching across a wide frequency range, and offer a compromise between the numerous demands. For high gain conditions, the noise and gain performance of a resistive-feedback and of a common-gate is virtually the same. A key difference arises at high frequencies, where the load capacitance C_L has a very significant impact on the input impedance in the case of the resistive-feedback amplifier, while this is not so in the common-gate case [5]. Derivations thoroughly presented and discussed in literature [17], show that the source impedance of a common-source topology yielding minimum noise factor must be inductive in nature. As the input impedance of a MOSFET in such configuration is capacitive, providing a good match to a 50 Ω source is a difficult task. Nevertheless, for an LNA, presenting a resistive impedance of this value to the external circuits and sub-circuits is a critical requirement – therefore, the LNA topology and the elements it comprises of, must be selected accordingly. The simplest approach would be to connect a 50 Ω resistor between the gate and source terminals of a common-source connected MOSFET. However, the resistor adds thermal noise of its own and, as it creates a voltage divider, it attenuates the signal by a factor of two. It turns out, as it is further explained in subsection 4.2, that a common-gate topology realizes resistive input impedance, as shown in equation (9).

However, common-gate amplifier topology cannot typically be used directly in UWB front-ends, as a consequence of its inadequate noise performance over the frequency range of interest, as well as potential failure to meet gain-bandwidth product requirement. This single-transistor topology thus needs to be enhanced to achieve the desired noise, gain and bandwidth specifications [5]. For this reason, the second stage consisting of a common-source amplifier employing the shunt-peaking technique [16] is cascaded to the first stage.

The proposed solution schematic is shown in Figure 3. This LNA circuit can be divided in three sub-circuits: common-gate (first stage), bandpass filter and common-source (second stage). All transistors operate in the strong inversion region.

Two circuit nodes directly controlling transistor biasing are accessible from outside through the pads, thus making the LNA operating region adaptable even after fabrication. These connections are omitted from Figure 3 for simplicity, but allow fine tuning of M_1 and M_2 operating points through V_{B1} and V_{B2} values setup. This is done with the idea to enable compensation of the potential process variations.

Finally, substrate of each transistor is grounded with a high resistivity resistor (body floating). In this way substrate current noise referred to drain node is reduced, resulting in overall *NF* reduction of about 0.5 dB [17].

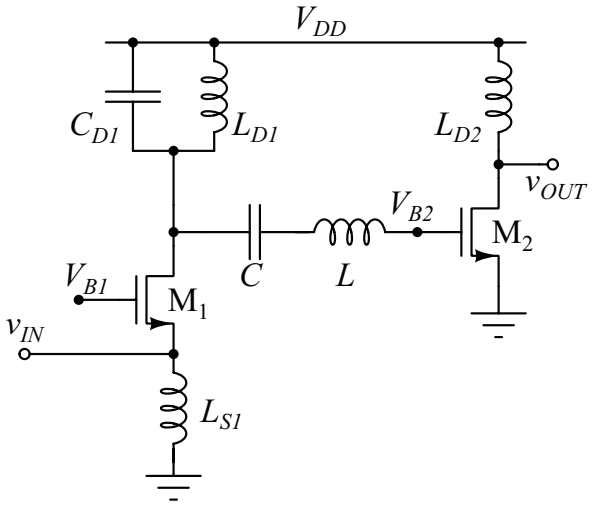

Figure 3: Proposed circuit (biasing, substrate contacts, pads and body floating resistors omitted)

4.2 Common-gate Stage

The first stage consists of a transistor M_1 in a common-gate configuration with a coil L_{S1} in the source and an *RLC* resonant circuit in the drain. In its first approximation, its input impedance is:

$$Z_{in} \approx \frac{1}{g_m}, \tag{9}$$

where g_m is transistor's transconductance. This relation is quite straightforward and, thus, M_1, along with inductor L_{S1}, is used to set input impedance towards the goal of 50 Ω, i.e. input return loss (S_{11}) below -10 dB. The source input matching is needed in order to avoid signal reflections at the input of the LNA or the alterations of the characteristics of the RF filter preceding the LNA, such as pass-band ripple and stop-band attenuation [7].

Voltage gain of the common-gate stage is given as [1]:

$$\frac{V_{out}}{V_{in}} = \frac{g_m r_{out} + 1}{2\left(1 + \frac{r_{out}}{R_{D1}}\right)}, \tag{10}$$

where r_{out} represents the M_1 output resistance and R_{D1} is the resistance in the drain of M_1. The resistor R_{D1} is not shown in Figure 3, as it is actually composed of resistive parasitics contained in L_{D1}, C_{D1} and interconnects.

This common-gate configuration also acts as a tuned amplifier; namely, the resonant circuit consisting of L_{D1}, C_{D1} and R_{D1} enables this subcircuit to amplify the signal within the band around the resonant frequency. The resonant circuit is not decoupled from the rest of the amplifier, so in all considerations other elements also must be included. Concretely, it is influenced by the M_1 parasitic output impedance and the bandpass filter input impedance. Including the additional parasitics, the resonant circuit is tuned to 5.8 GHz.

For a MOSFET transistor operating in saturation, the most dominant noise source is channel thermal noise. Power spectral density of a saturated MOSFET is calculated in the following way [16]:

$$\overline{i_{nd}^2} = 4 \cdot kT \cdot \gamma \cdot g_{d0} \cdot \Delta f \tag{11}$$

is assumed the dominant source of noise, where g_{d0} is the drain-source conductance at zero V_{DS} and γ is the correction factor named excess-noise factor. For a submicron MOSFET, we assume: $g_{d0}/g_m > 1$ and γ = 2/3 for a long-channel saturated transistor in strong inversion. Value of γ can be larger, γ > 1, in the case of a short-channel transistor, as it strongly depends on the channel length modulation effect [16]. The noise factor of a common-gate device at low frequencies, when the input impedance is matched to the source, is given by:

$$F = 1 + \gamma + 4\frac{R_S}{R_L}. \tag{12}$$

which, indirectly, yields *NF*, also. Thus, as the gain is increased by increasing the value of R_L, the noise factor similarly asymptotically assumes a value of 1+γ. This result also assumes that the common-gate amplifier uses an RF choke, which in this case is L_{S1}. The inductor is necessary, as the usage of a resistor or a current source instead would increase the noise factor [15, 16]. Therefore, the main purpose of L_{S1} is the reduction of noise factor. To achieve this, its value must be carefully selected. This is done first by preliminary calculations, based on the fact that this inductor, to enable noise figure reduction, must resonate with the total capacitance in its proximity, which includes: capacitance of the input signal pad (C_{pad}), the parasitic of the transistor M_1 (C_{SB1} and C_{GS1}) and its own parasitic capacitance (C_{LS1}). A first order approximation yields:

$$L_{S1} = \frac{2 \cdot \pi \cdot f_{res}}{C_{pad} + C_{SB1} + C_{GS1} + C_{LS1}} \tag{13}$$

where f_{res} is the frequency at which the resonance occurs, in this case being equal to the frequency the *RLC* circuit in the drain of M_1 is tuned to (5.8 GHz). As these capacitive parasitics cannot be known a priori, the calculation according to equation (13) is only the first step; namely, the final value of L_{S1} is yielded through simulations in several iterations.

4.3 Common-source Stage

The cascaded second stage is a common-source circuit consisting of the transistor M_2 loaded by the coil L_{D2}. Just as in the previous stage, a resonant circuit was used to set the working frequency range, in this stage it is done by a single coil in the drain circuit. This approach is known as shunt-peaking technique [16]. At higher frequencies, as the impedance of the inductance increases, that of the load capacitance decreases. By properly controlling the relative value of the load inductance in relation to the parasitic capacitance, a flat gain can be achieved over a wider bandwidth. In fact, a bandwidth extension of as much as 70% can be achieved by use of a single inductor, in comparison to a simple shunt RC load. In the case of wideband amplifiers, the inductor does not require a high-quality factor, since the bandwidth is supposed to be the widest possible.

Besides its influence on the gain characteristic, L_{D2} directly determines the output return loss, S_{22}.

4.4 Bandpass filter

Impedance matching between the amplifying stages is achieved employing the bandpass filter composed of an inductor *L* and a capacitor *C*. The capacitance *C* is also used to decouple the first and the second stage, thus enabling the M_2 transistor biasing. Keeping in mind this other purpose of the capacitive element and including the influence of the rest of the circuit, the bandpass filter is tuned to 9.5 GHz.

4.5 Layout

In Figure 4 circuit's floorplan is presented. Elements occupying the largest area are four inductors, twelve

pads and a large decoupling capacitor formed as a vertically interdigitated structure encircling the LNA core, formed in metal layers 1 and 8.

During schematic level design, pad influence on LNA performance (especially on Γ(ω)) was taken into account (even though omitted from Figure 3). Groups of three pads on the left and right represent input and output ports in the constellation ground-signal-ground (GSG), where the middle pad is input and output, respectively. Top and bottom pad groups are in power-ground-logic form, where "logic" contacts are used as the inputs for transistor biasing control. Both power supply and ground connections are present on two sides (top and bottom) of the design in order to secure equal voltage levels of V_{DD} over the whole die.

The transistors M_1 and M_2 are each implemented as multiple transistors in parallel. Thus, more fingers are available to reduce effective gate resistance [17, 23].

Contrary to analog circuits where components and interconnects can be placed in the vicinity of each other, in the case of RF circuits that is not always possible. To ensure inductor operation without crosstalk, they must be safely distanced from other circuit components. The same consideration is applied to interconnects, as their behavior significantly changes at high frequencies (HF). For this reason plenty of empty space can be seen in Figure 4. However, that may not be fabricated as such, because metal density limitations are present in every CMOS technology node [24]. Therefore, these areas are filled with metal islands in order to satisfy the demand for metal density while degrading circuit performance as minimum as possible.

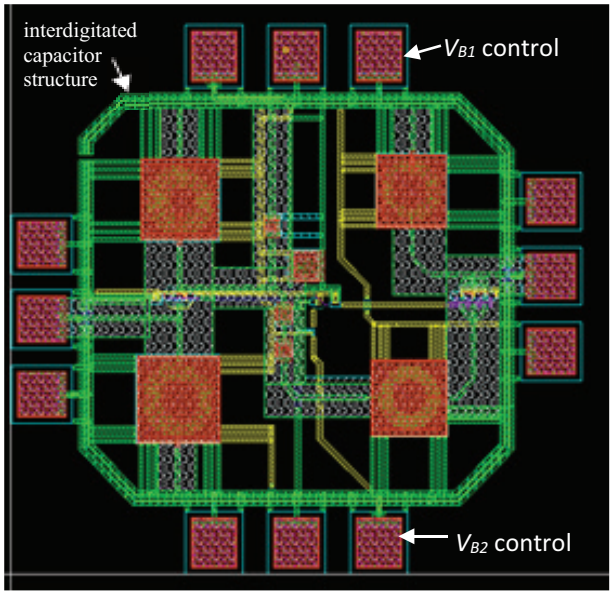

Figure 4: LNA layout screenshot as designed

The circuit occupies silicon area of 0.89 mm^2, whereas the LNA core (LNA design without the pads and the interdigitated capacitor) occupies the area of 0.66 mm^2.

4.6 Post-layout Simulation Results

After the parasitic extraction and prior to fabrication, final scattering parameters and noise figure results are shown in Figure 5. For this nominal case, M_1 biasing is set at V_{B1}=570 mV and M_2 biasing is done through a current mirror – the reference branch of which is biased at V_{B2}=1.2 V. The maximum gain, S_{21}, is 15.48 dB, whereas the 3 dB frequencies are at 6.31 and 9.07 GHz. Input matching, measured by S_{11}, is better than -10 dB over the whole range. Output reflection coefficient is somewhat higher than -10 dB. However, such values for S_{22} are acceptable [17].

Minimum value of *NF* within the frequency range of interest is 3.8 dB at 7.10 GHz.

Power consumption is 18.41 mW from the supply voltage of 1.2 V.

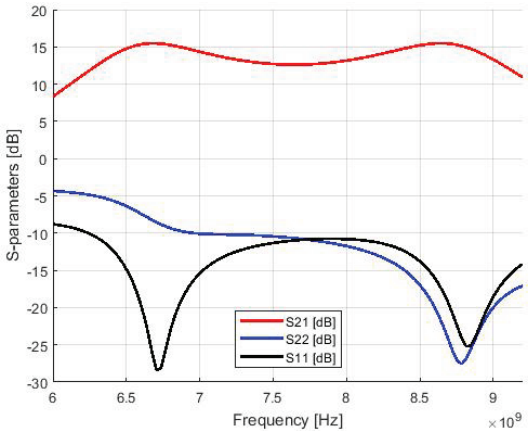

Figure 5: Post-layout scattering parameter simulation results

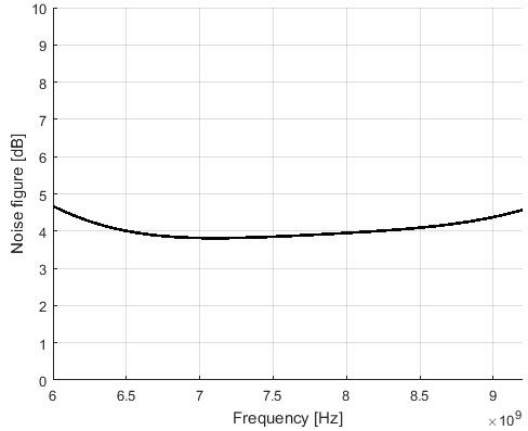

Figure 6: Post-layout noise figure simulation results

Linearity figures of merit of the designed LNA are summarized in 0, as defined in section 0. *IIP3* is simulated in two cases, hence the designations @ 50 MHz and @ 200 MHz. In the former case, the second signal is a 50 MHz offset relative to the main signal, whereas in the latter case the second signal is a 200 MHz offset relative to the main signal.

Table 1: Linearity figures of merit simulation results

f [GHz]	6.4	7	7.6	8.2	8.8
IIP3 @ 50 MHz [dBm]	0.38	1.33	3.18	2.38	0.95
IIP3 @ 200 MHz [dBm]	0.92	1.27	3.25	2.59	1.00
P1dB [dBm]	- 8.68	- 8.33	- 6.35	- 7.01	- 8.60

5 Characterization

The on-chip characterization set-up is shown in Figure 7, consisting of VNA (N5240A from Keysight Technologies ®), RF probe station, RF cables, two GSG probes and two DC PGL probes (all from Cascade Microtech ®). First the influence of the equipment is canceled through VNA calibration process – short, open, load and thru (SOLT) procedure in this case – and then the characterization is performed.

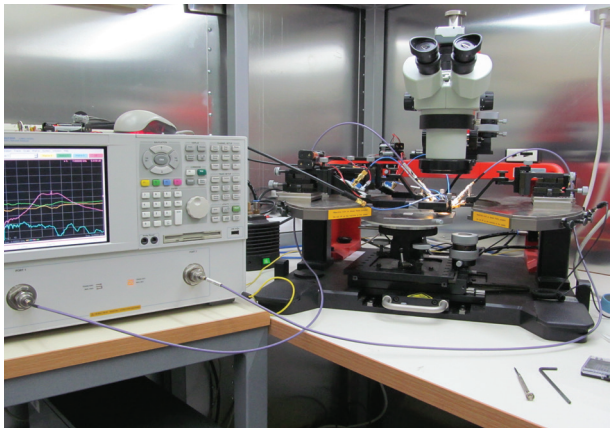

Figure 7: Measurement set-up

In Figure 8 fabricated circuit microphotograph is shown, while probe contact with pads is secured. Contrary to Figure 4, in this image metal filings are obvious.

In Figure 9-11 characterization results are shown at nominal biasing as given in subsection 4.6, witnessing scattering parameters behavior close to simulated values. A frequency shift of less than 10 % is present in all characteristics. Maximum gain is 12.33 dB, whereas the 3 dB band ranges from 5.74 GHz to 8.14 GHz, as shown in Figure 9. Input matching raises above -10 dB at mid-

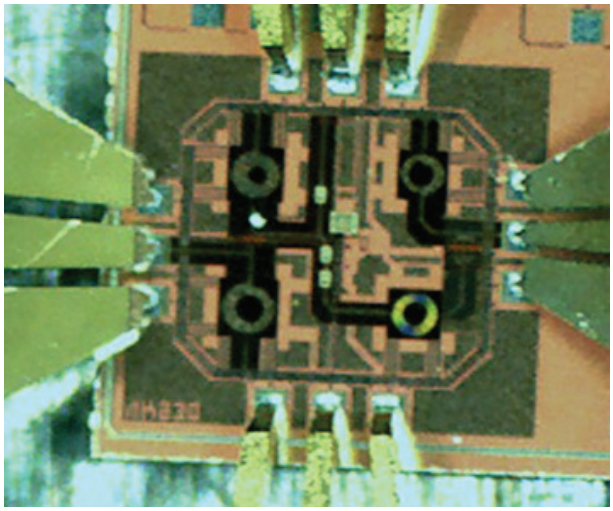

Figure 8: Die microphotograph

dle frequencies (around 7.54 GHz) but remains below for the rest of the 3 dB range, which is shown in Figure 10. Output reflection coefficient also deteriorates compared to post-layout simulation results shown in Figure 5, but within acceptable limits, as it is shown in Figure 11.

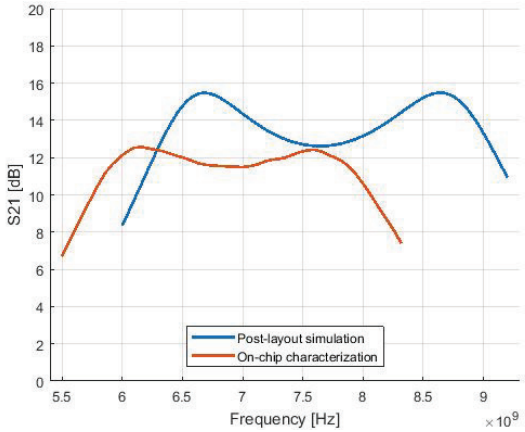

Figure 9: S_{21} characterization results (red) compared against the post-layout simulation results (blue)

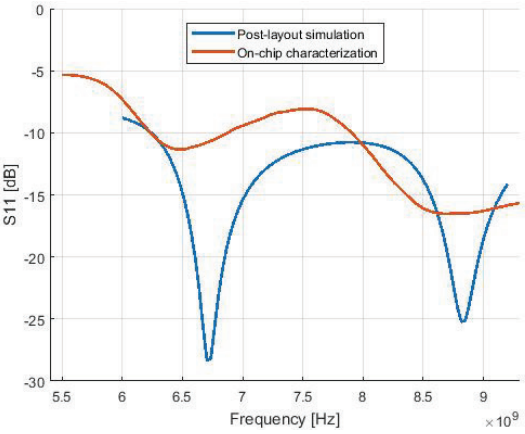

Figure 10: S_{11} characterization results (red) compared against the post-layout simulation results (blue)

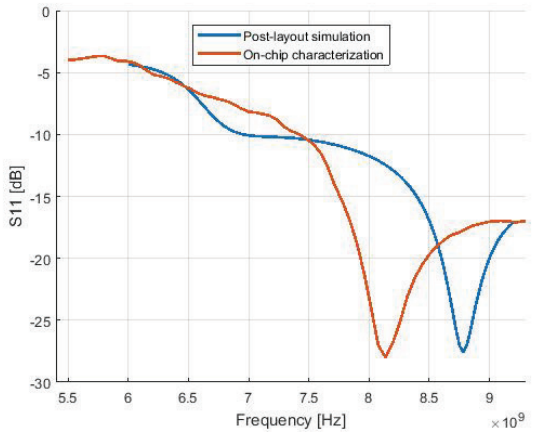

Figure 11: S_{22} characterization results (red) compared against the post-layout simulation results (blue)

In Figure 12 linearity characterization results are presented, showing a P_{1dB} point at -4.5 dBm of input power.

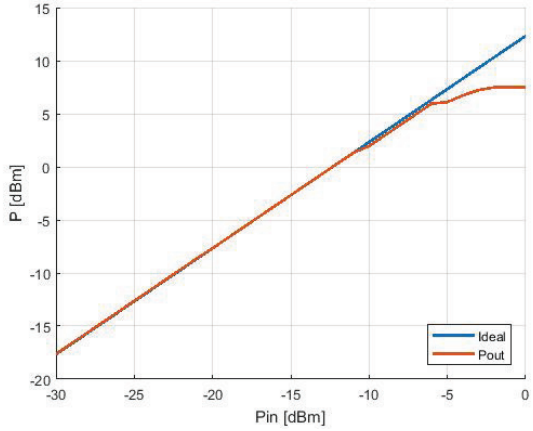

Figure 12: 1-dB compression point (P_{1db}) characterization results

6 Discussion

Characterization results deviate from the postlayout simulation as the frequency shift of 10 % is noticed in Figure 9 when compared to Figure 5. Therefore, 3 dB bandwidth of this circuit is from 5.74 to 8.14 GHz. Furthermore, LNA gain is deteriorated by 3 dB, as the maximum in postlayout is 15.48 dB, whereas the characterization yielded a maximum value of S_{21} as 12.33 dB. This is the reason why P_{1dB} is somewhat improved (-4.5 dBm) compared to expected results (Table 1); namely, since the gain is smaller, the amplifier will operate in the linear region at higher input signal power. Measured S_{11} is above -10 dB for a segment of the 3 dB bandwidth, in the vicinity of 7.54 GHz. Finally, S_{22} also departs from the predicted curve, but it does remain less than -5 dB over the frequency range of interest.

Frequency shift to lower frequencies and decrease in S_{21} are both signs of increased resistive parasitic components within the circuit interconnects [24]. Current density within a conductor of a circular cross-section is given as [25]:

$$J(u) = J(0)\left\{\mathrm{Re}\left(J_0(u)\right) + \mathrm{jIm}\left(J_0(u)\right)\right\}, \quad (14)$$

Where $u = \sqrt{-\mathrm{j}}s$, $s = k'r$, $k' = \sqrt{\omega\mu\sigma}$, r distance to the conductor axis, $J(0)$ current density along the conductor axis and J_0 Bessel's function of order zero. At high frequencies, equation (14) can be approximated as follows:

$$J(x) = J_S e^{-\frac{x}{\delta}} \quad (15)$$

where J_S is current surface density, x distance to the conductor surface and δ penetration depth, given by:

$$\delta = \frac{1}{\sqrt{\pi\mu\sigma f}}, \quad (16)$$

where μ and σ represent permeability and conductivity, respectively.

Equation (14) is valid only for conductor of circular cross-section, whereas approximation (15) is also valid for conductors of rectangular cross-section. This effect is known as skin effect and it actually means that at low frequencies current flows through the whole cross-section uniformly; while, as the operating frequency rises, current flow is retreating towards the conductor surface. If the skin effect is dominant, current flows almost completely on the surface of the conductor. This further means that the cross-section of the part of the conductor used for current flow reduces as the frequency rises. Reduction of cross-section increases conductor surface resistance, which is directly proportional to $\sqrt{f}$ [25], which theoretically justifies the decrease in gain magnitude and its shift to the lower frequencies, visible in Figures 9-11.

In Figure 13 and Figure 14 the influence of transistor M_1 biasing to circuit operation is shown – S_{11} and S_{21}, respectively.

Two resonant pairs of frequencies can be seen in Figure 13. At values of 476, 526 and 576 mV for V_{B1}, one pair of resonant frequencies and at values of 810 mV, 1 and 1.2 V, another pair of resonant frequencies is noticed for S_{11}. The reason for such fundamental change in behavior is a consequence of different modes of operation of transistor M_1. For values of 476, 526 and

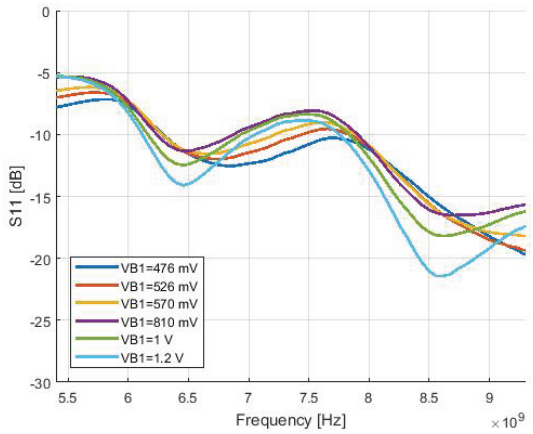

Figure 13: Transistor M_1 biasing influence to S_{11}

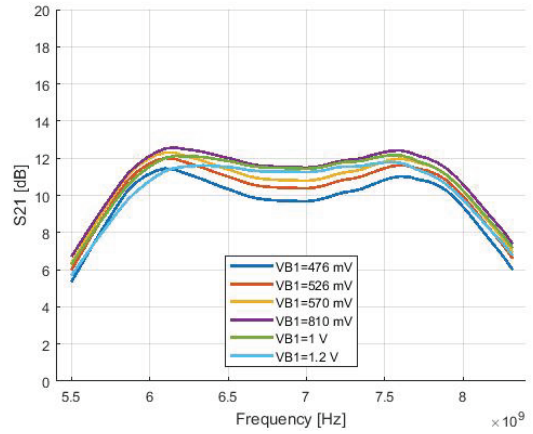

Figure 14: Transistor M_1 biasing influence to S_{21}

576 mV it operates in the weak inversion operation region and for values of 810 mV, 1 and 1.2 V it operates in the strong inversion. All parasitic capacitances (except for gate-substrate capacitance, denoted as C_{gb}) are zero, whereas they (gate-source and substrate source, for example, denoted as C_{gs} and C_{bs}) rise to significant values in the strong inversion saturation [26]. Thus, as gate-source voltage, V_{B1}, of M_1 raises and it passes intro strong inversion, the resonant frequencies shift to left. Even though S_{11} deteriorates above -10 dB at nominal value of V_{B1} (Figure 9), it Figure 13 it can be seen that V_{B1} may be used to eliminate this variation, e.g. by setting V_{B1}=476 mV. In Figure 14 it is seen that variation of S_{21} may not be remedied as easily, but characteristics that are easily influenced to the extent are 3 dB range and S_{21} variation over that range. During characterization, V_{B2} was also varied. However, its influence to S_{22} was negligible, as that parameter is primarily determined by L_{D2}.

In Table 2, a summary of the circuit performance presented in this paper is given, along with several other works cited. The purpose of this table in no way is a claim which of the circuits performance is better, since each of them was designed to optimize a different figure of merit; for example, in [21] the main goal was low power consumption, whereas in [22] the authors achieved very high linearity. Therefore, Table 2 is given here in order to point out that the characterization results obtained within this paper are of the same order like the results found in relevant and up-to-date literature.

Table 2: This work result summary and comparison to related work

	This work	[2]	[3]	[4]	[5]
technology [nm]	130	180	90	130	130
S_{21MAX} [dB]	12.33	10.15	15	14	13.28
3 dB range [GHz]	5.74-8.14	1.1-5	3.5-9.25	0.6-4.2	0.05-10
S_{11} [dB]	< -10	< -10	< -10	< -10	< -10
S_{22} [dB]	< -5	< -10	< -10	< -10	< -10
NF_{min} [dB]	3.8*	4.05*	2.4	4	3.29
P_{1dB} [dBm]	-4.5	-9.5	-17.25	-19.6**	3.6**
V_{DD} [V]	1.2	1.8	0.8	0.5	1.2
P_{DD} [mW]	18.41*	28.54	9.6	0.25	31.2
area [mm²]	0.66	0.35	0.56	0.39	0.77

* simulated

** estimated according to equation (5)

This work represents the continuation of research presented in [27]. In the next iteration of circuit redesign, electromagnetic (EM) properties [12, 24], such as skin effect, and PVT compensation techniques [28, 29] will be included.

7 Conclusion

Successful characterization of a fabricated UWB LNA using a standard 130 nm CMOS technology node is presented in this paper. The characterization results show that the techniques applied during the design phase of the circuit successfully fulfill its task: amplification over a wide frequency range with low noise factor. To prove this, a comparison with several state-of-the-art LNA designs found in literature is given in Table 2. The designed LNA provides 12.33 dB gain within the upper EU UWB band, its input reflection coefficient being less than -10 dB over the whole range. Minimum noise figure is shown to be 3.8 dB, while the circuit consumes 18.41 mW of power from a 1.2 V supply voltage. The amplifier remains linear for the input power levels up to -4.5 dBm and its area on chip is 0.66 mm².

The in-depth discussions of the design procedure, the figures of merit and, especially, characterization approach provide detailed insight in the steps performed to achieve the obtained results. The characterization results do deviate less than 10 % of the post-layout simulation results, as a consequence of the skin effect; namely, due to the fact that the current is flowing on the surface of the conductor, resistance of the signal line increases proportionally to the square root of the operating frequency. However, techniques to tackle these effects are recognized and will be implemented in future work.

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