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Synthesizable 2D Vernier TDC based on gated ring oscillators

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Abstract: Time to digital converter (TDC) is a device, which measures time interval between two edges of signals and converts it to digital code. Lately it is used as phase detector in all-digital frequency synthesizers. One of main parameters of TDC is resolution, which describes smallest time interval, which can be measured using TDC. Resolution of basic inverter-based TDC improves with reduction of delay of inverter in modern nanometric CMOS technology nodes. But in more mature technologies delay of inverter does not provide needed TDC resolution. In this paper sub-inverter-resolution 2D Vernier TDC, which is based on gated ring oscillators and is implemented in VHDL hardware description language for easy migration to various technology nodes, is presented. It is synthesized, placed and routed in 65 nm CMOS technology. Main blocks of TDC are two gated ring oscillators, their lap and edge counters, arbiter matrix, output decoder and control block. Frequency and single stage delay of gated ring oscillators is changed by switching parallel-connected sections of three-stage oscillators. Tuning step of single stage delay of gated ring oscillator, which is equal to the resolution of TDC, can be changed from 3.2 to 0.8 ps at typical operation conditions, when number of enabled stages of oscillator is changed from 22 to 48. TDC occupies 123,0 μm × 148,8 μm area of silicon.

Keywords: CMOS; integrated circuit; time to digital converter; Vernier; gated ring oscillator

Sestavljivi 2D Vernier TDC na osnovi obročnih oscilatorjev

Izvleček: Časovno digitalni pretvorniki (TDC) so naprave, ki merijo časovni interval med dvema roboma signal in ga pretvorijo v digitalno obliko. Pretvornik je uporabljen kot fazni detektor v digitalnih frekvenčnih sintetizatorjih. Glavni parameter TDC je resolucija, ki je opisana kot najmanjši časovni interval, ki ga še lahko izmeri. Resolucija osnovnih invertirajočih TDC se izboljša z znižanjem zakasnitev inverterja v moderni nanometrski CMOS tehnologiji. Pri zrelih tehnologijah zakasnitev ne omogoča doseganja željene resolucije TDC. V članku je predstavljen 2D Vernier TDC na osnovi obročnega oscilatorja s podinvertersko resolucijo. Zaradi lažje migracije v različne tehnologije je realiziran v VHDL strojnem jeziku. Sestavljen je v 65 nm CMOS tehnologiji. Glavni bloki TDC so: dva krožna oscilatorja na osnovi vrat, njihov krog, robni števci, arbitna matrika, izhodni dekoder in kontrolni blok. Frekvenčne in enostanjske zakasnitve se spreminjajo s preklapljanjem vzporedno vezanih sekcij tristanjskega oscilatorja. Korak je nastavljiv od 3.2 do 0.8 ps pri tipičnem delovanju in predstavlja resolucijo TDC. Velikost TDCja je 123,0 μm × 148,8 μm.

Ključne besede: CMOS; integrirana vezja; časovno digitalen pretvornik; Vernier; obročni oscilator

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1 Introduction

Time to digital converter (TDC) is electronic device which converts time interval between edges of two signals into digital code. It is often used as phase detector in all-digital phased locked loops, which are used as high frequency synthesizers. Such synthesizers are gaining popularity in recent years, since it becomes harder to implement conventional charge-pump synthesizers in modern nanometric integrated circuit (IC) technology nodes. Therefore, there is a lot of effort put into research and development of all-digital frequency synthesizers and their constituting blocks.

The output of TDC is digital, therefore due to quantization, which is related to resolution of TDC, it affects phase noise of whole synthesizer [1]. The most

basic TDC is based on inverter delay line. In such TDC signal generated by digitally controlled oscillator (DCO) propagates through delay line and its value after each inverter is sampled by the edge of reference signal. At the output, there is a pseudo thermometric code, which shows how many inverters are between edges of reference and generated signals. The minimal time interval, which can be measured by this TDC, is equal to inverter delay.

Therefore, performance of this TDC increases and its quantization decreases in newer technology nodes as the delay of inverters decreases. Although in more mature technology nodes performance of such TDC decreases and consequently there is a need for TDC which can measure time intervals lower than inverter's delay. There are several structures of TDC with sub-inverter delay resolution, such as multi-stage TDC, Vernier family of TDC's (1 dimensional (1D), 2 dimensional (2D), 2D Gated Ring Vernier), stochastic TDC etc. [2]–[7]. Although these structures can achieve high resolution, their complexity is much higher compared to TDC based on inverter delay line. Also, often TDCs are manually designed and routed despite of digital nature of TDC, what defeats one of the advantages of all-digital frequency synthesizers – easy migration from one IC technology to another.

The aim of this work is to design time to digital converter, which has sub-inverter delay resolution, large input time range and can be easily implemented in various IC technology nodes. Proposed TDC is implemented using VHDL hardware description language and is fully synthesized in 65 nm CMOS technology. It employs 2D Vernier properties and as in 2D Gated Vernier TDC [6], its delay lines are replaced with gated ring oscillators. Also, compared to [6] different phase detection technique and structure of oscillator and its tuning method is used to make design synthesisable. Output decoding procedure and its issues in 2D Vernier architecture are also addressed in this paper.

2 Structure of TDC

The structure of proposed time to digital converter is presented in Fig. 1. Two main inputs for reference and DCO signals are respectively marked as F_{REF} and F_{DCO} and output is marked as TD_{COUT}. Main blocks of TDC are lower frequency gated ring oscillator (GRO_L), higher frequency gated ring oscillator (GRO_H), lap counter of lower frequency oscillator, edge counter of higher frequency oscillator, matrix of arbiters, control block and output decoder.

2.1 Gated ring oscillators and counters

Lower and higher frequency gated ring oscillators share same structure, which is shown in Fig. 2. They are composed of N parallel-connected three-stage gated ring oscillators, made of tristate inverters, similar as in [8]. Such inverters are available in most IC manufacturing technologies. Therefore, usage of these inverters does not prevent synthesis of oscillators. The frequency of an oscillator can be tuned by turning on different numbers of parallel-connected sections of oscillator.

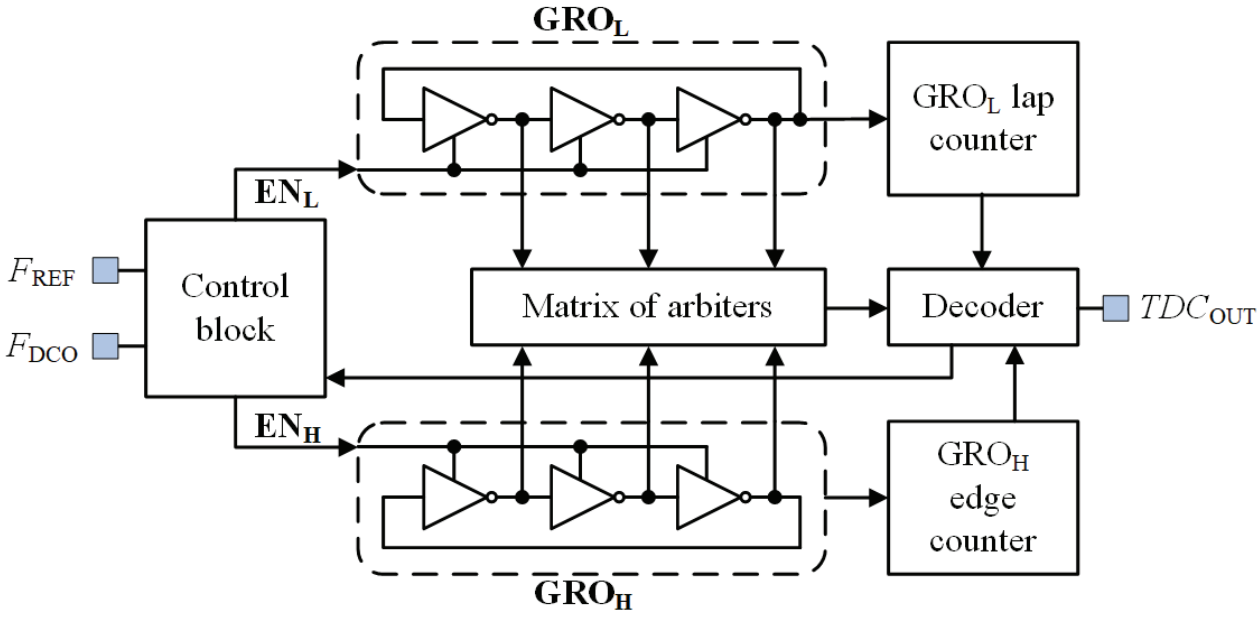

Figure 1: Structure of proposed time to digital converter

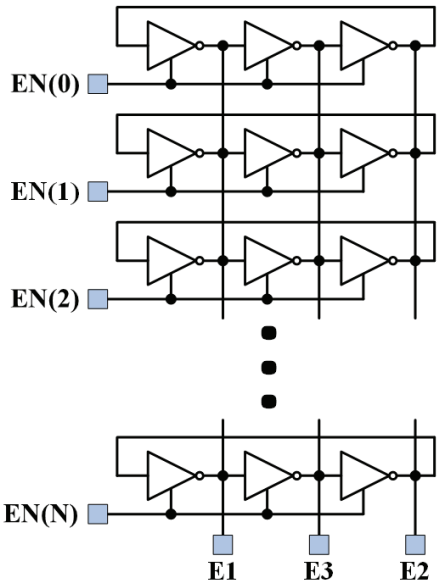

Figure 2: Structure of Gated Ring Oscillators

The output of oscillators is a periodic signal, but in this case oscillators are turned on only when the edge of the reference signal or the edge of the signal generated by the frequency synthesizer (i.e. DCO output signal) is received and oscillators are treated as infinite delay lines. To calculate the output of TDC we need to know through how many delay elements (oscillator's stages) signal has propagated. For this task lap counters are used to calculate through how many oscillator's laps the signal has travelled and edge counters to calculate signal's edges in one lap (i.e. through how many delay elements the signal has traveled in current lap). From values of both counters the total number of propagated delay elements may be calculated.

Only rising edges of gated ring oscillator's signals are used to calculate the time interval between edges of TDC input signals to avoid mismatch between edge rise and fall times [9]. Since oscillators are made of tristate inverters, edges used for calculation are distributed not in succession as shown in Fig. 2 (ports E1, E3, E2), because the signal is inverted after each stage. Therefore, one logical delay element is made of two tristate inverters and one logical lap is counted after two laps.

2.2 Arbiters

Often D type flip-flops are used as arbiters in time to digital converters – data input can be used as input for delayed versions of reference signals and clock inputs are used as input for delayed versions of generated signals. As it is known, for correct operation of D flip-flop, its data signal should be constant during setup and hold time near clock signal edge i.e. in metastability window (time interval $T_S + T_H$, shown in Fig. 3). Otherwise, if signal changes in metastability window, the output of the flip-flop can acquire any value (Fig. 3, (b)). Correct operation of flip-flop is essential in TDC application, because in locked state of the frequency synthesizer or when the edge of generated signal catches up with the edge of reference signal (in Vernier operation), edges of clock and data signals are very close to each other. One of the common method to address this issue is to use sense amplifier flip-flops, which have a narrow metastability window [1]. But unfortunately, these flip-flops are not suitable for synthesis.

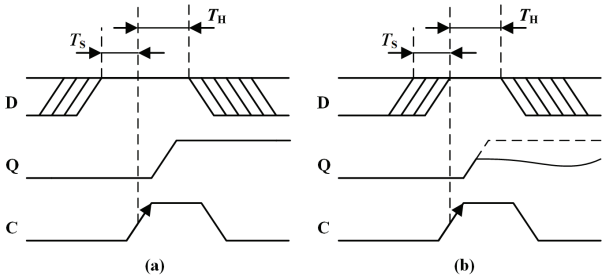

Figure 3: Operation of D type Flip-Flop: correct output (a) and possible metastability (b). T_S – setup time, T_H – hold time

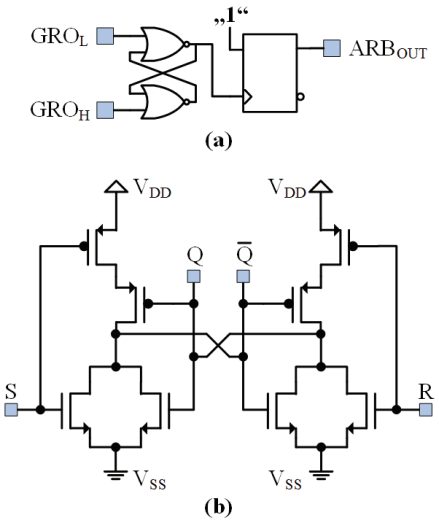

Figure 4: Arbiters made of SR latch and D flip-flop (a) and symmetrical structure of SR latch, composed from NOR gates (b)

Arbiters made of SR latch and D type flip-flop shown in Fig. 4, (a), can be used to narrow the metastability window [5], [9]. Latch is a level sensitive device, so even if edges of input signals are received close to each other, the output of the latch will settle to a known logic level. D type flip-flop is edge sensitive, so its metastability is eliminated by connecting data input to constant logical "1" level and the output of the SR latch is used as a clock signal. It should be noted, that the D flip-flop in such an arbiter should be reset before each

measurement, since it can't change its state to logic "0" after it was set to "1", because its data input is constant high. Also, SR latch made of NOR or NAND gates has symmetrical structure (Fig. 4, (b)), so it is equally loading both ring oscillators, although if it is implemented in hardware description language, designer is dependent on foundry-provided standard cells and usually cannot affect schematics and layout of individual gates.

3 Operation of TDC.

The control algorithm of proposed TDC is shown in Fig. 5. To simplify overall design of the TDC and lower used area of silicon, TDC is measuring only positive time intervals, i.e. when the edge of the reference signal is received earlier than the edge of the signal generated by digitally controlled oscillator. On the other hand, negative delays are equal to large positive delays (larger than half of the period of the reference signal).

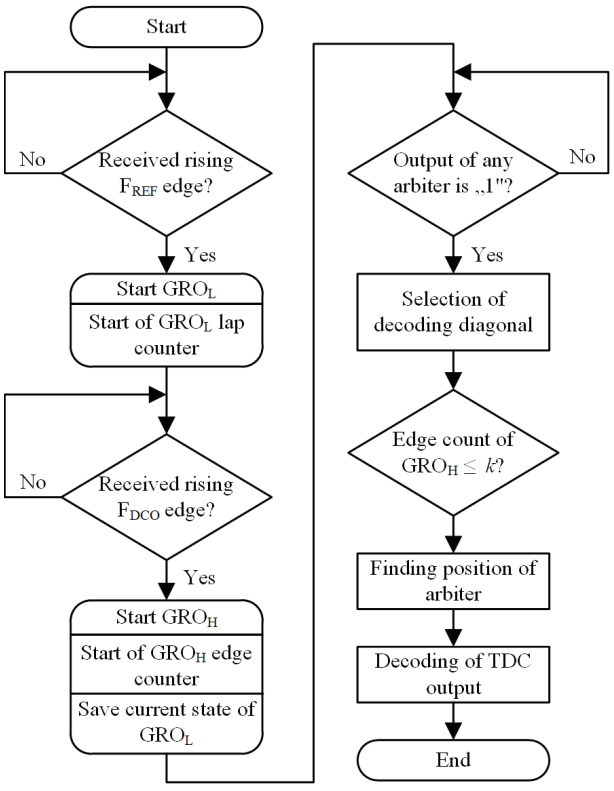

Figure 5: Control algorithm of proposed time to digital converter

At the beginning of the measurement TDC is waiting for the rising edge of the reference signal. When it is received, the lower frequency gated ring oscillator and its lap counter are started and the TDC's input for the reference signal is disabled. After that TDC is waiting for the rising edge of the signal generated by synthesizer's DCO. When it is received, the state of lower frequency oscillator (signal levels after each inverter) is saved, higher frequency oscillator and its edge counter are started and the TDC's input for the signal of DCO is disabled. When both oscillators are started, the output values of arbiters are monitored. When the output of any arbiter changes to high logic level, position of that arbiter is searched and depending on that position, the output signal of TDC is decoded. After that, all counters are reset, both inputs of TDC are enabled and TDC is waiting for another pair of the input signals for new measurement. Such operation allows to avoid usage of complex phase detector, introduced in [6].

Distinct case of 2D Vernier operation is obtained when the delays of stages composing two oscillators (or delay lines) are related with such dependency [5, 6]:

$$\Delta = \tau_{res} = \tau_1 - \tau_2; \quad \tau_1 = k \cdot \Delta; \quad \tau_2 = (k-1) \cdot \Delta \qquad (1)$$

where τ_1 and τ_2 are delays of respectfully lower and higher frequency oscillator's stages. Coefficient k should be set depending on values of τ_1 and τ_2 to meet this dependency.

In this case, the resolution of 2D Vernier TDC is same as of 1D Vernier TDC, but we are obtaining continuous Vernier plane of TDC's output time samples without breaks or missing points. The values of this plane can be calculated as shown in equation (2).

$$TDC_{OUT} = k \cdot X - (k-1) \cdot Y \qquad (2)$$

where X and Y are coordinates of Vernier plane, which show through how many stages propagated respectfully reference and DCO's signal.

Fragment of calculated plane of TDC's output time samples, when τ_1 is set to 10 ps, τ_2 is set to 9 ps, and k = 10, is shown in Fig. 6. GRO_{LL} and GRO_{HL} are lap counts of respectfully lower and higher frequency gated ring oscillator, GRO_{LE} and GRO_{HE} are edge counts in one lap of respectfully lower and higher frequency gated ring oscillator. Part of the plane, which is marked in green is used for calculation of TDC output. Grey area is not used for calculation - it marks negative time intervals which aren't measured by TDC. White area of the plane can be used for TDC output calculation if coefficient k is set to a different value, e.g. if k is set to 15, green area in first diagonal would extend to 15, recalculated values of second diagonal would be equal from 16 to 30, values of third diagonal – from 31 to 45, etc.

One of the main tasks in 2D Vernier TDC, which is based on gated ring oscillators, is output decoding. The output of arbiter will change to high logic level when arbiter's input, connected to GRO_H stage, will be high and

GRO_{HL}	GRO_{HE}	Y															
4	3	15	-125	-115	-105	-95	-85	-75	-65	-55	-45	-35	-25	-15	-5	5	15
	2	14	-116	-106	-96	-86	-76	-66	-56	-46	-36	-26	-16	-6	4	14	24
	1	13	-107	-97	-87	-77	-67	-57	-47	-37	-27	-17	-7	3	13	23	33
3	3	12	-98	-88	-78	-68	-58	-48	-38	-28	-18	-8	2	12	22	32	42
	2	11	-89	-79	-69	-59	-49	-39	-29	-19	-9	1	11	21	31	41	51
	1	10	-80	-70	-60	-50	-40	-30	-20	-10	0	10	20	30	40	50	60
2	3	9	-71	-61	-51	-41	-31	-21	-11	-1	9	19	29	39	49	59	69
	2	8	-62	-52	-42	-32	-22	-12	-2	8	18	28	38	48	58	68	78
	1	7	-53	-43	-33	-23	-13	-3	7	17	27	37	47	57	67	77	87
1	3	6	-44	-34	-24	-14	-4	6	16	26	36	46	56	66	76	86	96
	2	5	-35	-25	-15	-5	5	15	25	35	45	55	65	75	85	95	105
	1	4	-26	-16	-6	4	14	24	34	44	54	64	74	84	94	104	114
0	3	3	-17	-7	3	13	23	33	43	53	63	73	83	93	103	113	123
	2	2	-8	2	12	22	32	42	52	62	72	82	92	102	112	122	132
	1	1	1	11	21	31	41	51	61	71	81	91	101	111	121	131	141
			1	2	3	4	5	6	7	8	9	10	11	12	13	14	15 X
			1	2	3	1	2	3	1	2	3	1	2	3	1	2	3 GRO_{LE}
			0			1			2			3			4		GRO_{LL}

Figure 6: Calculated plane of TDC's output time samples, when τ_1 = 10 ps, τ_2 = 9 ps, k = 10

input, connected to GRO_L stage, is low. Since arbiters in 2D structure are connected between all stages of both gated ring oscillators, even first rising edge of GRO_H will trigger one or two arbiters. It happens because in three-stage ring oscillator, at any given moment the output signal of one or two inverters is low (it can be seen in Fig. 8, provided in next section). For this reason, such TDC can't measure time intervals lower than k using 2D structure and it is needed to evaluate if the output of arbiter is valid. E.g. in our example, if input time interval is lower or equal to 10, arbiter connected between first stage of GRO_H and second stage of GRO_L will become high with first GRO_H edge, since it will always lead second edge of GRO_L and output of TDC will be incorrectly set to 11 (X = 2, Y = 1 position in Fig. 6). This issue is solved by saving the state of arbiters after first GRO_H edge, which corresponds to GRO_{LE} in Fig. 6. This value, combined with lap count of GRO_L, will give total number of propagated GRO_L stages – coordinate X. After that checking is done in 1D Vernier manner: going diagonally up in Vernier plane, but only in diagonal, which is starting at coordinate X.

As discussed earlier, value of the coefficient k should meet equation (1). Coefficient k shows, that the total delay of k-1 stages of the lower frequency oscillator should be equal to the total delay of k stages of the higher frequency oscillator. Therefore, stage counters of the both oscillators can be employed to set needed value of the coefficient k.

Following guidelines can be used to set the values of coefficient k and number of turned on oscillator's sections (N_{OSC}) for both oscillators. At the beginning (e.g. after power-on of the chip) N_{OSC} for higher frequency oscillator can be set to highest available value N_{OSCH}, since, as it will be seen in the following section, frequency step, which corresponds to the resolution of TDC, is smaller at highest values of N_{OSC}, and N_{OSC} for lower frequency oscillator can be set to N_{OSCH}-1. After that both oscillators should be enabled and counters should count through how many stages of each oscillator signal has propagated. When value of stage counter of higher stage oscillator reaches targeted value of k, stage count of lower frequency oscillator should be checked:

- if it is equal to k-1, correct values of N_{OSC} are set for both oscillators;
- if it is equal to k – tuning step is too small for current value of coefficient k. Value of N_{OSC} for lower frequency oscillator should be decreased by one and measurement should be repeated. After that, if value of the counter drops to k-2, N_{OSC} for higher frequency oscillator should be decreased by one and measurement should be repeated. Also, coefficient k can be increased, since, as it can be seen from equation (1), higher k value is needed for lower tuning step when value of stage delay is constant.
- if it is equal to k-2 – tuning step is too large for current value of k. coefficient k should be decreased and measurement should be repeated.

After initial settings, measurement can be repeated for longer period of time, to validate correct values e.g. count to 4×k higher frequency oscillator's stages and check if count of lower frequency oscillator's stages is equal to 4×(k-1).

Additional fine-tuning can be done by using technique, described in [8] which takes advantage of the irregularity in automatic place-and-route, when different sections of the oscillator have different effective driving strength, resulting in different tuning step. i.e. same number of the enabled oscillator's sections can result in different stage delay, depending on the position in chip layout of the sections.

It should be noted, that incorrect value of k will introduce nonlinearity when TDC is operating in 2D Vernier mode i.e. measuring large input time intervals. When input time intervals are small and TDC is operating in 1D Vernier manner, value of the coefficient k has no effect for it.

Another advantage of 2D Vernier TDC is faster calculation of output signal, compared to 1D structure. The time duration to calculate the output of proposed TDC can be expressed as:

$$T_{IN} + \tau_2 \le T_{OUT2D} \le T_{IN} + k \cdot \tau_2 \qquad (3)$$

where T_{IN} – TDC's input time interval.

As it can be seen from equation (3), the time duration of TDC's output signal calculation depends nonlinearly on input time interval. Maximal time duration to calculate output signal of TDC is equal to $T_{IN} + k \cdot \tau_2$, i.e. after receiving the rising edge of DCO signal, it has to propagate through k stages of higher frequency gated ring oscillator.

The output of 1D Vernier TDC is calculated after:

$$T_{OUT1D} = T_{IN} + \frac{T_{IN}}{\Delta} \cdot \tau_1 \quad (4)$$

Output calculation time dependency on input time interval, when 2D and 1D TDC structure is used, is shown in Fig. 7. If τ_1 = 10 ps, τ_2 = 9 ps and TDC input time interval is 21 ps, from equations (3) and (4) it can be seen that TDC output will be calculated after 30 ps, when proposed TDC is used, and it will take 231 ps to calculate the output signal, if 1D Vernier TDC is used. Such long interval in latter case is obtained, because arbiters in 1D Vernier TDC are comparing signals only after respectful stages of ring oscillator (or delay line). After each stage, time interval between edges of reference and DCO output signals is reduced by Δ ps. Therefore, after receiving rising edge of DCO signal, it has to travel T_{IN}/Δ stages, to catch up with the edge of reference signals.

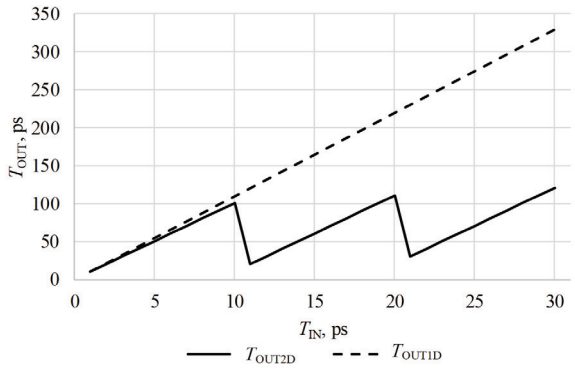

Figure 7: Output calculation time dependency on input time interval of proposed 2D time to digital converter and 1D Vernier time to digital converter

4 Modeling results

Functional modelling of TDC, implemented in VHDL hardware description language, was done using ModelSim environment. Figure 8 shows the results of functional modelling and main signals of TDC, when τ_1 and τ_2 are respectfully set to 10 ps and 9 ps. As it can be seen, when input time interval is equal to 8 ps, the output of TDC is calculated when eighth edge of higher frequency oscillator outruns eighth edge of lower

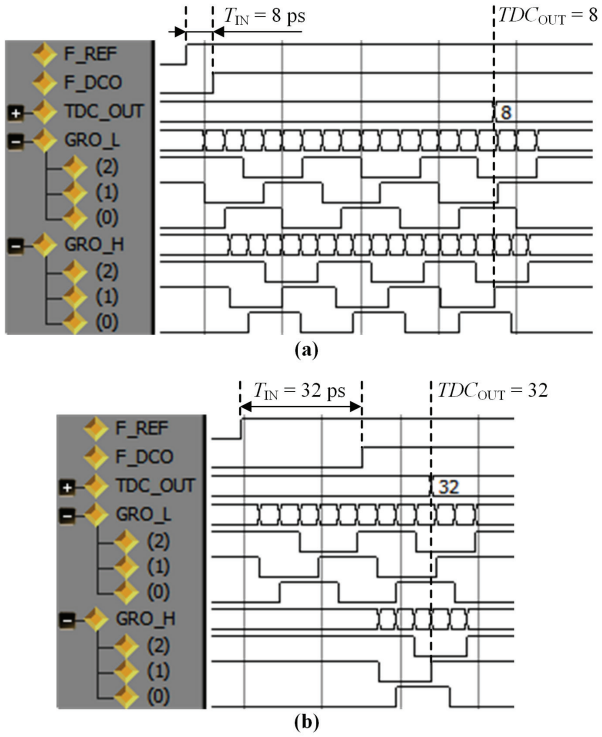

Figure 8: Time to digital conterver's functional modeling results, when input time interval is equal to 8 ps (a) and 32 ps (b)

frequency oscillator. When input time interval is equal to 32 ps, the output of TDC is calculated when second edge of higher frequency oscillator outruns fifth edge of lower frequency oscillator. These results correspond to data in Vernier plane, shown in Fig. 6.

TDC was synthesized, placed and routed in 65 nm CMOS technology using Cadence software. 48 parallel GRO sections were used to form both oscillators used in TDC. It is hard to model oscillators and their tuning using digital IC design tools. Therefore, additional post-layout transient simulations of synthesized oscillators were made using analog design approach to investigate its frequency and stage delays dependency on enabled number of GRO sections.
Simulations were made in three conditions:

- Typical: typical process corner, 1.2 V supply voltage, 40 °C temperature;
- Worst: slow process corner, 1.1 V supply voltage, 80 °C temperature;
- Best: fast process corner, 1.3 V supply voltage, -40 °C temperature;

Simulation results of frequency F_{OSC} dependency on number of turned on oscillator's sections N_{OSC} is shown in Figure 9 and corresponding stage delay τ is shown in Figure 10.

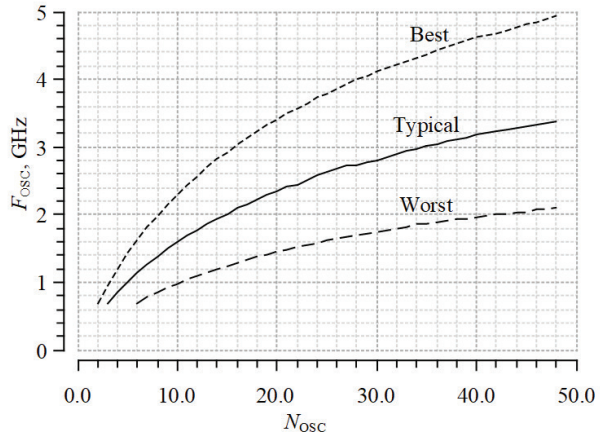

Figure 9: Dependency of frequency F_{OSC} on number of turned on oscillator's sections N_{OSC}

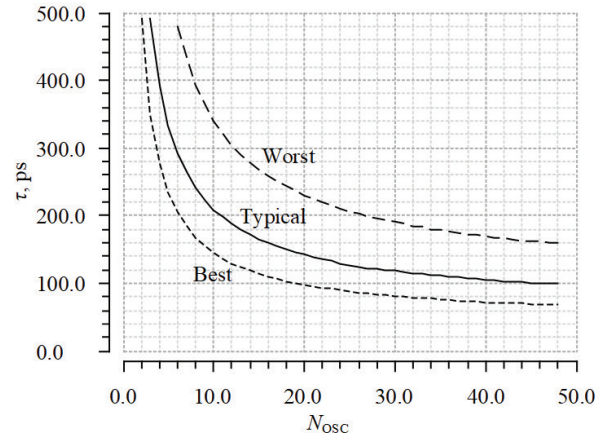

Figure 10: Dependency of stage delay τ on number of turned on oscillator's sections N_{OSC}

As it can be seen from Fig. 9 and Fig. 10, the stage delay changes depending on working conditions (process, voltage, temperature). Although in the 1D and 2D Vernier operation the difference of time delay is more important than the absolute value of stage delay, to compensate variation of the stage delay and to maintain same value

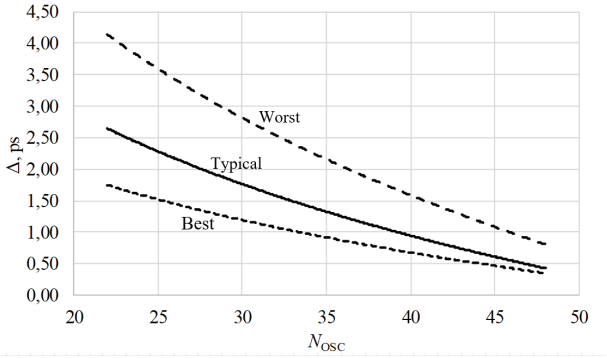

Figure 11: Step of oscillator's stage delay when number of enabled oscillator's sections changes from 22 to 48

of coefficient k at different values of temperature (e.g. at 25 °C and 65 °C), tuning technique from [8], which was mentioned earlier, can be used.

The frequency of GRO can be tuned from 0.68 GHz to 3.38 GHz in typical conditions, from 0.70 to 2.10 GHz in worst conditions, from 0.68 GHz to 4.93 GHz in best conditions. At least 3, 6 and 2 sections of oscillator need to be enabled respectfully in typical, worst and best condition for oscillator to start. Delay of single stage can be changed from 491 ps to 98 ps in typical conditions, from 479 ps to 158 ps in worst conditions and from 491 ps to 67 ps in best conditions.

As it can be seen, dependency of frequency and stage delay on turned on number of oscillator sections is nonlinear, similar to hyperbolic. Its slope is higher at low values of N_{OSC} and lower at higher values of N_{OSC}. Therefore, to achieve higher resolution of Vernier TDC, higher numbers of N_{OSC} should be used, where steps of oscillator's frequency and stage delay are smaller, since step of stage delay $\Delta = \tau(N_{OSC}-1) - \tau(N_{OSC})$ corresponds to the resolution of TDC if N_{OSC} sections are enabled in higher frequency oscillator and N_{OSC}-1 sections are enabled in lower frequency oscillator.

Table 1: TDC's performance comparison to other works

Reference	Structure	Technology	Resolution, ps	Supply, V	Current, mA	Area, mm²	Synthesised
This work	2D Vernier GRO	65 nm	3.2-0.8	1.2	3.0	0.008 (core); 0.018 (full)	Yes
[1]	Delay line	65 nm	10-30	1.2	N/A	N/A	No
[2]	Three-step	0.13 µm	1	1.2	2.9	N/A	No
[3]	Two-step	0.13 µm	4	1.2	3.7	0.028	No
[5]	2D Vernier delay line	65 nm	4.8	1.2	1.42	0.02 (core)	No
[6]	2D Vernier GRO	90 nm	2.2	1.0	2.3	0.068	No
[7]	Stochastic	0.13 µm	0.7	1.2	2.25	0.11	No
[8]	1D Vernier GRO	65 nm	5.5	1.0	1.4	0.006	Yes
[9]	1D Vernier GRO	90 nm	3.2	1.2	3.0	0.027	No

Recalculated step of oscillator's stage delay in close to linear fragment of Figure 10, when N_{OSC} changes from 22 to 48, is shown in Figure 11. In this part step of stage delay changes from 3.2 ps to 0.8 ps in typical conditions, from 4.0 ps to 1.1 ps in worst conditions and from 1.8 ps to 0.5 ps in best conditions. It should be noted, that the correct value of coefficient k should be set to meet the requirements of equation (1) as it was described in the previous section.

Summary of TDC's parameters and comparison to other works is presented in Table 1.

5 Layout

Layout of proposed time to digital converter, synthesized in 65nm CMOS technology is shown in Figure 12. The core of TDC occupies 75 µm × 100.8 µm space of silicon, total area of TDC including power rings is 123 µm × 148.8 µm.

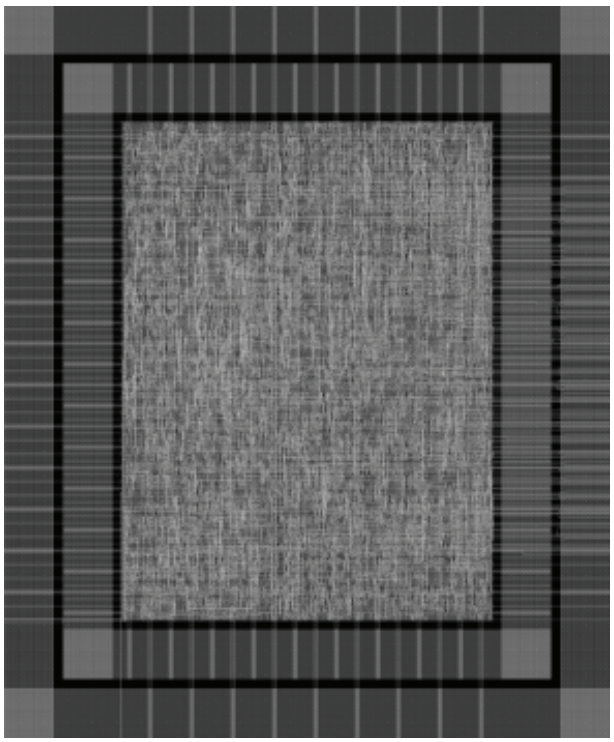

Figure 12: Layout of proposed time to digital converter

6 Conclusions

In this paper, synthesizable 2D Vernier time to digital converter (TDC) based on two gated ring oscillators and its control algorithm was proposed. Such TDC can measure sub-inverter delay time intervals and its result is calculated faster, compared to 1D Vernier TDC. Proposed TDC is implemented using VHDL hardware description language, therefore it can be easily migrated to various technology nodes. It was synthesized, placed and routed in 65 nm CMOS technology.

Main blocks of TDC are two oscillators, made of parallel-connected three stage gated ring oscillators (GRO), their lap and edge counters, arbiter matrix, decoder and control block. Frequency of oscillators and corresponding delay time of single stage are controlled by changing number of enabled GROs. To reduce metastability window of arbiters, they are composed of SR latches and D flip-flops.

Tuning step of single stage delay of gated ring oscillator, which is equal to the resolution of TDC, ranges from 3.2 ps to 0.8 ps at nominal conditions, when number of enabled oscillator's sections is changed from 22 to 48.

Total area of silicon occupied by time to digital converter, including power rings, is equal to 123 µm × 148,8 µm.

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