A New Low-Power CMOS Sample-and-Hold Circuit Based on High-Speed Dynamic Body Biased Switches

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Abstract: In this paper, a low-power open-loop CMOS sample-and-hold (S/H) circuit with improved linearity is presented. The incorporated switches utilize dynamic body connection technique to reduce distortions due to threshold voltage variations during track mode as well as signal feedthrough in the hold mode. To accomplish dual-edge sampling characteristic and differential operation, the proposed S/H circuit utilizes two pairs of the proposed switch and a 2:1 multiplexer. A current mode logic multiplexer without tail current is utilized to reduce power consumption while still fulfilling the speed and linearity requirements. The proposed S/H circuit is designed in a 90-nm CMOS process where it consumes approximately 610 µW from a 1.2 V supply voltage. Post-layout results show that a SFDR of about 73 dB is achieved when sampling a 1 GHz differential sinusoidal input at 2 GS/s rate using both edges of a 1 GHz clock signal.

Keywords: Sample and hold circuits; high-speed switches; body biasing; dual-edge sampling

Novo vzorčevalno vezje nizke moči na osnovi hitrih dinamičnih stikal

Izvleček: Članek opisuje odprtozančno CMS vzorčevalno vezje nizke porabe z izboljšano linearnostjo. Vgrajena stikala vnašajo dinamično povezovalno tehniko za zmanjševanje distorcij pri nihanju pragovne napetosti v načinu sledenja, kakor tudi prenos signala v stanju zadržanja. Za zagotaljanje dvorobne vzorčevalne karakteristike in diferencialnega delovanja sta v predlaganem vzorčevalnem S/H vezju uporabljena dva para stikal in 2:1 multiplekser. V tokovnem načinu je uporabljen logični multiplekser za zniževanje porabe energije, pri čemer se hitrost in linearnost ohranjata. Predlagano S/H vezje je načrtano v 90 nm CMOS tehnologiji in pri napajalni napetosti 1.2 V porabi okoli 610 µW. Rezultati izkazujejo 73 dB SFDR pri vzorčenju z 2 GS/s in difenecialni sinusni vzorčevalni frekvenci 1 GHz.

Ključne besede: vzorčevalna vezja; stikala velikih hitrosti; dvorobno vzorčenje

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1 Introduction

High speed sample-and-hold (S/H) circuits have found many applications in emerging communication systems such as software defined radio, direct RF sampling receivers and sub-sampling RF architectures [1-3]. The S/H circuits are substantially classified into two main groups of closed-loop and open-loop configurations. There is a main trade-off between linearity and speed in both types. Closed-loop S/Hs [4], [5] are more linear than open-loop counterparts while open-loop S/Hs [6-8], on the other hand, have relatively higher speed, less power consumption and less circuit complexity [7]. However, in very high speed applications, distortions imposed by embedded switches seriously limit their application. Charge injection and signal feedthrough, in the hold mode, beside threshold voltage variation due to body effect along with amplitude and phase distortion due to finite channel resistance, in the track mode, are blamed as the main sources of distortions [9], [10].

Transmission gates implemented by parallel connection of PMOS and NMOS transistors are the simplest way to implement a CMOS switch. However, the unequal turn-on and turn-off delays of PMOS and NMOS transistors makes them suitable only for applications with moderate precisions especially when fast switching operation is required [11]. A vast varieties of boot-

strap switches have been reported as linear and high-precision switches [12-14]. However, due to their circuit complexity and thus relatively lower speeds, they are not applicable in high speed applications. In this paper, a low-power high-speed sample-and-hold (S/H) circuit is proposed which takes the advantage of dynamic body connection technique to improve the linearity and speed of the incorporated switches. The paper is organized as follows; Section 2 illustrates the operation and analysis of the employed CMOS switches in details and then illustrates the implementation of the proposed S/H circuit. The results and discussion are provided in Section 3 followed by the conclusion in Section 4.
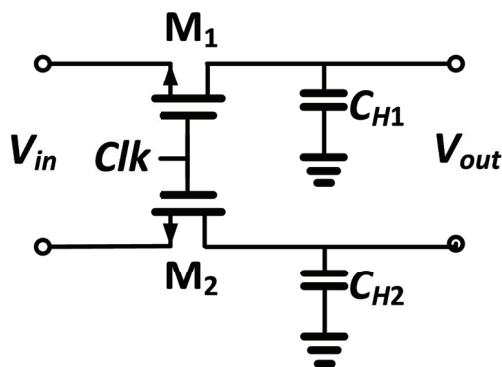

Figure 1: A simple differential CMOS switch

2 Proposed S/H circuit

Shown in Fig. 1, a simple differential switch can be realized using a pair of nMOS (or pMOS) transistors M_1, M_2 and holding capacitors C_{H1}, C_{H2}. When the switch is conducting (Clk=1), the transistors are in deep triode region and exhibit a channel resistance of:

$$R_{ON} = \frac{1}{\mu_n C_{ox} S (V_{GS} - V_{th})} \quad (1)$$

where μ_n is the electron mobility, C_{ox} is the gate-oxide capacitance, S denotes the transistor's aspect ratio and V_{GS} and V_{th} are gate-source voltage and threshold voltage, respectively. Reducing both R_{ON} and C_H results in better speed performance, however, a small C_H will significantly increases the impact of signal feedthrough on the sampled values leaving R_{ON} as the main means for alleviating the speed constraints. The simple switch shown in Fig. 1 also imposes phase and amplitude distortion during track mode mainly due to non-negligible switch resistance which can be evaluated as

$$\frac{V_{out}(j\omega)}{V_{in}(j\omega)} = \frac{1}{\sqrt{(\tau\omega)^2 + 1}} \exp\left(-j \tan^{-1} \tau\omega\right) \quad (2)$$

where $\tau = R_{ON} C_H$ is the switch time constant.

Charge injection and clock feedthrough are other sources of distortion in CMOS switches. Methods such as differential design and using dummy transistor have been suggested [11] to mitigate these problems. However, in the case of differential design, each side of the differential switch receives different input voltage, which causes unequal impact of charge injection and clock feedthrough on each side that cannot be totally removed in a common mode scheme. Moreover, process-related variations also worsen the problem so that charge injection and clock feedthrough always partially impose inevitable residues at the output.
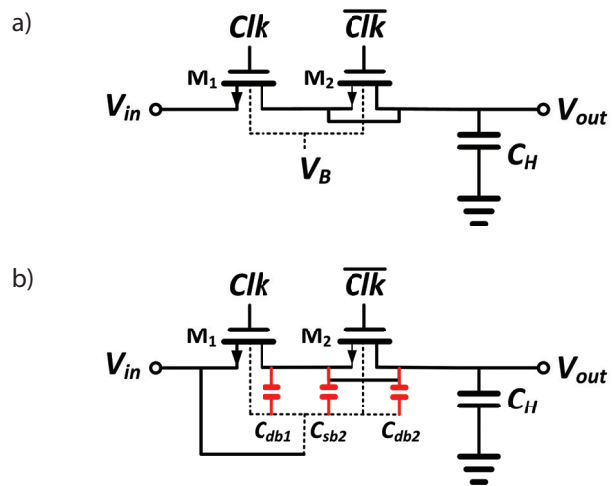

Figure 2: (a) MOS switch with constant body bias, (b) Signal feedthrough via parasitic capacitances when the body is connected to the source.

Shown in Fig. 2(a), to reduce the effects of non-idealities, there is benefits to using body-biasing technique. It is well-known that by applying a bias voltage to the bulk terminal of a MOS transistor, the threshold voltage decreases, which according to (1) and (2), lightens the amplitude and phase distortion. Obviously, the body bias voltage, V_B, should be applied to both switch transistor (M_1) and the dummy transistor (M_2) as it should be noted that an appropriate value for V_B, which allows for maximum input dynamic range with a symmetrical swing of at most 0.5 V, is the common-mode level of the input signal V_{in}. However, a problem which arises with applying a constant body bias to the bulk is that since the source-bulk voltage (V_{sb}) of switch transistor varies with V_{in}, its threshold voltage depends on the input signal, acting as a main cause of distortion. This problem can be solved by connecting the bulk terminal to the source instead of connecting it to a constant voltage of V_B. Nonetheless, an advantage of applying a positive voltage to the bulk, in comparison to tying the bulk to the source, is preventing the input signal to leak

to the output through drain-bulk parasitic capacitance in the hold mode. To elaborate more on this issue, Fig. 2(b) schematically illustrates this problem indicating that the ratio of the leaked signal to the output is

$$\frac{V_{out}}{V_{in}} = \frac{C_1}{C_1 + C_H} \qquad (3)$$

where $C_1 = C_{BD1} + C_{BS2} + C_{BD2}$ in which C_{BD} and C_{BS} are drain-bulk and source-bulk parasitic capacitances, respectively, so that subscripts 1 and 2 associate the parameters to M_1 and M_2, respectively. The both mentioned problems of the threshold voltage variation of constant-body-biased switches and signal feedthrough of switches with their body connected to the source can be effectively solved using body-bias control circuit first introduced in [15], and modified and then called here as dynamic body bias (DBB) switch. Shown in Fig. 3, the M_3 connects the body terminal of M_1 to its source terminal during track mode thus preventing threshold voltage variation due to the body effect. During hold mode, M_3 turns off disconnecting M_1 body node from its source node avoiding signal feedthrough through drain-bulk parasitic capacitance.
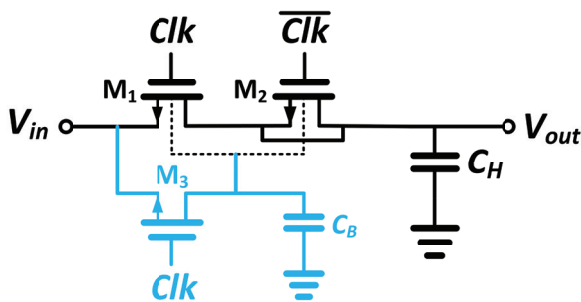

Figure 3: MOS switch with dynamic body connection technique. M3 connects the body nodes to the input to prevent distortion due to threshold voltage variation.

To analyze the feedthrough issue in the proposed DBB switch during hold mode (Clk=0), Fig. 4(a) shows how a capacitive coupling path between input and output is constructed by the parasitic capacitances of the M_1 and M_2. The equivalent circuit of the parasitic path is shown in Fig. 4(b) where the amount of feedthrough can be expressed by

$$\frac{V_{out}}{V_{in}} = \frac{C_{BS1}.C_1}{C_B(C_1 + C_H) + C_H(C_{BS1} + C_1) + C_{BS1}.C_1} \qquad (4)$$

Since C_B and C_H are sufficiently larger than C_{BS1} and C_1, (4) simplifies to

$$\frac{V_{out}}{V_{in}} \approx \frac{C_{BS1}}{C_B} \frac{C_1}{(C_1 + C_H)} \qquad (5)$$
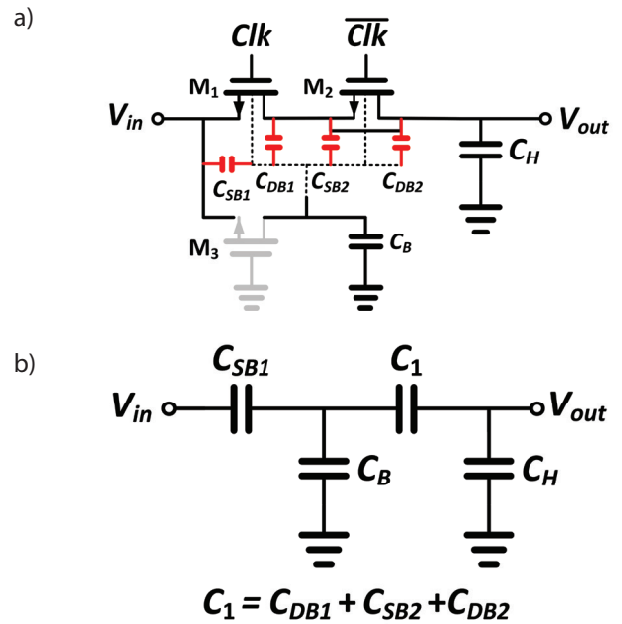
Figure 4: (a) The signal feedthrough via parasitic capacitances of the proposed switch, (b) equivalent circuit of the parasitic path.

Comparing (5) with (3), the amount of feedthrough has been considerably reduced by a factor of C_{BS1}/C_B.
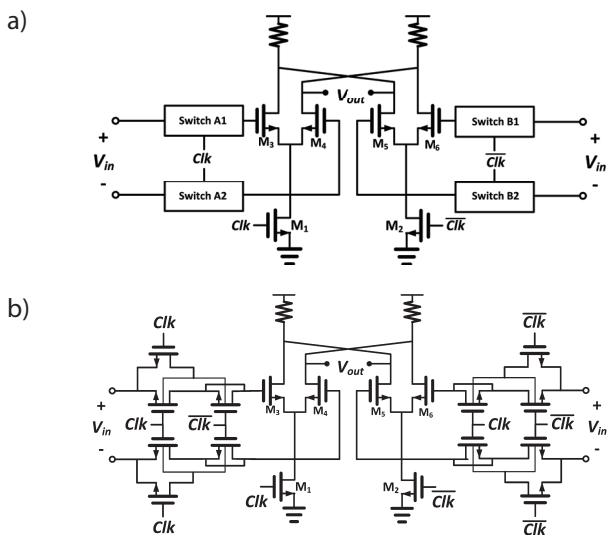
The dual edge triggered S/H circuit is realized using a pair of the proposed switch in differential configuration and a 2:1 multiplexer (MUX) circuit as conceptually illustrated in Fig. 5(a). The circuit is designed fully differential to improve its performance against common-mode distortions as well as supply and substrate noises [16]. Fig. 5(b) depicts the schematic circuit of
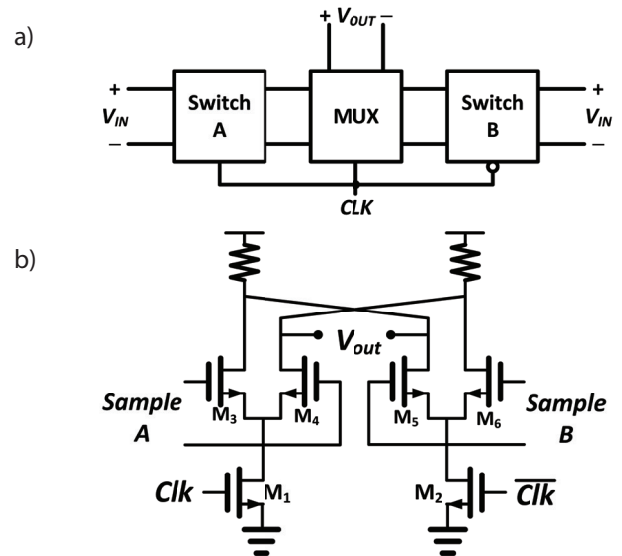
Figure 5: (a) The block diagram of the proposed dual-edge triggered S/H, (b) schematic circuit of the 2:1 CML MUX.

the incorporated 2:1 MUX. A high-speed current mode logic (CML) MUX without any specific tail current is utilized. The reason is to reduce the number of stacked transistors allowing for higher output swing. The M_1 and M_2 operate as current switches working in deep triode region (when turned on) with a small drain-source voltage. In addition, since higher voltage headroom is now available for M_3-M_6, their transconductances can be higher. In other words, we can reduce the sizes of these transistors while still having the same value of g_m comparing to the case with a specific tail current. Thus, the parasitic capacitances are reduced resulting in an improved speed.

Fig. 6(a) shows the structure of the proposed S/H circuit. The operation of the circuit is as follows. On the rising edge of the Clk, the switches B1 and B2 turn off providing a sample of the input signal at their output. At the same time, the switches A1 and A2 are conducting and track the input signal. On the falling edge of the Clk, the input will be sampled by the switches A1 and A2. Thus, on each clock edges a sample of the input is provided and thus the 2:1 MUX can choose the samples on each proper switch output. The circuit implementation of the proposed S/H circuit is shown in Fig. 6(b). Each differential switch is implemented using a pair of DBB switch where no explicit holding capacitor (i.e. C_H and C_B) is utilized. In fact, parasitic capacitances of the associated circuit nodes are sufficient for holding the samples over a short time.

Figure 6: (a) The structure of the proposed S/H circuit, (b) The schematic circuit of the proposed dual-edge triggered S/H circuit.

3 Simulation results

The proposed S/H circuit is implemented in a 90 nm CMOS process and post-layout simulations are carried out with a 1.2 V supply voltage while it consumes about 610 μW. To evaluate the performance of the switches, Fig. 7 compares the outputs of the switch with constant body bias (CBB) (shown in Fig. 2(a)) and the switch with dynamic body bias (DBB) (depicted in Fig. 3) when taking samples from a 500 MHz sinusoidal input having 200 mV amplitude (over 0.5 V common mode level). Their sampled values include an error voltage of about 12 mV and 7.5 mV, respectively. The dynamic body bias switches offer higher speed and less distortion.
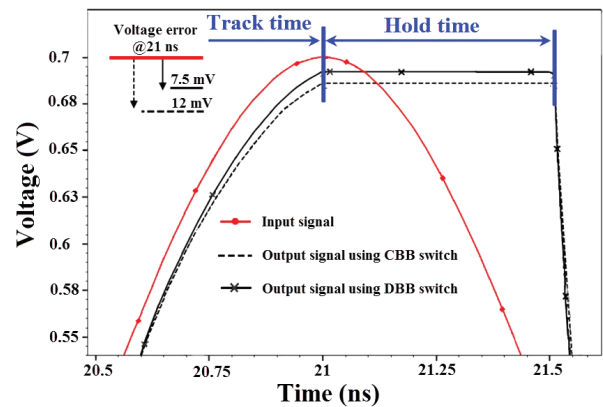
Figure 7: Comparison of samples taken by constant body bias (CBB) and dynamic body bias (DBB) switches.

Fig. 8 indicates the SFDR of the proposed S/H circuit employing various switches, i.e. the simple switch (shown in Fig. 1) and the CBB and DBB switches, supposing a differential sinusoidal waveform with 0.2 V amplitude is applied to the inputs sampled at a rate of 2 GS/s. The SFDR at Nyquist rate when incorporating the proposed DBB switch is about 73 dB. If using CBB switch the SFDR drops to about 69 dB. For the sake of comparison, the SFDR if using simple nMOS switch is also shown that is about 48 dB. Obviously, the circuit that benefits from
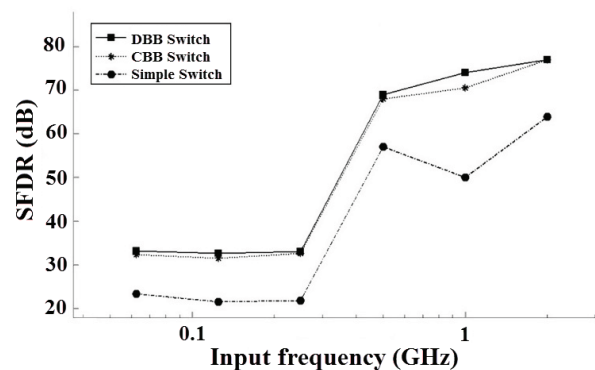

Figure 8: SFDR of the proposed S/H circuit versus input frequency incorporating different switches.

proposed switch achieves better SFDR since threshold voltage variations are reduced.

Table 1: Performance summary of the proposed dual edge triggered S/H circuit and its comparisons with some prior work

Design	This work	Ref. 3	Ref. 6	Ref. 8	Ref. 5	Ref. 7	
Technology	90 nm	90 nm	0.35 μm	0.18 μm	0.35 μm	0.18 μm	0.35 μm
Sampling rate	2 GS/s	~810 MS/s	250 MS/s	200 MS/s	400 MS/s	500 MS/s	250 MS/s
Supply voltage	1.2 V	1.2 V	_	1.8 V	2 V	_	_
Power consumption	610 μW	-	_	12.5 mW	6.7 mW	_	_
SFDR	73dB@1GHz	27.3dB* @ ~20GHz	_	76dB@200MHz	_	_	_
Configuration type	Open-loop	Open-loop	Open-loop	Open-loop	Closed-loop	Open-loop	Open-loop

The output of the circuit in response to a 1.25 GHz sinusoidal input sampled at a rate of 5 GS/s is also shown in Fig.9. The delay from the clock edges to the time that the samples settle at the output implies that the whole circuit has less than 0.1 ns delay from input to the output. Table 1 shows the proposed S/H circuit performance summary and its comparison with other recently published CMOS realizations. The circuit do not have static power consumption and the input switches are fully passive without extra power consumption causing the overall circuit to operate with a lower power. The ability of the circuit to operate at a relatively high sampling rate mainly comes from appropriate MUX architecture and the optimized switches.
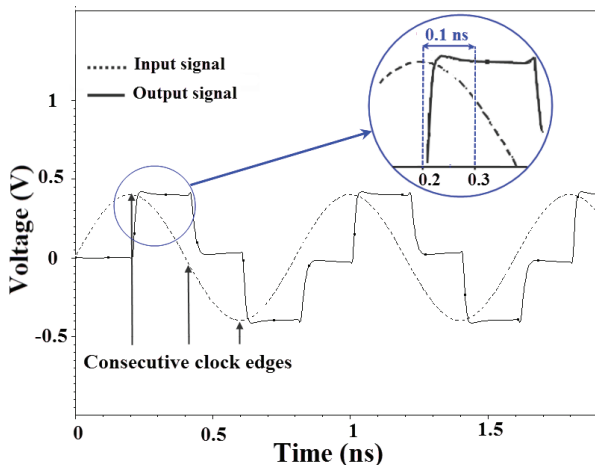
Figure 9: Sampling a 1.25 GHz sinusoidal input at a rate of 5 GS/s using a 2.5 GHz clock signal.

4 Conclusion

In this paper, a new architecture for open-loop S/H circuits was presented providing higher precision in

sampling. The switches were optimized using dynamic body bias technique in order to reduce distortions. It utilizes a CML multiplexer at the output operating in a switching manner as a means for dual edge sampling. The proposed S/H has some advantages compared to other open-loop counterparts, such as low complexity, low-power operation and fully differential configuration.

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