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Space transformer connector characterization for a wafer test system

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Abstract: Standard connections from the probe head to the PCB for vertical type probe cards in wafer test are individual separate wires in space transformers (STs), traditionally used for device pitches 80 µm and above for quick turn inexpensive solutions compared to multilayer ceramic substrates. There are inherent signal integrity issues using separate wires in controlling impedance, bandwidth, and cross-talk of STs and probe cards. A method of wiring that includes parallel pairs and twisted pairs is proposed and electrical characterization was performed to establish predictive specifications on the test cards.

Keywords: Semiconductor test; space transformers; paired-wiring schemes

Karakterizacija konektorja prostorskega pretvornika za testni sitem silicijevih rezin

Izvleček: V nasprotju s keramičnimi substrati se za razmake nad 80 µm uporablja poceni in hitre standardne priključke. Standardni priključek med glavo sonde in PCBjem vertikalnih sond pri testiranju silicijevih rezin predstavljajo ločene žičke in prostorski pretvorniki (ST). Uporaba posameznih žičk predstavlja problem inherentne integritete signala pri kontroli impedance, pasovne širine in presluha med ST in sondami. Predlagana je metoda povezovanja s prepletenimi paralelnimi pari. Opravljena je bila električna karakterizacija in napovedane specifikacije testnih kartic.

Ključne besede: test polprevodnikov; prostorski pretvorniki; sheme parnega ožičenja

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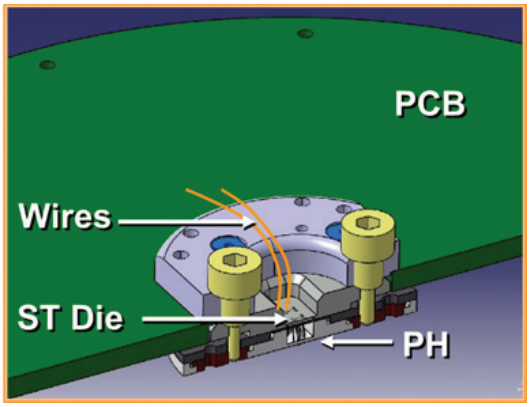
1 Introduction

In wafer test, main space transformers which provide connection between the probe head to the PCB in the test system include two common types. First one is typically wired space transformers (WST) and the second one is multilayer ceramic (MLC) or multilayer organic (MLO) types. Although MLC or MLO type space transformers offer better signal integrity for the test system, there are lead time and cost issues affecting the first silicon arrival on test floor. Typical WSTs utilize individual and separate wires for signals or gnd/power lines and are simple to produce mechanically without requiring photolithography. It makes them inexpensive and allow for quick turn vertical probe cards for mainly testing area-array devices such as logic, SoC, and microprocessors as the requirements for finer pitch, higher densities and lower cost of test are accelerating [1-3]. Higher total pin counts above 1000 for area array configurations are more difficult to accommodate depending on the designs compared to MLC type STs.

It is difficult to manufacture a ST with separate-wire-method according to well defined bandwidth or cross-talk specifications for vertical probe cards since there are inherent signal integrity issues using separate individual wires in controlling impedance, bandwidth, and cross-talk. High-speed data transmission using twisted pair cables for transport of telecommunication services or computer networks have been used in the telecom field [4-5]. These type of cables constitute larger diameters with long distances (i.e. Cable lengths of 100 m).

In this study, we have designed these interconnections with new wiring schemes and applied them on conventional space transformers where there is only one guide plate mounted on a PCB. We have experimentally measured the electrical characteristics of these wiring schemes on conventional or wired space transformers (WST). We have proposed earlier the interconnection and wiring schemes in a patent (US 8,430,676 B2) [6] and however, no measurement data was provided in the patent. The space transformer designs proposed were modular type which were different compared to electrical connection assembly of WSTs. In the patent, both parallel-pair or twisted wiring schemes were designed to apply to modular space transformers where there are two guide plates and wiring distances are much shorter, typically less than 20 mm, since spring pin contacts were (Fig 1D and 1E) also used. The top plate had spring pins inserted to mounting holes. The wire ends were connected via several means to the bottom ends of the pin springs inside an aperture. However, wire lengths required for WSTs are typically much higher from the guide plates to the solder connection pads on PCBs. This study provides actual experimental measurements on WSTs for the first time using paired wiring schemes to improve their electrical performance.

a)



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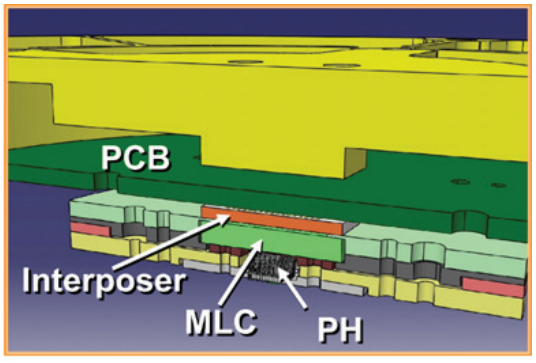


Figure 1: Illustrations of cross-sections of cards with two configurations; a) Probe card showing probe-head (PH) and wired space transformer; b) Probe card with PH, MLC and interposer structure

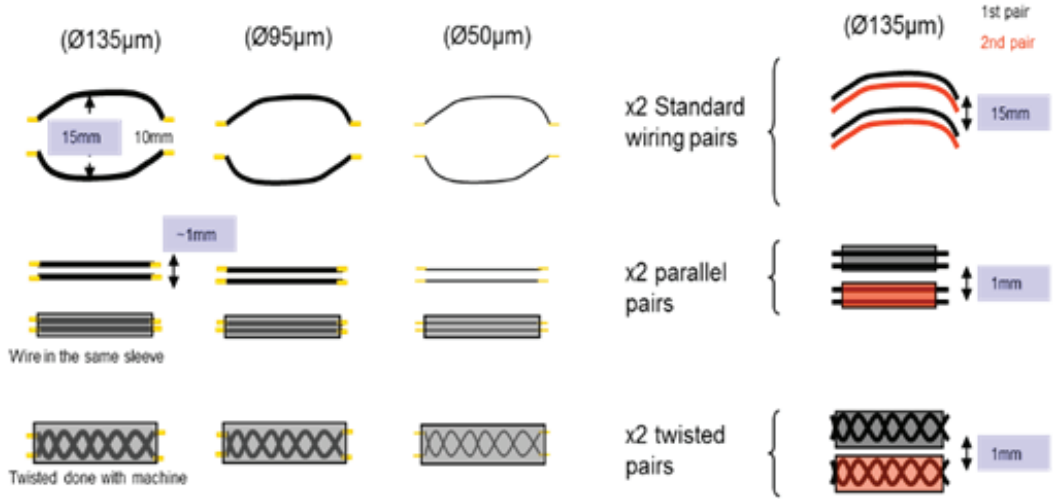
In this investigation, we propose a simple method of wiring that includes parallel and twisted pairs to improve performance and establish reliable ST specifications for semiconductor test system environment. The electrical characterization was performed on the test cards.

2 Design of wired ST and test prototypes

Fig. 1a shows a probe card showing a mechanical assembly of a probe-head (PH), wired space transformer and PCB (printed circuit board). It shows wire connection starting from PH side all the way to PCB sites. A probe card with a PH with probes, MLC and an interposer structure making connection to PCB is shown in Fig. 1b.

A test vehicle was designed and manufactured to characterize the bandwidth and cross-talk for three main vertical probe types corresponding to three different wire diameters, 50µm, 95µm, and 135µm. Wires are made of copper conductors. Bandwidth tests for wires corresponding to 2, 3, 4-mil probes according to wiring configuration which represents the parallel wire and the twisted wire. Crosstalk tests were designed with 3-mil probe configured ST wires according to new wiring configuration: parallel wire and twisted wire pairs. Standard ST electrical performance is not very predictable and the bandwidth is typically limited to 350 MHz and variable crosstalk values were observed based on simulations and characterizations done previously [3, 7]. The wire separation distances may vary greatly depending on the manufacturing process. We assume 10 mm to 15 mm in our studies for standard wiring. With newer configurations of wire connectors proposed, it will be possible to establish the specifications of the bandwidth and the crosstalk for both twisted wire vs parallel wire pairs for WST. The wire length for the experiments was fixed to 60 mm for all samples. Fig. 2 illustrates samples prepared for WST used in RF testing for bandwidth (50µm, 95µm, and 135µm wire pairs) tests on the left and for crosstalk tests for wire pairs for 135µm on the right. Parallel pairs were also inserted in a sleeve for better control of distances on separate wires. Distances between pairs were kept to 1 mm.

The measurement of S parameters was carried out using network analyzer, HP8722D, on a Gigatest GTL3030 probe station using Model Pico probes with appropriate pitch for contacting probe tips. Time domain reflectometry (TDR) measurements were also done to observe impedance variations in the same setup.



a. Bandwidth test **b. Crosstalk test**

Figure 2: Wire configurations for test vehicle; a) Samples for bandwidth tests; b) Samples for crosstalk tests

Both parallel and twisted paired wiring and the standard wiring in ST were built in a similar fashion and the wire still must travel through the PCB and over mechanicals. For simplicity, only critical and high speed lines were paired on the ST to keep manufacturing cycle short and achieve optimum performance. The design of device and pin configurations, location of signal and return paths, is important to establish GNDS on either side of the critical signal for a given test system.

On probe heads, the characteristic impedance and the bandwidth are mainly dependent on the electrical pitch since we can assume relatively short probes (< 4 mm in total length) are used compared to much longer wires in ST. The electrical signal-return path and pitch of the test system may not be the same as the device pitch, because other forward and return path probes can be utilized. It is critical to determine forward and return current paths in the design cycle of STs. Simulations indicated that speeds up to 10 GHz are possible for 2 or 3 mil-dia probes for their minimum allowable pitch configurations. However, this performance is not achieved for wired STs because the length of wires needed is much longer and it is difficult to control separation distance along the wire connection. So for a test system, we can ignore the PH for test speed requirements of 1 GHz, the critical components of the assembly become the space transformer and its connection to the PCB.

Table 1: Bandwidth measurements on the test vehicle with three different wire types and configurations for STs.

Configuration/ Wire Diameter	1 cm separation	1 mm separation	Parallel pair	Twisted pair
50 µm	100 MHz	180 MHz	640 MHz	3 GHz
95 µm	50 MHz	230 MHz	1.45 GHz	1.29 GHz
135 µm	100 MHz	270 MHz	1.65 GHz	1.27 GHz

3 Results

Table 1 summarizes the findings for three different diameters of wires for STs. For 4-mil probes (135µm wire ST configuration), results are very close to simulation results done earlier. As expected at 10mm wire separation, the bandwidth is measured close to 100 MHz at – 3 dB. It indicates that at 1mm separation, the bandwidth rises to 270 MHz at – 3 dB. When the parallel pair inside sleeve version is tested for the same wire diameter, it is good up to 1.6 GHz at – 3 dB. The bandwidth for the twisted pair is close to that of parallel pair, but it has little bit less bandwidth, 1.3 GHz at – 3 dB. This may be due to the fact that the twisted-pair wire separation is too close and there are variations along the length. A difference on the bandwidth is not expected between the twisted-wire versus the straight-wire on the measurements. The difference may be created if the twisted wire length is more than the straight wire length. The measured length of the wires on probe card was 60 mm on average. It is expected that the twisting of wire will provide crosstalk performance improvement since the induced voltage from different segments of the wire cancels out. For this type of wire layout with

1mm distance, the crosstalk is less than 30 dB (Fig. 3). To prevent serious crosstalk problems, the wire pairs should be close to each other. It is typically assumed that the distance between the two wires (ground and signal) is kept same along the 60 mm wire connection. In reality however, this is not the case for the end connections, especially for the ground connections near the probe-head side. The variation in the separation distance between the ground and the signal wire on main body of wires can introduce serious bandwidth performance issues.

As a general rule, the wire diameter is not the main source of the bandwidth limitation since the distance in between can be adjusted to achieve 50-ohm for a given diameter as long as mechanical probe card design rules allow. It is possible then to achieve the expected bandwidth with 95 µm dia. wire on built parts and the same bandwidth can be obtained with 135 µm or 165 µm dia. wires as long as the separation distance is adjusted properly. To optimize the probe card, the distance between two wires for a 95 µm wire case should be close to 105 µm. The insulation thickness for the wire should be 5 µm. The distance between two wires for a 135 um dia. wire case should be close to 147 µm. This implies the insulation thickness should be 6 µm. The distance between two wires for a 165 µm dia. wire case should be close to 181 µm. The insulation thickness needed is 8 µm.

For a proper manufacturing of a twisted-wire pair, wires should be in close contact with each other and irregular air gaps should not be allowed. For the optimum connection trace lines, the total length of wires should be reduced as much as possible. The total electrical performance of this structure is mostly dominated by the length of the wires (60 mm) rather than the wire diameter in the design. It is known that the number of twists on wire pairs will affect the crosstalk. A higher crosstalk cancellation on higher frequencies is expected, as the number of twist rises. To cancel the crosstalk, it is best at least to make one twist per one tenth of the wavelength for a given frequency. To calculate the wavelength we can use 'wavelength = speed of light / frequency'. For example, a twist per 3-mm will give rise to a crosstalk attenuation up to 10 GHz. Similarly, a twist per 6-mm of wire pair length will support a crosstalk attenuation up to 5 GHz. Another effect to consider is the angle between the victim line and aggressor line when they are less than 180 degree. This would also make the analysis complex. More number of twists allow for better attenuation on crosstalk. It should be noted that if the twisting increase the total wire length significantly compared to a straight-wire case, the bandwidth will be reduced compared to a straight-line case. Therefore, moderate twisting in wire-pair formation process should be preferred for optimal results.

3.1 S-parameter in dB

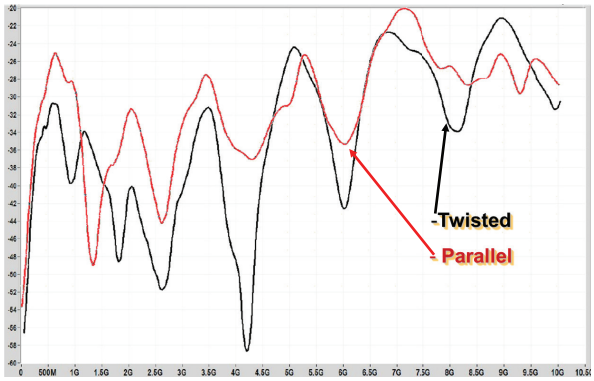


Figure 3: S21 data-Crosstalk for ST with 1 mm-distance for parallel and twisted pairs of 135µm diameter wires.

In wafer test, there are many configurations of device types especially for logic and mixed signal applications and the multi-device testing is always critical from the test efficiency and yield perspectives. However, the fab teams require very short lead times for initial test results from the design time and fab to the first silicon. This forces teams to use certain vertical probe-card types which allow versatile designs and short cycles. In this family, vertical or cobra type probe cards with WSTs offer a good solution due to their simplicity and cost. The pitch is easy to customize and several suitable wire types with proper diameters are readily available for WSTs. WSTs offer lead time advantages of at least 4-5 weeks (1-2 weeks vs 6-8 weeks) compared to MLC (multilayer ceramic substrate) or MLO (multilayer organic substrate) in the probe card assembly. This lead time differential is crucial in some cases for the first silicon test. The cost for MLC/MLO is also 5-10 times more expensive. If the lead time is not critical and the volume count for probe cards are high, only then the probe card solutions with MLC/MLO assembly become a reasonable option. The factors to consider when choosing the best fit of STs for device types include the pitch, line numbers per device (1 or 2 rows), peripheral rows (1-3), number of DUTs (device under test), configuration (partial area array or full array) and area size for each DUT. There are five common classes of substrate systems of interconnects different than WSTs that are used in connecting probe heads to PCB and tester system. These can mostly support impedance-matched traces for signal transmission lines, except for via-sections, produced by layered-lithographic production methods.

MLC: Multi-Layer Ceramic, can be with standard thin film or Multi-layer Thin Film (MTF)

MLC: LTCC (low-temperature co-fired ceramic) or HTCC (hi-temperature co-fired ceramic) types.

MLO: Multi-Layer Organic made from packaging technology, laminated core with several microvia build-up layers

HDI PCB: High Density Interconnect made from PCB technology, laminated layers with through hole and microvia on 1 buildup layer

Direct Attach: PCB with embedded pads in the center area

These substrates or space transformers are either connected by BGA (Ball Grid Array) using soldering or spring pin connected by PGA (Pin Grid Array) to main PCB and the test system. Interconnects with BGA-arrays are hard to repair due to solder-connection in case of channel failures. PGA-type interconnects are repairable, however, they can apply very high force levels when pin counts are above 2500. PGA-type connection is used mainly for HTCC since they are strong and thick ceramic substrates can better withstand bending. WSTs are typically repairable and do not induce any pin force into the PCB or the probe-head. They are also the lowest cost STs. HDI PCB density limitations arise as the pitch shrinks and Direct Attach process are only feasible when large pitch allows manufacturing PCBs for a particular design. Fine pitch device testing typically cannot be supported by HDI PCB or Direct Attach.

4 Conclusion

Electrical characterization of proposed designs of wire pairs of parallel and twisted types was carried on test vehicles for vertical probe card applications. When the parallel pair inside sleeve version is tested for the wire diameter of 95 µm, it is good up to 1.45 GHz at – 3 dB. To optimize the probe card, the distance between two wires for 95 µm wire should be close to 105 µm. So the insulation thickness for the wire should be 5 µm. Studies on wire diameters of 50µm, and 135µm were performed and presented for both parallel pair and twisted wire types for space transformers.

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