Original scientific paper

Informacije MIDEM
Journal of Microelectronics,
Electronic Components and Materials
Vol. 48, No. 1(2018), 53 – 61

Subthreshold Modeling of Triple Material Gate-All-Around Junctionless Tunnel FET with Germanium and High-K Gate Dielectric Material

G. Lakshmi Priya[1], N. B. Balamurugan[2]

[1]Jerusalem College of Engineering, Chennai, India
[2]Thiagarajar College of Engineering, Madurai, India

Abstract: In this paper, a subthreshold analytical model for Triple Material Gate-All-Around (TMGAA) Junctionless Tunnel FET (JLTFET) with Germanium and High-K gate dielectric material is developed. Various performance metrics like Transconductance-to-Drain Current ratio, Subthreshold leakage current, and Subthreshold Swing are derived to model the subthreshold behavior of the device. The gate structure incorporates the effect of Germanium (Ge) and High-K gate dielectric material (Titanium Oxide) to combat the adverse effects imposed by the short channel. The subthreshold characteristics of Ge based JLTFET is compared with Silicon (Si) based TFET with SiO_2 as gate dielectric. The results concede that the developed model is highly immune to hot carrier damage because of high transconductance-to-drain current ratio of 50 V^{-1}, minimal leakage current, and subthreshold swing less than 40 mV/dec. The results of the proposed analytical model are validated using 2-D Sentaurus TCAD device simulator.

Keywords: Germanium; Junctionless; High-K gate dielectric; Hot Carrier Reliability; Tunnel FET; Transconductance-to-Drain Current ratio; Subthreshold Current; Subthreshold Swing.

Podpragovno modeliranje brezspojnega tunelskega FET iz treh materialov in neprekinjenimi vrati z germanijem in vrati iz dielektrika z visokim K

Izvleček: V članku je predstavljen podpragovni analitični model brezspojnega tunelskega FET (JLTFET) iz treh materialov in neprekinjenimi vrati (TMGAA) z germanijem in vrati iz dielektrika z visokim K. Za modeliranje podpragovnega obnašanja elementa so uporabljeni številni parametri, kot so razmerje transkonduktance s ponornim tokom, podporagovni uhajalni tok in podpragovni razpon. Za kompenziranje vplivov kratkega kanala struktura vrat vključuje vpliv germanija in titanovega oksida kot dilektričnega materiala z visokim K. Podpragovna karakteristika JLTFET z germanijem je primerjana silicijevim TFET z vrati iz SiO_2. Rezultati izkazujejo, da je model neobčutljiv na poškodbe vročih elektronov zaradi visokega transkonduktance s ponornim tokom (50 V^{-1}), majhnega uhajalnega toka in podpragovnega razpona manjšega od 40 mV/dec. Rezultati so potrjeni z analitičnim modelom v 2-D Sentaurus TCAD simulatorju.

Ključne besede: germanij; brezspojno; isolator vrat z visokim K; vroči elektroni; tunelski FET; razmerje transkonduktance s tokom ponora; podpragovni tok; podpragovni razpon

** Corresponding Author's e-mail: priya0217@gmail.com*

1 Introduction

Aggressive downscaling of devices has almost reached a sub-nanometre regime, which deteriorates the gate control over the channel. Several novel device architectures have been introduced to suppress the Short Channel Effects (SCEs) [1]. For many technology generations, the gate electrode structures were made of silicon and silicon dioxide as gate dielectric material. As the channel length is reduced tremendously, other potential alternatives have to be explored to improve the subthreshold device characteristics [2 - 5]. Conventional Si based TFETs, suffers from an exponential increase

of the subthreshold leakage current and requires a very high gate voltage for TFET operation. Also, due to the continuous scaling of oxide thickness, the gate leakage current through the SiO_2 layer will be high. A potential candidate to continue FET scaling with improved subthreshold characteristics is Junctionless Tunnel FET (JLTFET) [6].

Junctionless FETs (JLFETs) have several advantages like diminished short channel effects, high I_{ON}/I_{OFF} ratio and nearly ideal subthreshold slope (SS ~ 60 mV/dec). The concept of gate material engineering is also incorporated to overcome the adverse short channel effects. Many analytical models have been proposed for junctionless TFETs. Triple Material Gate-All-Around (TMGAA) structures employ three gate materials with different work functions.

The gate material engineering [7 – 8] suppresses the peak electric field at the drain side, which is interpreted as a continuous reduction of Hot Carrier Effects (HCEs). Along with this, the usage of Germanium and Titanium Oxide (TiO_2) as High-K gate dielectric material [9 – 14] will improve the hot carrier reliability of the proposed device. High-K gate dielectric materials will minimize the tunneling of electrons through the gate-oxide interface and hence gate leakage current will also be minimized.

Subthreshold Current/Swing plays a vital role in low power circuits [15 – 19]. The use of Ge-based TMGAA-JLTFETs will efficiently enhance the subthreshold characteristics of the device. Device scientists have disclosed numerous analytical models for subthreshold analysis of MOSFETs [20 – 24]. But the effectiveness of combined design of Germanium (Ge), High-K gate dielectric (Titanium Oxide – TiO_2), Gate-All-Around (GAA) structure and three region doping profile in the channel has not yet been explored in short channel (12nm) junctionless tunnel FETs. Therefore, in this research work, we have developed a subthreshold analytical model of 12nm Triple Material Gate-All-Around (TMGAA) Junctionless Tunnel FET (JLTFET) with Germanium and High-K gate dielectric material for improved hot carrier reliability. An intensive comparative study with Si-SiO_2 interface is also carried out and the analytical model results are also simulated using TCAD.

In this paper, subthreshold analytical modeling has been developed by solving the 2-D Poisson equation by parabolic approximation. The key performance parameters like transconductance-to-drain current ratio, subthreshold current and subthreshold swing are derived by varying the device parameters such as drain-to-source voltage, germanium thickness, oxide thickness, channel length, and doping concentration. The obtained analytical and simulation results manifests that this transistor possesses higher transconductance, lower leakage current and steeper subthreshold slope compared to the bulk silicon FETs. The proposed analytical model results are validated using TCAD Sentaurus device simulator.

2 Mathematical Modeling

The cross sectional view and structure of the 12nm Ge based Triple Material Gate-All-Around Junctionless Tunnel FET (Ge-TMGAA-JLTFET) is shown in Fig.1. In this structure, the gate electrode comprises of three materials M1, M2, and M3 with different work functions. These three distinct materials are deposited over the respective gate lengths L_1, L_2 and L_3, with total gate length (12 nm) defined as $L = L_1 + L_2 + L_3$. The gate materials are chosen in such a way that $\emptyset_{M1} > \emptyset_{M2} > \emptyset_{M3}$. The work function of tunneling gate metal M_1 is $\emptyset_{M1}$ = 4.8 eV (Au), gate material M_2 with $\emptyset_{M2}$ = 4.6 eV (Mo), gate material M_3 at drain side is with $\emptyset_{M3}$ = 4.4 eV (Ti). The proposed model has a 12nm germanium channel, which is heavily n-type doped at $10^{19}cm^{-3}$. The formation of source and drain regions is without separate doping on the germanium channel.

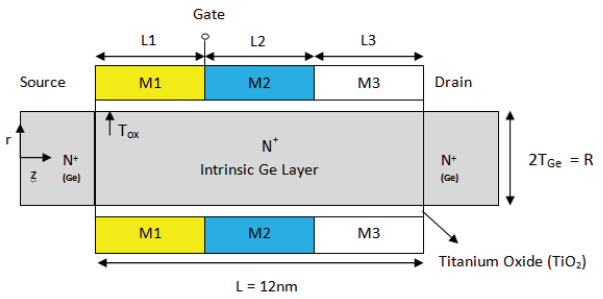

Figure 1: Cross section of 12nm Ge based Triple Material Gate-All-Around Junctionless Tunnel FET (Ge-TMGAA-JLTFET)

The 2-D Poisson's equation for the potential distribution in the channel is written as [4],

$$\frac{1}{r}\frac{\partial}{\partial r}\left(\frac{r\partial\phi_i(r,z)}{\partial r}\right)+\frac{\partial^2\phi_i(r,z)}{\partial z^2}=-\frac{qN_D}{\varepsilon_{Ge}};i=1,2,3 \quad (1)$$

where Ø(r, z) is the 2-D channel potential profile, q is the electric charge, N_D is the channel doping concentration, which is assumed to be uniform and ε_{Ge} is the permittivity of germanium. The potential profile in the vertical direction can be related by a simple parabolic function given by,

$$\phi(r,z)=S_1(z)+S_2(z)r+S_3(z)r^2 \quad (2)$$

where $S_1(z)$, $S_2(z)$ and $S_3(z)$ are arbitrary functions of z only.

The Poisson's equation is solved separately under the three gate metal regions by considering the boundary conditions stated below:

(a) The surface potential is a function of z only.

$$\phi(r=0,z)=S_1(z)=\phi_S(z) \tag{3}$$

(b) The electric field in the center of germanium pillar is zero.

$$\left.\frac{\partial\phi(r,z)}{\partial z}\right|_{r=0}=0 \tag{4}$$

(c) The electric field at the gate oxide interface is continuous.

$$\left.\frac{\partial\phi(r,z)}{\partial z}\right|_{r=R}=\frac{\varepsilon_{ox}}{\varepsilon_{Ge}R}\left[\frac{\psi_G-\phi_S(z)}{\ln\left(1+\frac{t_{ox}}{R}\right)}\right] \tag{5}$$

(d) The potential at the source end is:

$$\phi\left(r=0,z=0\right)=V_{bi} \tag{6}$$

(e) The potential at the drain end is:

$$\phi(r=R,z=L=L_1+L_2+L_3)=V_{bi}+V_{ds} \tag{7}$$

where, $\psi_G=V_{GS}-\phi_{M_i}+\chi+\frac{E_G}{2};i=1,2,3$ (8)

V_{GS} is the gate to source bias, E_G is the energy band gap of germanium, χ is the electron affinity of germanium, $\emptyset_{Mi}$ is the gate metal work function of three different materials and V_{bi} is the built-in potential.

In germanium based TMGAA-JLTFETs, we have three different gate materials with different work functions. Hence, the flat-band voltage for the three gate metal regions can be written as;

$$V_{FB_1}=\phi_{M1}-\phi_{Ge};V_{FB_2}=\phi_{M2}-\phi_{Ge};V_{FB_3}=\phi_{M3}-\phi_{Ge} \tag{9}$$

Where $\emptyset_{M1,}$ $\emptyset_{M2}$ and $\emptyset_{M3}$ denote the work functions of three different gate materials and $\emptyset_{Ge}$ is the work function of germanium.

Using the boundary conditions (3 – 7), we get the potential distribution under each gate metal region as;

$$\phi_{S1}(z)=P_1e^{\lambda z}+Q_1e^{-\lambda z}-\frac{\phi_{g1}}{\lambda^2};\quad for\quad 0\le z\le L_1 \tag{10}$$

$$\phi_{S2}(z)=P_2e^{\lambda(z-L_1)}+Q_2e^{-\lambda(z-L_1)}-\frac{\phi_{g2}}{\lambda^2};\ for\ L_1\le z\le L_1+L_2 \tag{11}$$

$$\phi_{S3}(z)=P_3e^{\lambda(z-(L_1+L_2))}+Q_3e^{-\lambda(z-(L_1+L_2))}-\frac{\phi_{g3}}{\lambda^2};\quad for\ L_1+L_2\le z\le L_1+L_2+L_3 \tag{12}$$

where the constants P_i and Q_i shown in (10 - 12) are obtained from the boundary conditions (3 - 7)

$$P_i=\frac{1}{(e^{\lambda L_i}-e^{-\lambda L_i})}\left[V_{bi}(1-e^{-\lambda L_i})+\frac{\phi_{g_i}}{\lambda^2}(1-e^{-\lambda L_i})+V_{ds}\right];i=1,2,3 \tag{13}$$

$$Q_i=\frac{1}{(e^{\lambda L_i}-e^{-\lambda L_i})}\left[V_{bi}(e^{\lambda L_i}-1)+\frac{\phi_{g_i}}{\lambda^2}(e^{\lambda L_i}-1)-V_{ds}\right];i=1,2,3 \tag{14}$$

The minimum surface potential under the gate metal region M_1 is given by:

$$\frac{d\phi_{S1}(z)}{dz}\Big|z=z_{\min}=0 \tag{15}$$

$$\phi_S(z_{\min})=2\sqrt{P_1Q_1}-\frac{\phi_g}{\lambda^2} \tag{16}$$

where, $\phi_g=-\left[\frac{qN_D}{\varepsilon_{Ge}}+\lambda^2\psi_G\right]$, $\lambda^2=\frac{2\varepsilon_{ox}}{R^2\varepsilon_{Ge}\ln\left(1+t_{ox}/R\right)}$ *and* $z_{\min}=\frac{1}{2\lambda}\ln\left(\frac{Q_1}{P_1}\right)$ (17)

2.1 Transconductance-to-Drain Current Ratio

The Transconductance-to-Drain Current ratio is strongly related to the performance measure of a device. This is obtained by differentiating the minimum surface potential with respect to gate-to-source voltage and it is given by [23],

$$\frac{g_m}{I_{ds}}=\frac{\frac{\partial\phi_S(\min)}{\partial V_{gs}}}{\frac{K_BT}{q}} \tag{18}$$

where K_B denotes Boltzmann constant = 1.38x10^{-23} and T is the Temperature.

On substituting (16) in (18), we get the Transconductance-to-Drain Current ratio as,

$$\frac{g_m}{I_{ds}} = \frac{-q}{K_B T \alpha}\left[\left(\sqrt{2(\beta-1)}\right)\left(1+\frac{1}{2\sqrt{V_{GS}}}\right)\right] \quad (19)$$

$$where\ \alpha = (e^{\lambda L_1} - e^{-\lambda L_1})/2\ \ and$$

$$\beta = -(e^{\lambda L_1} - e^{-\lambda L_1})/2$$

2.2 Subthreshold Current

In order to reduce the low power consumption, the supply voltage has been scaled down aggressively, which has driven attention towards the subthreshold leakage current. Hence, current in this subthreshold region has to be determined to assess the performance and reliability of the device.

The net current density in a semiconductor device can be defined as the total sum of drift and diffusion current densities. For Junctionless TFETs, the doping profile is uniform throughout the channel and because of the absence of concentration gradient, diffusion current density is neglected.

Hence, the total current density of Ge-TMGAA-JLTFET is written as,

$$J(r,z) = -q\mu n(r,z)E(z) \quad (20)$$

where E(z), is the applied electric field along the position of the channel (z).

In general, there are two electric field components which depends on both r and z. The electric field component along the channel is lateral electric field E (z) and the electric field component perpendicular to the channel is vertical electric field E(r). While analyzing the subthreshold current of the device, only E (z) is considered. Since, electron transport velocity along the channel can only be determined by the lateral electric field component (i.e. E (z)), which is obtained as follows,

$$E(z) = \frac{d\phi(r,z)}{dz} = \left[\frac{\lambda}{Sinh(\lambda L_j)}\right]\begin{bmatrix} V_{bi}\left[Cosh(\lambda z) - Cosh(\lambda(z-L_j))\right] \\ +\frac{\phi_{g_j}}{\lambda^2}\left[Cosh(\lambda z) - Cosh(\lambda(z-L_j))\right] \\ +V_{ds}\left[Cosh(\lambda z)\right] \end{bmatrix}; j = 1,2,3 \quad (21)$$

and $n(r,z) = n_i \exp\left(\frac{q}{K_B T}\left(\phi_j(r,z)\right)\right); j = 1,2,3$ is the electron carrier concentration.

By integrating (20), the subthreshold current is expressed as:

$$I_{ds}(z) = -\int_0^R q\mu\pi t_{ge} n_i \exp\left(\frac{q}{K_B T}\left(\phi_j(r,z)\right)\right)\left[\frac{\lambda}{Sinh(\lambda L_j)}\right] x$$

$$\begin{bmatrix} V_{bi}\left[Cosh(\lambda z) - Cosh(\lambda(z-L_j))\right] \\ +\frac{\phi_{g_j}}{\lambda^2}\left[Cosh(\lambda z) - Cosh(\lambda(z-L_j))\right] \\ +V_{ds}\left[Cosh(\lambda z)\right] \end{bmatrix} dr \quad (22)$$

By assuming that the subthreshold leakage occurs primarily at $z = z_{min}$, we obtain the subthreshold current as,

$$I_{ds} = \frac{\mu\pi t_{ge}^2 n_i^2 K_B T\left(1 - e^{-qV_{ds}/K_B T}\right)}{\delta N_D} \quad (23)$$

where $\delta = \exp\left(\vartheta_1 + \vartheta_2 + \vartheta_3\right)$

$$\vartheta_l = \frac{L_l}{q\left(\phi_{l,\min}/K_B T\right)}; l = 1,2,3$$

And μ = *electron carrier mobility = 3900 cm^2 /(V – s).*

2.3. Subthreshold Swing

Subthreshold swing normally describes the exponential behaviour of leakage current. For devices requiring high speed and low power, the subthreshold swing should be minimized. With steep subthreshold swing, improved I_{ON}/I_{OFF} ratio can be obtained and device reliability can be enhanced. Subthreshold slope is defined as the change in gate voltage required to reduce the subthreshold current by one decade. Subthreshold swing is the inverse of subthreshold slope.

Subthreshold swing is given as [24],

$$SS = \left(\frac{\partial \log I_{DS}}{\partial V_{GS}} \right)^{-1} \tag{24}$$

After approximation we obtain;

$$SS = \frac{K_B T}{q} \ln(10) \left[\frac{\partial \phi_{s,\min}}{\partial V_{gs}} \right]^{-1} \tag{25}$$

where,

$$\frac{\partial \phi_{s,\min}}{\partial V_{gs}} = \frac{\partial}{\partial V_{gs}} \left(\frac{\left\{ \left[\left(V_{bi} + \frac{\phi_{g1}}{\lambda^2} \right) \sqrt{2(\beta - 1)} \right] - V_{ds} + \left[V_{ds} \sqrt{2(\beta - 1)} \left(V_{bi} + \frac{\phi_{g1}}{\lambda^2} \right) \right] + \left[\frac{qN_D}{\varepsilon_{Ge}} + \lambda^2 (V_{GS} - V_{FB}) \right] \right\}}{Sinh(\lambda L_1)} \right) \tag{26}$$

On substituting (26) in (25) and on simplification, the final expression of subthreshold swing is obtained as,

$$SS = \frac{K_B T}{q} \ln(10) \left[\frac{-1}{\alpha} \left[\sqrt{2(\beta - 1)} \left(1 + \frac{1}{2\sqrt{V_{GS}}} \right) \right] \right]^{-1} \tag{27}$$

3 Results and Discussions

The proposed analytical model is verified using a 2-D TCAD device simulator. With uniformly n-type doped (N_d=10^{19}cm^{-3}) source, drain and channel regions, a germanium based TMGAA Junctionless TFET structure is implemented. The developed model has a triple material gate-all-around structure, where the work functions of gate metals M1, M2 and M3 are chosen to be 4.8eV, 4.6eV, and 4.4eV respectively. The analytical model results are plotted using MATLAB and compared with the TCAD device simulator results. Drift Diffusion (DD) model has been employed to model the carrier transport mechanism in device simulation. Also, to model the carrier concentration, Shockley-Read-Hall (SRH) recombination model combined with Auger recombination model are used in the simulation.

The total channel length of the proposed device is chosen to be 12nm. The remaining device parameters used are: channel thickness (t_{ge}) is 2nm, gate-oxide thickness (t_{ox}) is 1nm and V_{ds} = 0.3V. The length of the three gate metal regions is: L_1= L_2= L_3=4nm.

The transconductance-to-drain current ratio of 12nm germanium and silicon based triple material gate-all-around junctionless tunnel FET is shown in Fig.2. The results clearly indicate that the developed Ge based TMGAA-JLTFET has higher value of transconductance-to-drain current ratio of nearly 50V^{-1}. However, in silicon based JLTFETs with SiO_2 as gate dielectric material, the ratio is 35V^{-1}, which is less when compared to the proposed germanium based device. This implies that Ge-TMGAA-JLTFETs are profoundly insusceptible to Hot Carrier Effects (HCEs). Such a model with a high value of g_m/I_{ds} ratio is strongly desired for high-efficiency photovoltaic cell applications. Thus, the anticipated analytical results of the proposed model are validated against TCAD device simulation results.

The variation of transconductance-to-drain current ratio along the channel length is plotted for different values of High-K gate dielectric materials in Fig.3. As the channel length increases, g_m/I_{ds} ratio also increases. The term 'K' denotes the relative permittivity of the gate oxide material. Materials with high relative permittivity are useful in manufacturing high-value capacitors, high power RF transmitters and some electro-optical appliances. With higher relative permittivity of Titanium Oxide (TiO_2), the g_m/I_{ds} ratio is increased. The use of high-K gate dielectric material over conventional gate dielectric material (Silicon dioxide – SiO_2), has offered augmented carrier generation efficiency in the channel region. Thus, the projected model with germanium

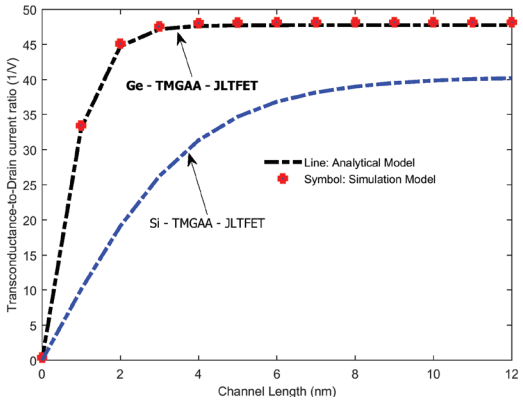

Figure 2: Transconductance-to-Drain Current ratio of Ge-TMGAA-JLTFET and Si-TMGAA-JLTFET with L=12nm, t_{ox}=2nm and t_{ge}=4nm.

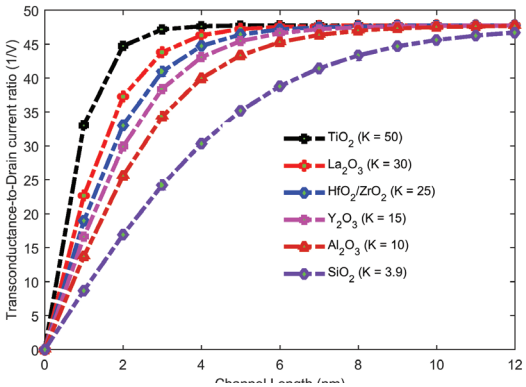

Figure 3: Plot of Transconductance-to-Drain Current ratio of Ge-TMGAA-JLTFET for different values of High-K gate dielectric materials.

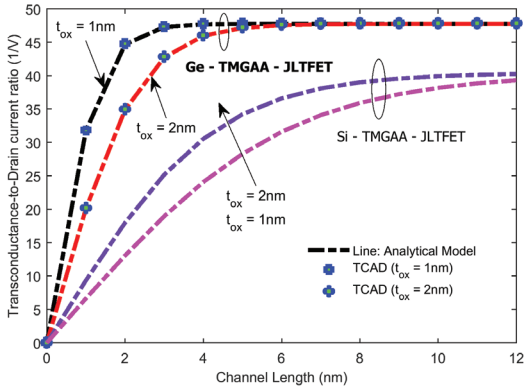

Figure 4: Variation of Transconductance-to-Drain Current ratio of Ge and Si based TMGAA-JLTFET for different values of gate oxide thickness.

and high-K gate dielectric material has significantly contributed to the performance of the device.

From Fig.2, we have noticed the combined supremacy of germanium and titanium oxide in proliferating the transconductance-to-drain current ratio. Here in Fig.4, also, it is clearly witnessed that the characteristics of the proposed device are better than in conventional Si-SiO_2 based devices. Fig.4. depicts the g_m/I_{ds} variation of Ge versus Si based TMGAA-JLTFET for various values of oxide thickness t_{ox}=1, 2nm. For thinner oxide thickness of t_{ox}=1nm, the g_m/I_{ds} ratio is high for both devices. But, the overall ratio is much higher for Ge-TMGAA-JLTFET, which again proves to be pertinent for high-efficiency, low power solar cell applications.

Fig.5. (a) illustrates the variation of subthreshold current for Ge and Si based TMGAA-JLTFET for various values of V_{ds}=0.3V and 0.4V. It is shown that in the proposed device the subthreshold leakage current is minimized when compared to Si-SiO_2 based junctionless TFETs. With Si-SiO_2 interface, several unwanted side effects can occur, remarkably the Hot Carrier Effect (HCE), which causes a displacement in the threshold voltage value and consequently leads to subthreshold leakage. For V_{ds}=0.3V, the subthreshold leakage is smaller compared to V_{ds}=0.4V. Also, when the gate voltage equals the drain voltage, the hot carrier injection is at maximum.

For higher drain voltages, the peak electric field will be at the drain end. The high electric field leads to avalanche multiplication of carriers. These carriers in turn gain high energy and become "Hot" electrons. The hot carriers can easily get trapped into the oxide layer and cause severe reliability issues. But with the incorporation of three different doping profiles in the gate region, the peak electric field at the drain side is suppressed effectively, shown in Fig.5.(b).

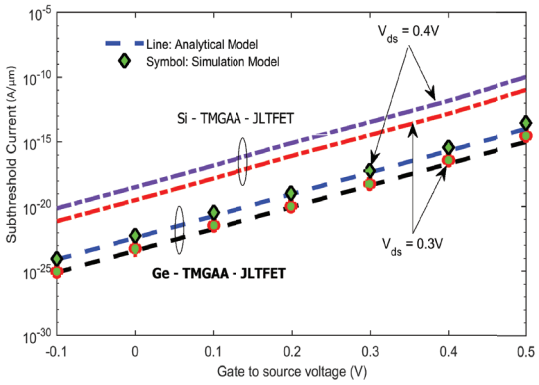

Figure 5.a: Variation of Subthreshold Current of Ge and Si based TMGAA-JLTFET for different values of drain-to-source voltage.

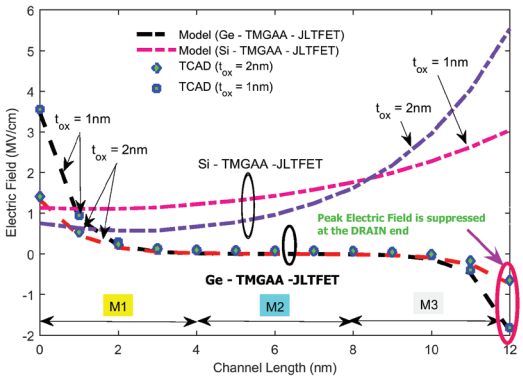

Figure 5.b: Electric Field variation of Ge and Si based TMGAA-JLTFET along the channel length for various values of oxide thickness.

Hot carrier damage may affect the endurance of non-volatile memory. Hot Carrier Effect (HCE) refers to device degradation or instability caused by hot carrier injection. This HCE being an important factor in the small-scale integrated circuits has to be reduced with-

out negotiating the advancements in device scaling. Hence, our proposed model (Ge-TMGAA-JLTFET) has overcome this hot carrier degradation with the usage of Titanium Oxide (TiO_2) as gate dielectric material. Fig.6. depicts the variation of subthreshold current for various channel lengths, L=15nm, 30nm and 45nm. Short channel (12nm) device using High-K dielectric material, offers improved hot carrier reliability, which is endorsed by minimum subthreshold leakage current of 10^{-25}A/μm near the subthreshold regime.

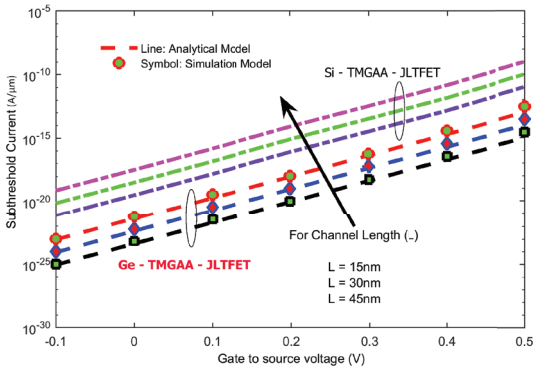

Figure 6: Subthreshold Current variation of Ge and Si based TMGAA-JLTFET for different channel lengths of L=15nm, 30nm and 45nm.

The plot of subthreshold swing along the channel length for various values of germanium thickness is shown in Fig.7. The proposed analytical model results are compared with Si based TMGAA-JLTFET and simulated using TCAD device simulator. It is inferred that the subthreshold swing has attained a minimum value of 35mV/dec, when compared to Si based JLTFETs having subthreshold swing less than 50mV/dec. With minimum germanium film thickness, the subthreshold degradation is also minimal.

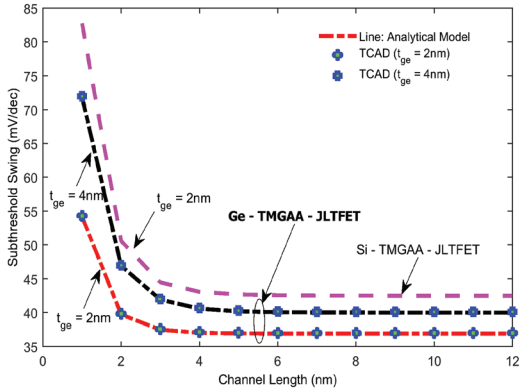

Figure 7: Dependence of Subthreshold Swing of Ge and Si based TMGAA-JLTFET along the channel lengths for various values of germanium thickness.

Fig.8. illustrates the dependence of subthreshold swing of Ge-TMGAA-JLTFET for various values of oxide thickness. As the oxide thickness is reduced from 3nm to 1nm, we witness that the subthreshold swing is also reduced to a greater extent. This demonstrates that, with thinner gate oxide, the electric field component can pervade the channel region more easily. Once the electric field components are strong enough, then the gate controlling capability is reinforced and subthreshold degradation in minimized. With lightly doped drain structure, the peak electric field at the drain end is suppressed and hence Drain Induced Barrier Lowering (DIBL) effect is also reduced tremendously.

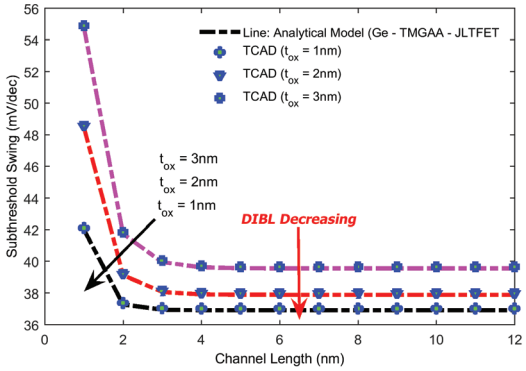

Figure 8: Plot of Subthreshold Swing of Ge-TMGAA-JLTFET along the channel lengths for various values of oxide thickness.

Fig.9. depicts the subthreshold swing of Ge-TMGAA-JLTFET for various values of doping concentration. For junctionless TFETs, the doping profile is uniform throughout the device. With higher doping concentration of $N_d=10^{20}cm^{-3}$, it is inferred that the subthreshold degradation is reduced.

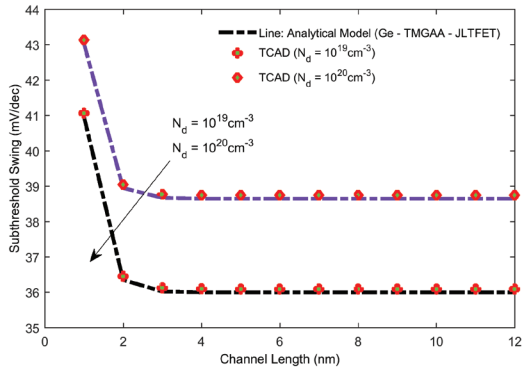

Figure 9: Subthreshold Swing of Ge-TMGAA-JLTFET along the channel lengths for various values of doping concentration.

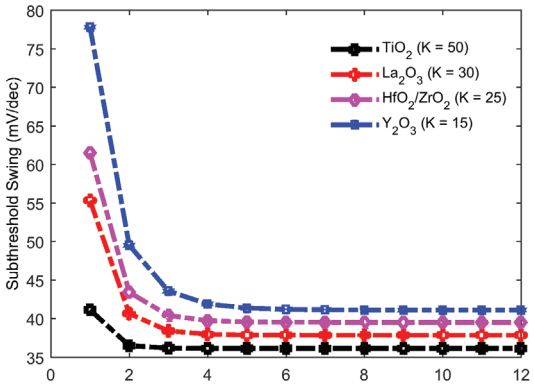

Figure 10: Plot of Subthreshold Swing of Ge-TMGAA-JLTFET along the channel lengths for different types of High-K gate dielectric materials.

The dependence of subthreshold swing of Ge-TMGAA-JLTFET for various types of High-K gate dielectric materials is shown in Fig.10. The subthreshold swing of the proposed model has been evaluated for various high-K gate dielectric materials such as Yttrium oxide, Hafnium/Zirconium oxide, Lanthanum oxide and Titanium oxide. The values of Transconductance-to-Drain Current ratio and Subthreshold Swing of Ge-TMGAA-JLTFET for different types of High-K gate dielectric material are listed in Table.1. The first row of Table.1 clearly indicates that, among different High-K materials, Titanium oxide offers less subthreshold swing and high g_m/I_{ds} ratio. It is visualized from Fig.10 that, Titanium oxide with higher dielectric constant, can hold large number of charge carriers and subthreshold degradation of the device is also reduced. The precise results of Ge and Si based TMGAA-JLTFET are listed in Table.2. The results suggest that the proposed model incorporated with Germanium, Titanium oxide and three different gate materials such as Gold, Molybdenum, and Titanium is a good solution and also as an excellent candidate for Improved Hot Carrier reliability.

4 Conclusions

In this paper, a subthreshold model of 12nm triple material gate-all-around junctionless tunnel FET with germanium and titanium oxide as high-K gate dielectric material is developed. The enhanced subthreshold characteristics of this novel device have been verified and validated by comparing the results with Si-SiO_2 based JLTFETs. Transconductance-to-Drain Current ratio, Subthreshold Current and Subthreshold Swing are derived analytically and simulated using the 2-D Sentaurus TCAD device simulator for various device parameters. Good agreement is obtained between our proposed analytical model and obtained simulation results. The results concede that Ge-TMGAA-JLTFET with TiO_2 exhibits improved hot carrier reliability with higher g_m/I_{ds} ratio, low leakage current and steep subthreshold swing. The proposed model proves to be an excellent device for high-efficiency photovoltaic cells, solar cell applications and solid-state LEDs.

5 References

1. S. E. Thompson and S. Parthasarathy, "Moore's law: the futureof Si microelectronics," *Materials Today*, vol. 9, no. 6, pp. 20–25, 2006

Table1: Transconductance-to-Drain Current ratio and Subthreshold Swing for Ge-TMGAA-JLTFET for different types of High-K gate dielectric material

High-K gate dielectric materials	Dielectric Constant (K)	Ge-TMGAA-JLTFET	
		Transconductance-to-Drain Current ratio (V^{-1})	Subthreshold Swing (mV/dec)
Titanium Oxide , TiO_2	50	49	35
Lanthanum Oxide, La_2O_3	30	45	39
Hafnium/Zirconium Oxide, HfO_2/ZrO_2	25	43	43
Yttrium Oxide, Y_2O_3	15	42	45

Table 2: Subthreshold parameters of Ge and Si-TMGAA-JLTFET with Titanium Oxide as gate dielectric material

Subthreshold Parameters	Device Type (L = 12nm)	
	Ge – TMGAA-JLTFET	Si – TMGAA-JLTFET
Transconductance-to-Drain Current Ratio	$49V^{-1}$	$39V^{-1}$
Subthreshold Current with Vgs = -0.1V	10 - 25A/μm	10 - 20A/μm
Subthreshold Swing	<35mV/dec	<50mV/dec

2. G. V. Reddy and M. J. Kumar, "A New Dual-Material Double-Gate (DMDG) Nanoscale SOI MOSFET-Two Dimensional Analytical Modeling and Simulation", *IEEE Transaction on Nanotechnology*, Vol. 4, pp.260-268, March 2005.
3. Z. Chen, Y. Xiao, M. Tang, Y. Xiong, J. Huang, J. Li, X. Gu, and Y. Zhou, "Surface-potential-based drain current model for long channel junctionless double gateMOSFETs", *IEEE Trans. Electron Devices,* vol. 59, no. 12, pp. 3292–3298, 2012.
4. R. K. Baruah, and R. P. Paily, "A dual-material gate junctionless transistor with high- k spacer for enhanced analog performance", *IEEE Trans. Electron Devices*, vol. 61, no. 1, pp. 123-128, 2014.
5. W. Long, H. Ou, J. M. Kuo, and K. K. Chin, "Dual material gate (DMG) field effect transistor", *IEEE Trans. Electron Devices*, vol. 46, pp. 865-870, 1999.
6. A. K. Agrawal, P. N. V. R. Koutilya, and M. J. Kumar, "A pseudo 2-D surface potential model of a dual material double gate junctionless field effect transistor", *J. Comput. Electron.,* vol. 14, no. 3, pp. 686-693, Sep. 2015.
7. M. J. Kumar, and A. Chaudhary, "Two-dimensional analytical modeling of fully depleted DMGSOI-MOSFET and evidence for diminished SCEs", *IEEE Trans. Electron Devices,* vol. 51, no. 4, pp. 569-574, 2004.
8. T. Skotnicki, C. Fenouillet-Beranger, C. Gallon et al., "Innovative materials, devices, and CMOS technologies for low-power mobile multimedia," *IEEE Trans. on Electron Devices,* vol. 55, no. 1, pp. 96–130, 2008.
9. J. Robertson, "High dielectric constant oxides", *Eur. Phys. J. Appl. Phys.*, vol. 28, pp. 265–291, 2004.
10. E. H. Toh, G. H. Wang, L. Chan, et al., "Device design and scalability of a double-gate tunnelling field-effect transistor with silicon–germanium source", *Japanese Journal of Applied Physics,* vol. 47, no. 4, 2008.
11. S. H. Kim, H. Kam, C. Hu, et al., "Germanium-source tunnel field effect transistors with record high I_{ON}/I_{OFF}", *IEEE VLSI Symp on VLSI Technology*, 2009.
12. K. Boucart, and A. Ioneacu, "Double gate tunnel FETs with high-k gate dielectric", *IEEE Trans. on Electron Devices*, vol. 54, no. 7, pp. 1725-1733, July 2007.
13. C. Ren, H. Y. Yu, J. F. Kang, X. P. Wang, H. H. H. Ma, Yee-Chia Yeo, D. S. H. Chan, M. -F. Li, and D. L. Kwong, "A dual-metal gate integration process for CMOS with sub-1-nm EOT HfO_2 by using HfN replacement gate", *IEEE Electron Device Lett.*, vol. 25, no. 8, pp. 580-582, 2004.
14. M. A. Abdi, F. Djeffal, Z. Dibi, and D. Arar, "A two-dimensional analytical subthreshold behavior analysis including hot-carrier effect for nanoscale Gate Stack Gate All Around (GASGAA) MOSFETs," *J. Comput. Electron.*, vol. 10, no. 1-2, pp. 179–185, June 2011.
15. T. K. Chiang, "A new compact subthreshold behavior model for Dual- Material Surrounding Gate (DMSG) MOSFETs," *Solid State Electron.*, vol. 53, no. 5, pp. 490–496, May 2009.
16. V. Kilchytska, A. Neve, L. Vancaillie, D. Levacq, S. Adriaensen, H. van Meer, K. D. Meyer, C. Raynaud, M. Dehan, J. P. Raskin, and D. Flandre, "Influence of device engineering on the analog and RF performances of SOI MOSFETs," *IEEE Trans. Electron Devices*, vol. 50, no. 3, pp. 577–588, Mar. 2003.
17. Y. Pratap, P. Ghosh, S. Haldar, R. S. Gupta, and M. Gupta, "An analytical subthreshold current modeling of cylindrical gate all around (CGAA) MOSFET incorporating the influence of device design engineering", *Microelectronics J.*, vol. 45, no. 4, pp. 408–415, 2014.
18. P. Suveetha Dhanaselvam, N. B. Balamurugan, and V. N. Ramakrishnan,"A 2D Transconductance and Sub-threshold behavior model for triple material surrounding gate (TMSG) MOSFETs", *Microelectronics J.,* vol. 44, no. 12, pp. 1159–1164, 2013.
19. R. Gautam, M. Saxena, R. S. Gupta, and M. Gupta, "Gate all around MOSFET with vacuum gate dielectric for improved hot carrier reliability and RF performance", *Electron Devices, IEEE Trans.*, vol. 60, no. 6, pp. 1820–1827, 2013.
20. T.-K. Chiang and J. J. Liou, "An analytical subthreshold current/swing model for junctionless cylindrical nanowire FETs (JLCNFETs) ", *Facta Universitatis Series: Electronics and Energetics*, vol. 26, no. 3, pp. 157–173, 2013.
21. S. Theodore Chandra, Dr. N. B. Balamurugan, G. Lakshmi Priya and S. Manikandan, "Subthreshold behavior of AlInSb/InSb high electron mobility transistors", *Chin. Phys. B,* vol.24, No. 7, pp. 076105-076105-5, 2015.
22. P. Vanitha, N. B. Balamurugan and G. Lakshmi Priya, "Triple material surrounding gate nanoscale tunnel FET - analytical model and simulation", *Journal of Semiconductor Technology and Science*, vol. 15, no. 6, pp.585-591, Dec. 2015.
23. A. Kranti, Rashmi, S. Haldar, and R. S. Gupta,"Design and optimization of vertical surrounding gate MOSFETs for enhanced transconductance-to-current ratio (g_m/I_{ds})", *Solid State Electron.*, vol. 47, pp. 153–159, May 2003.
24. P. K. Tiwari, S. Dubey, K. Singh, and S. Jit, "Analytical modeling of subthreshold current and subthreshold swing of short-channel triple-material double-gate (TM – DG) MOSFETs", *Superlattices and Microstructures*, vol. 51, pp. 715 – 724, 2012.

Arrived: 16. 10. 2017
Accepted: 27. 03. 2018