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Modelling Overvoltage Protection Components: Verilog Simulations of Combined MOV and GDT Arresters

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Abstract: Overvoltage protection systems are used to protect sensitive electrical and electronic equipment from voltage surges and lightning strikes. These systems are mostly based on the use of gas discharge tubes (GDTs) and metal-oxide varistors (MOVs), which are utilised individually or in various combinations. Adequate computer simulations play an important step in the process of designing overvoltage protection systems and selecting adequate parameters. In this paper, the modelling of low-voltage GDT and MOV components is performed using the Verilog-A hardware description language. The presented models are designed for integration with other overvoltage protection system components to form an integrated overvoltage protection system. The current–voltage characteristics of the GDTs and MOVs are highly nonlinear and frequency dependent. The developed Verilog-A mixed behavioural and structural models of GDTs and MOVs ensure a stable convergence of numerical processes during the simulations of circuits with these elements. The simulations of overvoltage protection systems were completed using a TINA circuit simulator. Two laboratory tests were performed using GDT and MOV components. In the first test, the time responses of the current and voltage on a GDT and MOV serial connection were measured in the laboratory. In the second test, the response of the GDT and MOV serial connection was tested in a power line network environment, where a surge current impulse and power line voltage of 400 V peak and frequency of 50 Hz existed simultaneously. The dynamic response of the GDT and MOV serial connection obtained through the simulations agrees well with the measurement results.

Keywords: Verilog; modelling; gas discharge tubes; metal-oxide varistor; overvoltage protection.

Modeliranje komponent prenapetostne zaščite: Simulacija serijske vezave prenapetostnih odvodnikov MOV in GDT v jeziku Verilog

Izvleček: Sistemi prenapetostne zaščite se uporabljajo za zaščito občutljive električne in elektronske opreme pred prenapetostjo in udari strele. Običajno so ti sistemi zasnovani na plinskih odvodnikih prenapetosti (GDT) in metal-oksidnih varistorjih (MOV), ki se uporabljajo posamezno ali v različnih vezavah. Računalniške simulacije predstavljajo pomemben korak pri načrtovanju sistemov prenapetostne zaščite in izbiri ustreznih parametrov. V tem članku predstavimo modeliranje nizkonapetostnih komponent GDT in MOV v jeziku Verilog-A. Predstavljeni modeli so namenjeni integraciji z drugimi komponentami, ki tvorijo integriran sistem prenapetostne zaščite. Tokovno- napetostne karakteristike GDT in MOV so močno nelinearne in frekvenčno odvisne. Razviti modeli GDT in MOV v jeziku Verilog-A uporabljajo opis obnašanja in strukturni opis, kar zagotavlja stabilno konvergenco numeričnih procesov. Simulacije sistemov prenapetostne zaščite so potekale z uporabo simulatorja TINA. V praktičnem delu smo izvedli dva laboratorijska testa. V prvem testu so bili v laboratoriju izmerjeni časovni odzivi toka in napetosti na serijski vezavi GDT in MOV. V drugem testu smo preizkusili odziv serijske vezave GDT in MOV ob hkratni prisotnosti impulza prenapetostnega toka in omrežne napetosti amplitude 400 V in frekvence 50 Hz. Dinamični odziv serijske vezave GDT in MOV, pridobljen s simulacijami, se dobro ujema z rezultati meritev.

Ključne besede: Verilog; modeliranje; plinski odvodnik prenapetosti; metal oksidni varistor; prenapetostna zaščita.

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1 Introduction

Overvoltage protection components have become an inevitable part of the devices aimed to protect sensitive equipment against overvoltage surges caused by atmospheric discharges and transients in power networks. An overvoltage protection system must be designed to capture the atmospheric discharge to a preferred point, conveying the energy into the ground and protecting all incoming power and communication lines using surge protection devices (SPDs).

SPDs must discharge high-magnitude impulse currents and limit the overvoltage levels [1, 2]. SPDs are primarily based on metal-oxide varistors (MOVs) and gas discharge tubes (GDTs), which are used individually or in serial combinations.

Overvoltage protection components can be divided into voltage switching and voltage limiting components [1]. Voltage switching components operate by switching from a high to low resistance state at certain breakdown voltages and behave as a short circuit. GDTs operate in accordance with this principle. The components in the second group limit a transient overvoltage impulse to a predefined voltage level. MOVs belong to this set of overvoltage components.

Modelling and simulation can significantly facilitate the process of designing overvoltage protection systems. Typically, simulations are based on models of the individual components comprising the overvoltage protection system, commonly described with mathematical expressions.

The modelling and simulation process is more complex when some of the components have nonlinear characteristics and states that vary depending on excitation input values. In addition, the models need to be developed in a form that allows their integration with the existing components within the electronic simulation program.

MOVs and GDTs have highly non-linear current–voltage characteristics [1–4]. The simulation of a system with these components can lead to non-convergent numerical calculations [5], which is especially critical during the transition of individual components from one state to another.

The simulation of overvoltage protection systems is mostly based on SPICE models and implemented using SPICE-based simulation tools [5]. Using intrinsic components as the basic building blocks for a larger model, designers can define new SPICE models. SPICE accepts netlists as a text description of a circuit that is comprised of interconnected basic components [6]. The models of these basic components are provided within the simulator.

The existing GDT models available in the literature are largely SPICE based, in the form of structured netlists composed of basic components [7–9]. The solution presented in [7] uses controlled switches and diodes with specified breakdown voltages. The model in [8] is created with transistors, providing theoretical triac voltage–current characteristics. Conversely, the GDT models in [10–12] are based on mathematical descriptions of basic operational principles developed for the Matlab/Simulink environment.

Several MOV models have been proposed in the literature [5, 12–17], aiming to properly represent MOV's nonlinear characteristics and frequency dependence behaviour. The IEEE W.G. 3.4.11 proposed a frequency-dependent model with two nonlinear resistors [14], which was further simplified by [15], preserving its basic principle. In [16], the authors neglected the first inductance in the IEEE model as well as the simplified parameter determination procedure [16]. The MOV model presented in [12] was developed in the Matlab/Simulink environment for simulations of transients in low voltage power-lines. A review of the existing models and their implementation for transient behaviour of electrical circuits is presented in [13].

Verilog-A, a subset of Verilog-AMS, has emerged as a standard language for the development of compact models of circuit components based on mathematical descriptions of the electrical behaviour of individual components [18]. This language allows the description and simulation of components and circuits at a higher level of abstraction [18, 19]. The compact models were originally coded in FORTRAN or C, with relatively complex codes [18]. The compact models should be sufficiently simple to be easily developed and incorporated in circuit simulators. Verilog-A, as a hardware design language (HDL) for analog circuits and system design, uses a text-file code to describe the mathematical models [19, 20]. The Verilog-A code is converted into low-level C language by a code generator [19]. The generated C code is then directly compiled into the simulator, resulting in an equivalent SPICE model. In this way, it is possible to simulate electronic circuits that include both Verilog and SPICE models. TINA supports simulations including Spice netlists along with components modelled in Verilog, Verilog-A and Verilog-AMS [21].

The presented MOV and GDT Verilog-A models are based on mathematical descriptions of the transfer function in the MOV modelling and transition between states during the GDT modelling. The developed mod-

els ensure a stable convergence of numerical process during simulations of circuits with these elements.

Verilog-A models of MOV and GDT are used to simulate a serial connection of these components. Using such a serial connection reduces some of the shortcomings that arise when using these components individually, especially in the first stage of overvoltage protection systems. For example, high GDT resistance eliminates leakage currents in MOVs. On the other hand, the use of MOVs in serial connections resolves fast surge discharges, as GDTs have a much longer response. The performed simulations demonstrated that the developed models ensure stable convergence of the numerical processes.

The validation of the developed models was performed by comparing the simulation results with the measurement results of the residual voltage measured on the GDT and MOV serial connection. In the laboratory, waveforms of residual voltage under surge currents of 40 kA (10/350 μs) and 20 kA (10/700 μs) were measured. The results obtained by performing simulations with the TINA program tool were verified by laboratory tests. In the first scenario, the residual voltage at the GDT and MOV serial connection ports were measured after stress with the current pulse shape. In the second scenario, the overvoltage protection was focused on measurement of voltage waveform at the terminals of the MOV and GDT serial connection when a surge impulse and power line voltage of 50 Hz existed simultaneously. The second scenario corresponds to a real application of an overvoltage protection device.

The rest of this paper is structured as follows: Section II describes the basic operational principles of GDTs and MOVs and appropriate current/voltage characteristics. Verilog-A GDT and MOV models (presented with simplified pseudo codes) are developed using the TINA circuit simulator and described in Section III. Section IV presents the results of the measurements and numerical simulations for two overvoltage protection system scenarios. Conclusions and recommendations for future research are given in the last section of the paper.

2 Overvoltage Protection Components

A basic description of the GDT and MOV components is given in this section to simplify the presentation of the developed models described in the next section.

GDTs consist of two or more metal electrodes separated by a small gap filled with a gas insulation medium and held by a ceramic or glass cylinder [1–3]. During normal operation at nominal voltage, GDTs behave as an insulator.

GDTs dissipate voltage transients through a contained plasma gas when an overvoltage pulse reaches the spark-over (breakdown) voltage (Fig. 1). The spark-over voltage is not constant but rather depends on the rate of rise of the surge voltage. As the voltage increases across the GDT, the gas in the tube starts ionising due to the charge developed across it [1-3]. In this region, known as the *glow region* with voltage U_{glow}, the increasing current flow generates an avalanche effect, transitioning the GDT into a virtual short. This is the arc burning phase. The glow region is shown in Fig. 1. During the short-circuit event, the voltage developed across the device is known as the arc voltage, U_{arc}. This region is known as the *arc region* (Fig. 1). The transition time between the glow and arc regions is dependent on the physical characteristics of the GDT [3]. In the arc region, the GDT diverts the transient current away from the protected device. During the extinguishing process, the transition from the arc to glow regions may be at a lower current than during the transition from the glow to arc regions (dashed line in Fig. 1.).

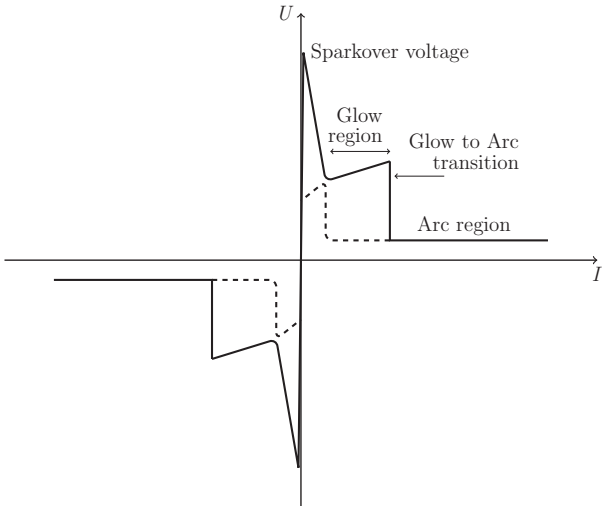

Figure 1: GDT *U-I* characteristics

GDT components have high insulation resistance and low capacitance. When a voltage applied to the GDT electrodes is below its spark-over voltage, the leakage current through the arrester is close to zero. A low leakage current ensures minimal influence on the normal operation of the equipment.

MOVs are resistors with a nonlinear *U-I* characteristic (Fig. 2.). Unlike GDTs, these elements do not cause short-circuits in the power supply network. MOVs are produced of a ceramic material obtained by mixing zinc oxide (ZnO) with a small amount of additives. The

ZnO grains have low resistance and are surrounded by granular layers of additives with high resistance [1]. This structure behaves like diodes connected in series/parallel, ensuring that the MOV has nonlinear characteristics.

When a low voltage is applied to the MOV electrodes, the diodes are not conductive and the MOV behaves as an insulator. After the electric field reaches a value above 100 kV/mm, the current starts to flow and varies from 1 mA to 1 kA. With a high electric field, the voltage drop in the MOV is linear since it is determined by the voltage drop in the ZnO grain resistance [1]. The voltage drop at the barrier can be neglected due to the tunnel effect. This part of the *U-I* characteristic is linear.

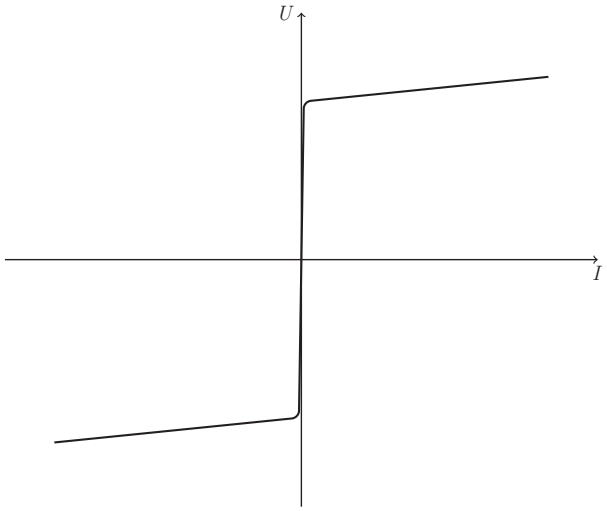

Figure 2: MOV *U-I* characteristics

The ability of components to withstand high-energy pulses is measured by the different pulse shapes (8/20 µs, 10/350 µs, 10/700 µs, and 1.2/50 µs) and amplitudes.

3 Verilog-A Models of Overvoltage Protection Components

The Verilog-A hardware description language is accepted for the modelling of electronic components and circuits due to its simplicity and flexibility when writing model code. The descriptions of the developed models of overvoltage components are based on pseudo code. For presentation purposes in this text, some blocks of the code are represented with mathematical equations.

GDTs can be in three different states, as described in the previous section [1, 7, 9]. A simplified GDT model can be presented as a symmetrical low-capacitance voltage and current controlled switch, whose resistance may instantly change from several GΩ during normal operation to values less than 1 Ω after ignition caused by a surge voltage. The transition from an open to closed switch includes an ionising state, and the GDT model must include these three states. The Verilog-A GDT model presented in this paper includes these three states, defined in accordance with the characteristic shown in Fig. 1.

The modelling of the GDT transition in SPICE is implemented with voltage and current control switches. The required voltage levels are ensured by diodes with the specified breakdown voltages [7]. The model presented in [8] does not include switches. The transition from a high-value impedance state to a very low impedance state in [8] is solved using bipolar transistors connected to provide theoretical triac behaviour of the GDT model as a whole.

The Verilog-A module may contain equations for behavioural modelling and instantiations of other modules such as structural modelling. The behavioural models define the relationships between the outputs and inputs, and they contain procedural statements that control the simulation and manipulation of the variables of the defined data types. The behavioural models are more abstract, and the focus is on the functionality of the design. Structural modelling defines the system in terms of basic components and their interconnections, describing the interconnection between the predefined components in the model. The model in Verilog-A is defined with the nodes and branches, so the behaviour of each branch must be specified.

The simplified pseudo-Verilog-A code of the proposed GDT model is shown in Fig. 3. The first line, *discipline.va*, provides common definitions that are used to specify the type of a continuous wire. The *discipline* includes a collection of related natures as physical signal types. Electrical discipline, used in our models, consists of voltages and currents. The second line defines the name of the component, in this case *GDT*, and the input/output nodes. The nodes *a* and *c* are declared as *inout* ports and presented with *electrical* discipline. The *a* and *c* pins are nodes that the GDT shares with the rest of the circuit (line 3). The pins are then declared as being electrical, meaning that the potential of each pin is a voltage and the flow into the pin is a current. The parameters, defined below, are treated as constants within the module and cannot be changed from within the module (lines 5 to 12). In Verilog-A, the description of the model is given as an analog process, which is denoted with the keyword *analog* in line 13.

The initial values and state of GDT is defined in (Fig. 3, line 14). The capacity *C* of GDT shows the behaviour at

nonconductive state, and is modelled using *ddt* function in line 16. The charge is first calculated in line 15 [18]. The construction of GDT is such that it has very low capacitance *C*. This allows GDT usage in high-frequency circuit applications protecting communication and data lines from overvoltage.

The inductance *L* takes into account dynamic response. If the voltage at GDT terminals has low rate of rise, the spark-over voltage will be determined by electrode spacing, the gas type and pressure, and pre-ionization of the enclosed noble gas [3]. When the overvoltage pulse has fast rate of rise the spark-over voltage of GDT will be increased. This is caused by the finite time necessary for the gas to ionize. The estimation of spark-over voltage is based on measured voltage levels for different values of rate of rise and provided by manufacturers of GDT components. The estimation of spark-over voltage is listed in lines 20 and 21.

GDT stressed by overvoltage impulse can be in previously described three states. The Verilog-A model of GDT, including descriptions of three states, can be simplified by using an 'IF THEN ELSE' conditional statement. From the current-voltage characteristic curve shown in Fig. 1, it is clear that the GDT has bi-directional symmetrical characteristics. The GDT can operate or function in either direction or overvoltage pulse polarity, and the GDT model must take this property into account.

When the voltage at the GDT terminals is greater than the spark-over voltage, the GDT goes into an ON state (line 23). After ignition, the voltage drops from the spark-over voltage to the glow voltage level. This transition can lead to a loss of convergence during the process of solving the voltage and current waveforms. In order to avoid this loss of convergence, the transition from the high resistance state to the glow region is modelled using the transition function (line 30):

$$u(t) = \left(U_p - U_{glow}\right) e^{-\frac{t-t_1}{10^{-8}}} + U_{glow} \quad (1)$$

where *u(t)* is the voltage at the GDT terminals, U_p is the spark-over voltage, U_{glow} is the voltage in the glow region and t_1 is the time at the moment when the overvoltage pulse reaches the spark-over voltage. The voltage in the glow region is represented by U_{glow}.

A similar transition exists when the GDT switches from the glow to arc regions. This transition can also lead to a loss of convergence. Hence, the transition from the glow to arc regions is modelled using the following equation:

$$u(t) = \left(U_{glow} - U_{arc}\right) \tau^{I_{glow} - I_{arc}} + U_{arc} \quad (2)$$

where U_{arc} is the voltage in the arc region, I_{glow} is the current in the glow region before transition and I_{arc} is the current in the arc region after transition. This transition is presented on line 33 in Fig. 3.

Using the two previously described functions, a smooth transition from one state to another is provided, and the standard use of switches in the GDT model is avoided. The resistance of the GDT in normal operation is R_{OFF} and is calculated in line 42. The calculated voltage *U*, using the contribution operator (<+) in line 44, determines the value of the potential between the *n* and *c* nodes *V(n,c)*.

MOVs are voltage-dependent resistors with a highly non-linear voltage-current relation, and they have different delays in the conduction mechanism at different surge current wavefronts. The IEEE model is the most used model in the literature for transient analysis of varistors. The Verilog-A model of MOV, presented in this paper, is based on the IEEE model. The model is frequency dependent and is suitable for the numerical simulation of fast transients [4, 5]. The simplified pseudo-Verilog-A code of the MOV model is shown in Fig. 4.

The non-linear voltage-current relation is represented by two non-linear branches separated by an *R*, *L* filter. This filter has an important role in taking into account different delays in the conduction mechanism at different surge current wavefronts [4, 5, 16].

The first line in Fig. 4 defines the *discipline* required for analog simulations. The second line lists the module name of the component, in this case *MOV*, and the list or node names (*p* and *n*). The port direction (line 3) and port and node types (line 4) are then declared. The parameters provide a way to pass values into the module at the time of instantiation. The parameters of the MOV model were computed using the procedure given in [14, 15]. The analog block describes the MOV model and includes lines from 18 to 45.

The series inductance is first introduced (line 20). The *L1* represents the inductance of the current path through the arrester. The resistance *R1* in line 21 provides convergence in the numerical simulations. These two components (*R1* and *L1*) also represent the input filter of the model.

The first and second nonlinear elements are modelled with the following expression [17]:

$$U = U_n k b^I I^c \quad (3)$$

where *U* is voltage across the varistor, *Un* clamping voltage and *I* is the current through the varistor. The

coefficients *k*, *b*, and *c* are obtained from fitting of the curves proposed by the IEEE Working Group. The first nonlinear element is listed in lines 22 to 30. The nonlinear *VI* characteristic is divided in three regions. The code of second nonlinear branch is listed in lines 36 to 44. The nonlinear elements are divided by the *R-L* filter (lines 34 and 35). The MOV capacitance *C* is presented in line 32.

MOV and GDT components are described using the module in Verilog-A [19]. These two components are then combined as a GDT and MOV serial connection (Fig. 5). The GDTMOV model uses previously presented

```
1: 'include "disciplines.va"
2: module GDT(a, c);
3: inout a, c;
4: electrical a, c, n;
5: parameter real Cgap = 0.5e-12;
6: parameter real Riso = 1.0e9;
7: parameter real L =1.0e-9;
8: parameter real Uglow=150.0;
9: parameter real Uarc=40.0;
10: parameter real tau=0.01;
11: parameter real Iarc=9.0;
12: parameter real Imin=90.0e-3;
13: analog begin
14: Initialize basic values and state of GDT
15: q=Cgap*V(a,c);
16: I(a,c) <+ ddt(q);
17: V(a,n) <+ L*ddt(I(a,n));
18: I(a,n) <+ V(a,n)/Rp;
19: Estimation of sparkover voltage U_p
20: absslope=abs(ddt(V(a,c))*1e-6);
21: U_p < +table_model(absslope,"table_slope.tbl","L");
22: if U > U_p then
23:     GDT goes into ON state
24:     define time t_1
25: else
26:     GDT remains in OFF state
27: end if
28: if GDT is in ON state then
29:     if I < I_arc then
30:         U = (U_p - U_glow)e^(-(t-t1)/10^-8) + U_glow
31:     else
32:         if I > I_arc + ΔI then
33:             U = (U_glow - U_arc)τ^(I-I_arc) + U_arc
34:         else
35:             U = U_arc
36:             if I < I_min then
37:                 GDT goes into OFF state
38:             end if
39:         end if
40:     end if
41: else
42:     U = I · R_OFF
43: end if
44: V(n,c)<+U;
45: end
46: endmodule
```

Figure 3: The pseudo Verilog-A code of the GDT model

models (Fig. 3, Fig. 4) of the *GDT* and *MOV*, which are included in the code (lines 10 to 13). In line 14, the module starts with the name of the model and the input and output nodes. Next, the direction of two *electrical* nodes are defined: *p* and *n* (line 16). Internal node *i1* is defined as *electrical*. The nodes are used as interconnection points for ports.

```
1: 'include "disciplines.va"
2: module MOV (p, n);
3: inout p, n;
4: electrical p, n, n1, n2;
5: parameter real L1 = 0.6e-9;
6: parameter real L2 = 45e-9;
7: parameter real R1 = 0.3;
8: parameter real R2 = 0.195;
9: parameter real k1 = 1.2968167;
10: parameter real k2 = 0.9713959;
11: parameter real b1 = 1.000005;
12: parameter real b2 = 1.000004;
13: parameter real c1 = 0.0376332;
14: parameter real c2 = 0.0510025;
15: parameter real Imin=1e-5;
16: parameter real Un=450.0;
17: parameter real C = 0.3e-12;
18: analog begin
19: // The first RL filter
20: V(p,n1) <+ L1 * ddt(I(p,n1));
21: V(p,n1) <+ I(p,n1) * R1;
22: // Te first nonlinear branch
23: i_1 = I(n1, n);
24: if i_1 > I_min then
25:     U_1 = U_n · k_1 · b_1^(i_1) · i_1^(c_1)
26: else
27:     R_L = U_n · k_1 · b_1^(I_min) · I_min^(c_1)/I_min;
28:     U_1 = R_L * i_1;
29: end if
30: V(mid1, n) <+ U_1;
31: // Varistor capacity
32: I(n1, n) <+ C * ddt(V(n1, n));
33: // The second RL filter
34: V(n1,n2) <+ L2 * ddt(I(n1,2));
35: V(n1, n2) <+ I(n1, n2) * R2;
36: // The second nonlinear branch
37: i_2 = I(n2, n);
38: if i_2 > I_min then
39:     U_2 = U_n · k_2 · b_2^(i_2) · i_2^(c_2)
40: else
41:     R_L = U_n · k_2 · b_2^(I_min) · I_min^(c_2)/I_min;
42:     U_2 = R_L * i_2;
43: end if
44: V(n2, n) <+ U_2;
45: end
46: endmodule
```

Figure 4: The pseudo Verilog-A code of MOV model

The GDTMOV model itself is constructed by creating instances of predefined GDT and MOV modules, wiring them together by connecting them to nodes and then specifying parameters for them. This is done for the GDT model (line 18) and the MOV model (line 19).

The statement in line 18 directs that an instance of the module *GDT* be connected to nodes *p* and *i1* and be named *GDT1*. The parameters of *GDT* are defined in the GDT module and are not stated here. The second statement (line 19) directs that an instance of *MOV* be named *MOV1* and connect to *i1* and *n*. The module terminates with the *endmodule* statement.

```
1:  ////////////////////////////////
2:  //TINA HDL Macro Description Begin
3:  //entity_name:GDTMOV;
4:  //arch_name:ignored;
5:  //ports:p,n;;
6:  //Mode:VerilogAMSTyp;
7:  //TINA HDL Macro Description End
8:  ////////////////////////////////
9:  ‘include "disciplines.va"
10: module GDT(a, c);
11: The code of GDT from Fig. 3.
12: module MOV (p, n);
13: The code of MOV from Fig. 4.
14: module GDTMOV (p, n);
15: inout p, n;
16: electrical p, n;
17: electrical i1;
18: GDT #( ) GDT1( .a(p), .c(i1) );
19: MOV #( ) MOV1( .p(i1), .n(n) );
20: endmodule
```

Figure 5: The pseudo Verilog-A code of GDT and MOV in serial connection

The parameters of the GDT and MOV models are adapted to the components used in the experimental tests. These parameters are based on data provided by the producers of the overvoltage components.

4 Numerical Simulations and Measurements

The validation of the developed GDT and MOV models is based on comparisons of the residual voltages obtained using numerical simulations and experimental tests when the MOV and GDT serial connection is stressed with a current pulse of a given shape and amplitude. The model of the MOV and GDT serial connection, developed in Verilog-A, is simulated using the TINA circuit simulator.

In the first scenario, the residual voltage at the GDT and MOV serial connection ports is measured after stress with a 10/350 µs current pulse shape with an amplitude of 40 kA. The measurement setup of the first test system is presented in Fig. 6. For this measurement, a surge generator (TUG-200 generating an impulse of direct atmospheric discharge 10/350 µs short circuit), a digital scope Tektronix (100 MHz, 1 GSample/s), and a Pearson current monitor model 1423 were used. The test system from Fig. 6 is simulated in the TINA software tool. The scheme of the circuit with the GDT and MOV serial connection as an integrated component modelled in Verilog-A is presented in Fig. 7. The 10/350 µs current pulse is modelled using the piecewise linear signal definition as a set of *Time/Value pairs*.

The residual voltage is measured at the terminals of the MOV and GDT serial connection and presented in Fig. 8. The residual voltage waveform obtained by the simulation is presented in Fig. 9. The time response of the GDTs and MOVs depends on the rate of rise and the magnitude of the surge pulses [3–5].

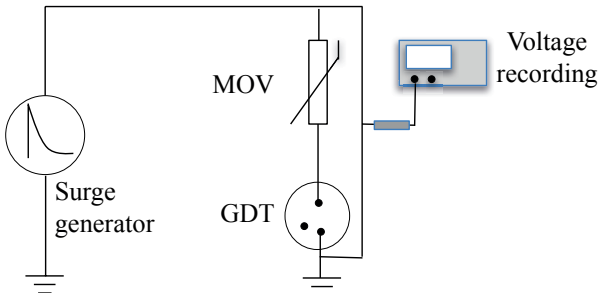

Figure 6: Measurement setup of the GDT and MOV in serial connection (surge current shape is 10/350 µs and the amplitude is 40 kA)

GDTs provide insulation between the protected lines and the ground potential during normal operation. High GDT resistance eliminates the leakage current that occurs when MOV-based surge devices are used. GDTs are also characterised by a high surge current discharge capacity, which can take more than ten thousand amperes (8/20 µs). However, GDTs have a slightly slower response compared to MOVs. The voltage drop in GDTs remains constant and low regardless of the surge current and behaves as a low impedance switch.

MOVs can also be used to meet the requirements of lightning protection class I with low protection levels due to high-performance varistor ceramics and the ability to discharge high surge pulses in acceptable installation spaces. The fast response time of MOVs (nanosecond range) makes them suitable for limiting even particularly dynamic surge voltage phenomena.

In normal operation, GDTs cut off leakage currents. During the surge pulse, the GDT and MOV serial connection effectively discharges the transients to ground and limits the voltage below the dielectric strength of the end device. The typical dielectric strength value of end devices is about 1.5 kV.

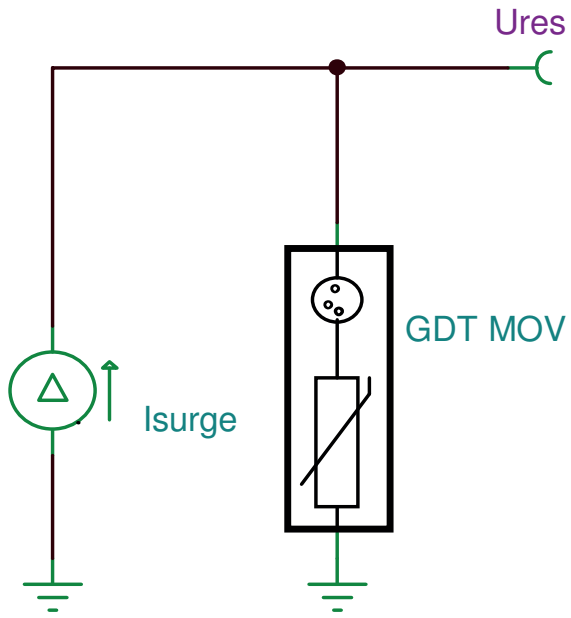

Figure 7: The circuit for numerical simulation of the MOV and GDT in serial connection

The serial connection of GDTs and MOVs takes advantage of both technologies and eliminates certain deficiencies of the single components. GDTs and MOVs together provide faster response and require lower capacitance when power lines are used as communication media. The MOV in this configuration eliminates follow-on currents and allows the GDT arc to be extinguished. The follow-on current is supplied by the electrical power system and flows through the GDT after the discharge current impulse disappears.

The residual voltage at the GDT and MOV terminals (Fig. 6) is observed by a digital oscilloscope and presented in Fig. 8. The residual voltage obtained by measurements is 940 V. Equal values for residual voltage and a

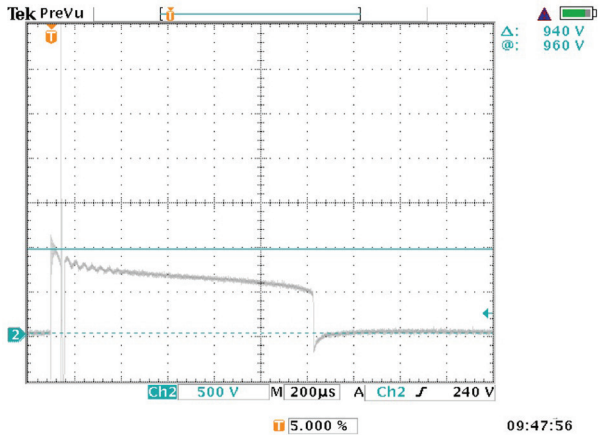

Figure 8: The residual voltage measured using the measurement setup presented in Fig. 6

similar waveform of voltage at the GDT–MOV terminals is obtained by numerical simulation (Fig. 9).

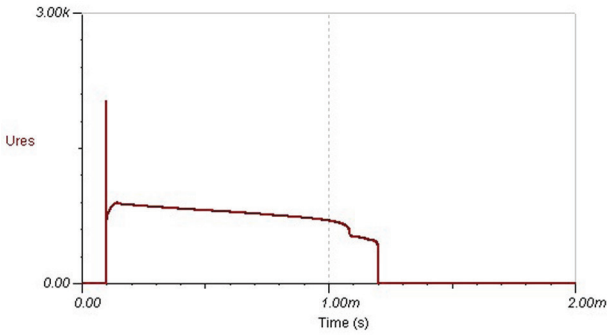

Figure 9: The waveform of the residual voltage obtained by simulation in TINA

The second case of the overvoltage protection laboratory tests and simulations is focused on the measurement of the voltage waveform at the terminals of the MOV and GDT serial connection when the surge impulse (10/700 µs surge pulse shape) and a power line voltage of 50 *Hz* exist simultaneously. The surge impulse appears on the LV network during its operation. In the laboratory measurements and in the numerical simulations, it is assumed that a surge wave appears at a certain moment on an energised LV conductor. The SPD device is connected to a phase conductor, and phase voltage exists during the measurements and numerical simulations.

A schematic representation of the measurement setup is presented in Fig. 10. Measurement equipment consists of: a surge generator TUG-200 (generating an impulse of direct atmospheric discharge 10/700 µs short circuit), an auto-transformer for the power line voltage, an oscilloscope LeCroy (350 MHz, 2,5 GSample/s), a digital scope Tektronix (100 MHz, 1 GSample/s), and a Pearson current monitor model 1423. The currents are measured in the MOV and GDT branch and the power line branch. The voltage drop at the terminals of the GDT and MOV serial connection is also measured.

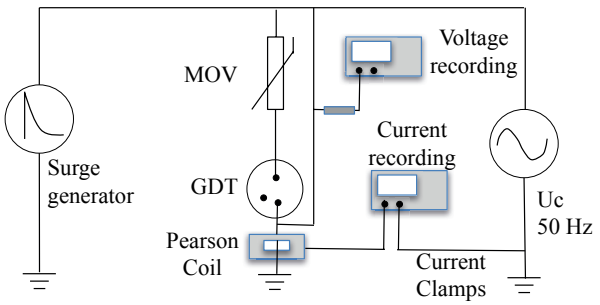

Figure 10: Measurement setup of the GDT and MOV in serial connection

The measurement setup from Fig. 10 is simulated using the TINA software tool. The scheme of the circuit with the GDT and MOV serial connection when the surge impulse (10/700 µs surge pulse shape) and a power line voltage of 400 V peak and frequency of 50 Hz exist simultaneously is presented in Fig. 11. An RC circuit is used to simulate a 10/700 µs single output impulse generator. This type of surge generator is designed according to the description of impulse generators proposed in [22]. The scheme of the 10/700 µs surge generator is shown in Fig. 11. An overvoltage pulse is generated using a capacitor with initial voltage, and with a switch defining the time of the pulse. A capacitor bank, represented by *C1*, will be charged to an initial DC voltage, U_{dc}. The capacitor will be discharged through a wave-shaping RC network. The voltage of the power frequency is added as a branch connected in parallel with the surge generator (Fig. 11).

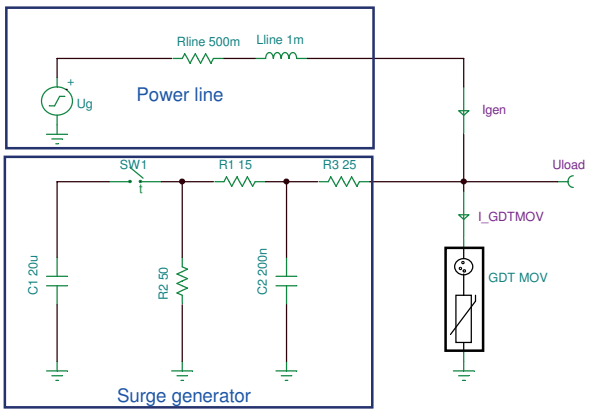

Figure 11: The circuit for the measurement setup of the GDT and MOV in serial connection

The measured values of these three waveforms are presented in Fig. 12. The three signals, presented on the screen of an oscilloscope, have different horizontal scales. The current waveform is indirectly observed through the voltage waveform and presented on the oscilloscope screen as an F1 waveform (Fig. 12). The waveform F1 has a time base of 200 µs/div and a vertical scale of 10 kA/div. The second waveform is current flowing through the power line branch. This signal has a time base of 200 ms/div and a vertical scale of 200 A/div. The third signal is the voltage at the terminals of the GDT and MOV serial connection. This waveform has the same time base as the second signal. The vertical scale is 500 V/div. After the appearance of the surge current impulse (F1 in Fig. 12), the surge arrester reacted and started to conduct. The surge current amplitude is 21 *kA*, with a 10/700 µs current pulse shape. It is evident from Fig. 12 that the surge wave appeared after 40 ms. The current from the surge generator also flows through the power line branch. The maximum value of the current in the power line branch during the surge current pulse is 198 *A*.

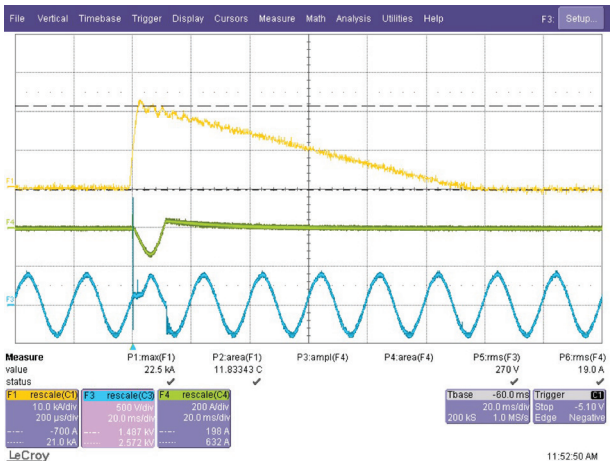

Figure 12: Surge current pulse, current in the power frequency branch and the voltage across the GDT and MOV serial connection

Fig. 13a shows the time diagram of the surge current generator presented in Fig. 11. After the appearance of the surge current pulse, the GDT and MOV responded and started to conduct. The voltage drop across the GDT and MOV stayed below 1000 V (Fig. 13b). The main part of the surge current was grounded through the GDT and MOV surge arrester. A small portion of the surge current during the conductive phase of the GDT and MOV was flowing through the power line branch. Extinguishing of the electric arc is assured when the MOVs are connected in series with GDTs.

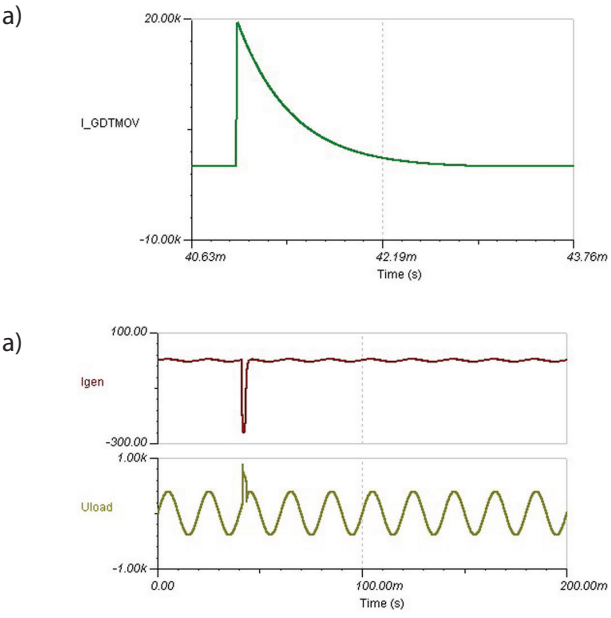

Figure 13: Surge current pulse, current in the power line branch and voltage of power frequency.

5 Conclusions

This paper presented overvoltage component models based on the Verilog-A language utilising a simplified approach to modelling components with nonlinear transfer characteristics and their description with built-in nonlinear functions. GDT and MOV Verilog-A models were provided, and simulations were completed using the TINA circuit simulator. A serial connection of GDTs and MOVs was constructed by creating instances of developed modules. The developed Verilog-A models were used together with SPICE models of other components for the simulation of surge protection devices.

The GDT and MOV serial connection was analysed, and the simulation results were compared with adequate laboratory measurements. Two types of measurements of the response of overvoltage components during the overvoltage impulse are presented. The validation of the developed models is based on a comparison of the residual voltages obtained by measurements and simulations. The first measurement is a standard test of overvoltage components, while the second measurement tests overvoltage components in a real environment.

The difference between simulation results and measurements is directly dependent on the accuracy of mathematical description of physical components at a higher abstraction levels. The compact models of GDT and MOV are based on presented mathematical descriptions. The differences that arise between the simulations and measurement results have been recognized by adjusting the models of surge pulse sources to better fit the measurement results. In the first case, a piecewise linear description of surge pulse is utilized and in the second case modelling with discrete elements is used.

We conclude that varistors connected in series with the arrester are well suited for limiting the follow-on current. The advantages of the serial connection of GDTs and MOVs are proven, and we showed that this topology eliminates certain deficiencies of individual components.

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