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Design of Operational Transconductance Amplifier with Temperature Compensation

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Abstract: In this paper an operational transconductance amplifier [1] with temperature compensation is presented. It is a voltage-controlled current source, which operates in an open loop configuration with a single output connected to a resistive load. The amplifier is internally compensated to keep the gain stable over the -40 °C to 125 °C temperature range. It features low input voltage noise and operates at supply voltages from 3 V to 5.5 V. Additionally, an internal 1.21 V bandgap reference is used to ensure a stable internal voltage reference point. The active area of the proposed integrated circuit designed with 0.18 µm Bipolar, CMOS, DMOS (BCD) technology is 750 µm x 260 µm. It consumes 423 µA of current and it has 8.87 nV/$\sqrt{}$Hz of input noise at 500 kHz. The resulting simulated voltage gain is 40 dB and variations are less than ±0.3 dB over the temperature range of -40 °C to 125 °C.

Keywords: Operational Transconductance Amplifier; Temperature compensated bias current; Temperature sensitivity optimization

Načrtovanje operacijskega transkonduktančnega ojačevalnika s temperaturno kompenzacijo

Izvleček: V članku je predstavljen transkonduktančni ojačevalnik s temperaturno kompenzacijo. Na izhod odprto-zančnega ojačevalnika oziroma napetostno krmiljenega tokovnega vira je priključeno uporovno breme. Notranja kompenzacija skrbi za stabilno ojačenje v temperaturnem območju od -40 °C do 125 °C. Poleg tega ojačevalnik izkazuje majhen vhodni šum in deluje v napetostnem območju od 3 V do 5.5 V. Vezje vsebuje napetostno referenco, ki poskrbi za stabilno referenčno točko. Integrirano vezje je bilo načrtano v 0.18 µm BCD (Bipolar, CMOS, DMOS) tehnologiji, njegova aktivna površina znaša 750 µm x 260 µm. Poraba ojačevalnika znaša 423 µA, njegova šumna gostota na vhodu je 8.87 nV/$\sqrt{}$Hz pri frekvenci 500 kHz. Napetostno ojačenje znaša 40 dB in v temperaturnem območju od -40 °C do 125 °C odstopa za manj kot ±0.3 dB.

Ključne besede: Transkonduktančni operacijski ojačevalnik; temperaturna kompenzacija delovnega toka; optimizacija temperaturne občutljivosti

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1 Introduction

In the paper, an integrated circuit including a symmetrical Operational Transconductance Amplifier (OTA) with temperature compensation is described. The OTA can be presented as a voltage controlled current source. The ideal OTA has very high input and output impedances and a wide frequency bandwidth. The output current I_{OUT} is proportional to the differential input voltage and is expressed as:

$$I_{OUT} = g_m V_d \tag{1}$$

where g_m is the transconductance of the amplifier and V_d is the differential input voltage.

One of the major drawbacks of the OTA is its high temperature sensitivity, caused by inversely proportional temperature variations of g_m [2, 3]. Transconductance of the Metal-Oxide-Semiconductor (MOS) transistor, using small signal model in saturation region is defined as follows:

$$g_m = \sqrt{2\mu_n C_{ox}(\frac{W}{L})I_D} \tag{2}$$

where μ_n is carrier mobility, C_{ox} is oxide capacitance, W is width of the device, L is length of the channel and I_D is drain current [4].

The root cause of temperature variations is the temperature dependent threshold voltage V_T and the carrier mobility μ_n variations of the MOS transistor, according to equations (2) and (3):

$$V_T(T) = V_T(T_0) + \alpha_{VT}(T - T_0) \tag{3}$$

$$\mu_n(T) = \mu_n(T_0)\left(\frac{T}{T_0}\right)^{\alpha_\mu} \tag{4}$$

where T_0 is the reference temperature (300 °K), α_{VT} and α_μ are negative values which vary with temperature [5]. As one of possible solutions, a circuit with output voltage Proportional To Absolute Temperature (PTAT) can be implemented to compensate the temperature variations of g_m. The difference between the two base-emitter voltages in PTAT is expressed as:

$$\Delta V_{BE} = V_t \ln(J_2 / J_1) \tag{5}$$

where V_t is thermal voltage and J_1, J_2 are different current densities of bipolar transistors. The PTAT circuit generates voltage which has a positive Temperature Coefficient (TC) [4].

The following section (Section 2) presents the OTA design method to overcome the mentioned problem. In section 3, simulation results for typical simulation conditions, process variations and Monte Carlo analyses are presented.

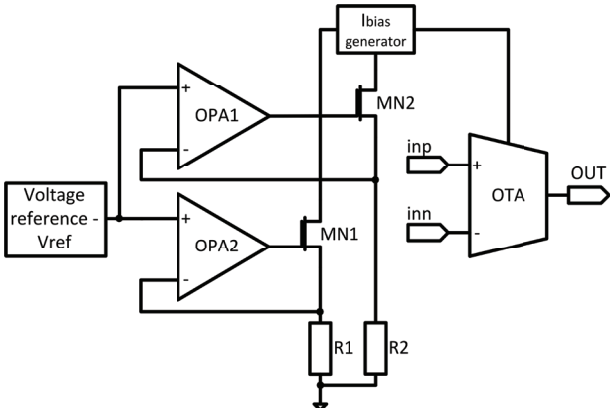

Figure 1: Block diagram of integrated circuit**.**

2 Ota circuit design

The block diagram of the OTA with temperature compensation is shown in Fig.1. The main advantage of the proposed solution is the temperature compensated bias current. The compensation circuit consists of two resistors (R1 and R2) having different TC. The block diagram also includes internal a 1.21 V voltage reference (V_{ref}), biasing current generator (I_{bias} generator) which compensate the temperature variations of g_m, two Operational Amplifiers (OPA1 and OPA2) for voltage to current conversion and OTA circuit. Our objective was to keep the gain of the OTA stable over the -40 °C to

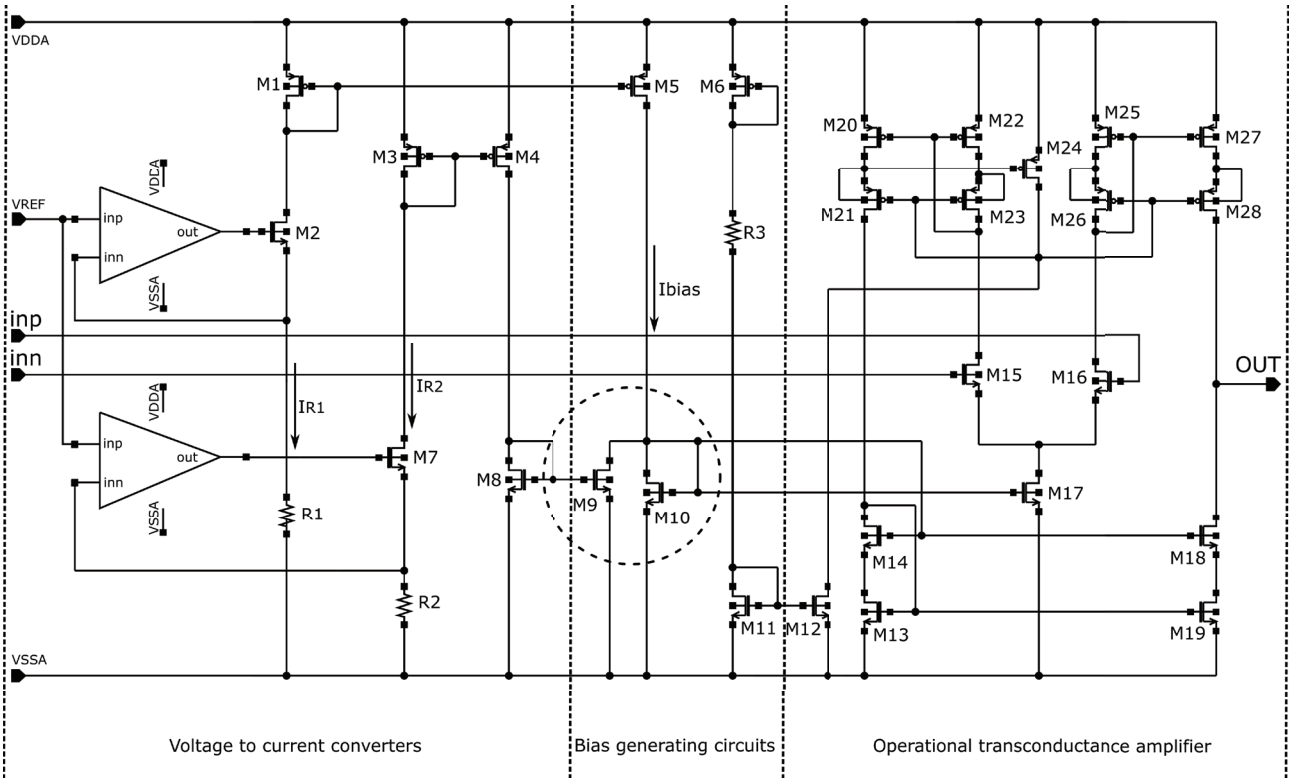

Figure 2: The schematic of integrated circuit.

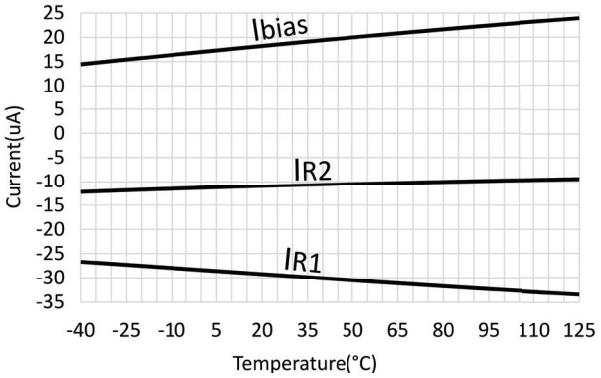

Figure 3: Generated currents.

125 °C temperature range, low input voltage noise and high Power Supply Rejection Ratio (PSRR).

2.1 Topology of the circuit

The schematic of the balanced OTA with temperature compensation is shown in the Fig. 2. The voltage to currents converters are used to convert the reference bandgap voltage to the corresponding current. Both converters are designed as classic two stage amplifiers with a N type Metal-Oxide-Semiconductor (NMOS) input differential stage and a common source output stage including compensation capacitor and resistor. To ensure precise conversion, the temperature stable reference voltage is employed. The voltage reference - bandgap circuit, maintains a stable voltage over the temperature range and power supply voltage variations. The OTA consists of NMOS input differential stage and three current mirrors. Transistors M20 – M23 form the first current mirror stage, M25 – M28 form the second current mirror stage and M13, M14, M18 and M19 form the third current mirror stage. To increase the output impedance the cascode current mirrors are used. The gate of transistors are connected and biased as low voltage cascode, which keeps the minimum drain source voltages of transistor M13, M22 and M25 and also insures transistor saturation operation. The Length (L) of transistor M10 is higher in order to compensate the body effect of cascode transistors M14 and M18 [6].

2.4 Compensation circuit

The compensation circuit consists of transistors M9 and M10 and two resistors (R1 and R2) with different TC, which is calculated using the box-method [7], -1618 ppm/°C and 1322 ppm/°C, respectively. The Fig. 3 presents the currents I_{R1} and I_{R2}, determined by resistors R1 and R2, and bias current I_{bias}, flowing through M10.

The compensation circuit generates bias current I_{bias} which is stated as:

$$I_{bias} = -I_{R1} + I_{R2} \tag{6}$$

The bias current I_{bias} increases with temperature compensating decreasing transconductance of OTA.

3 Simulation results

3.2 Results for typical simulation parameters

The typical process parameters simulations at 25 °C were performed for the supply voltages 3.3 V and 5 V, respectively. The simulation results are presented in Table 1. Input noise density was measured at 500 kHz.

Table 1: Simulation results at typical simulation conditions.

Param. \ Suppl.	3.3 V	5 V	Units
Ivdda	423	540	µA
G	40.2	40.4	dB
BW	13.6	15.0	MHz
Input noise density	8.87	8.56	nV/√Hz
Input offset voltage	1.08	1.99	mV
CMRR	-132	-142	dB
+SR	9.01	9.60	V/µs
-SR	9.23	9.72	V/µs
PSRR @ 100 Hz	-73.5	-78.2	dB
Transconductance	778	737	µA/V

The input referred noise voltage can be further reduced by changing the channel *W/L* ratio of the M15 and M16 transistors or increasing the bias current I_{bias}. This action would lead to larger chip area (higher cost) and higher power consumption. To reduce the offset which effects the performance of the OTA, the auto-zeroing or chopping technique method could be used, adding complexity to the design. Precise matching strategies of the transistors and resistors devices must be used to minimize offsets and provide symmetry.

Typical performance characteristics for a 3.3 V supply voltage are shown from Figures 4 to 7. The input referred noise voltage was measured at 500 kHz, while PSRR was measured at 100 Hz.

Fig. 4 shows the voltage gain vs. frequency at three temperatures (-40 °C, 25 °C, 125°C), which is 40 dB. The results show that the gain sensitivity to temperature variations are almost eliminated with the presented design. The bandwidth of the OTA varies from 14.1 MHz at -40 °C to 12.8 MHz at 125 °C.

Table 2: Corner analysis results

Parameters	FF1	SS1	FS1	SF1	FF2	SS2	FS2	SF2	Units
Ivdda	485	374	430	416	621	476	550	530	µA
G	41.3	39.2	40.2	40.1	41.5	39.4	40.45	40.32	dB
BW	14.5	12.6	13.8	13.3	16.0	14.0	15.2	14.7	MHz
Input noise density	8.25	9.43	8.81	8.92	7.95	9.13	8.50	8.62	nV/√Hz
Offset	1.57	0.71	1.16	1.00	2.72	1.37	2.11	1.89	mV
CMRR	-132	-130	-134	-129	-140	-144	-141	-143	dB
+SR	10.28	8.02	9.06	8.95	10.97	8.54	9.66	9.54	V/µs
-SR	10.54	8.19	9.3	9.13	11.1	8.65	9.79	9.66	V/µs
PSRR @ 100 Hz	-68.9	-78.5	-75.3	-72.1	-73.8	-83.5	-81.3	-75.8	dB
Transconductance	856	715	785	770	816	672	737	737	µA/V

Note[1]: Supply voltage: 3.3 V
Note[2]: Supply voltage: 5 V

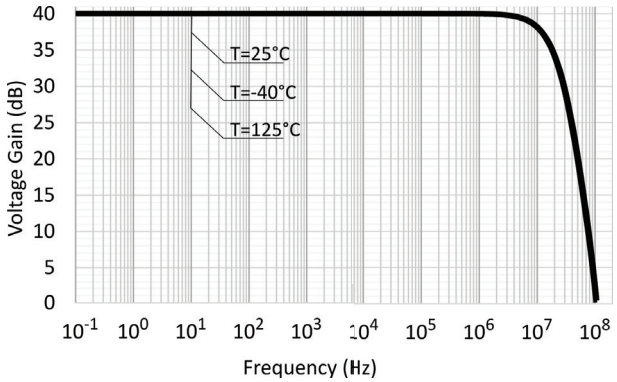

Figure 4: Voltage Gain vs. Frequency

Fig. 5 presents input referred noise voltage density as a function of frequency at temperatures (-40 °C, 25 °C, 125°C). The noise measured at 500 kHz increases with temperature from 8.16 nV/√Hz at -40 °C to 10.1 nV/√Hz at 125 °C.

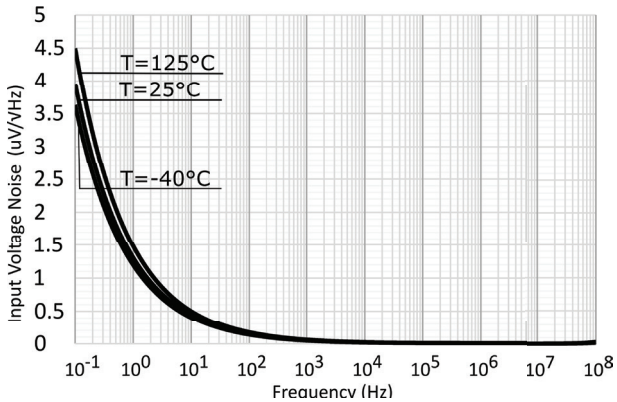

Figure 5: Input Noise Voltage vs. Frequency

The Common Mode Rejection Ratio (CMRR) is measured as the ratio of the common mode gain to differential mode gain. At lower frequencies the CMRR varies from -131 dB at -40 °C to -121 dB at 125 °C. The results are shown in Fig. 6.

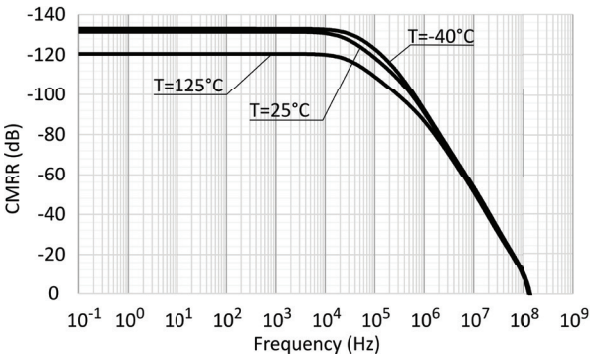

Figure 6: CMRR vs. Frequency

The PSRR is measured as the ratio of the OTA output variation vs. the supply voltage variation regardless the input signal. The PSRR varies from -78.2 dB at -40 °C to -62.9 dB at 125 °C, measured at 100 Hz. At higher frequencies, PSRR deteriorates. The results are shown in Fig. 7.

3.2.1 Corner analysis

The process variations of MOSFETs and resistors influence on performance of fabricated integrated circuit. Therefore, the OTA was simulated for different process corners – four corner models (FF, SS, FS and SF). The results at 25 °C are gathered in Table 2. The input noise density was measured at 500 kHz.

3.2.2 Monte Carlo simulation

In this section the results of the Monte Carlo (MC) analysis are shown. The MC simulations were performed

including mismatch and process variations at typical conditions (25 °C and 3.3 V) comprising 512 MC runs. The simulation results are presented in the following histograms.

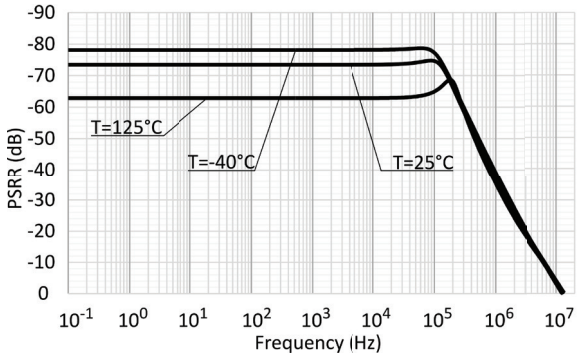

Figure 7: PSRR vs. Frequency

Fig. 8 shows the resulting histogram of input referred noise density at 500 kHz, which has a mean value of 8.873 nV/√Hz and the standard deviation of 151 pV/√Hz. The result is a bit higher than the mean value of previously shown corner analysis results, which is 8.853 nV/√Hz.

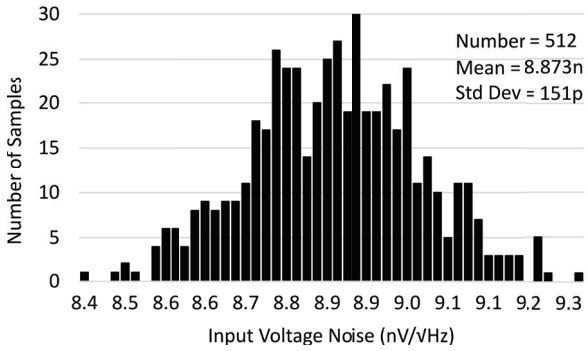

Figure 8: MC test of Input Voltage Noise

The voltage gain distribution is shown in the Fig. 9. The mean value from the corner analysis results is 40.20 dB

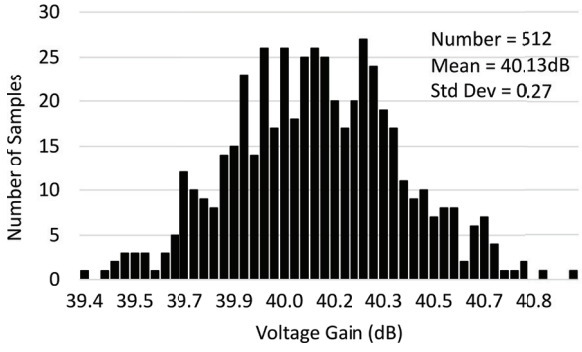

Figure 9: MC test of Voltage Gain

and it is slightly higher than the mean value obtained by MC analysis, which is 40.13 dB with a standard deviation of 0.27 dB.

The offset voltage mean value from MC runs is 1.079 mV with standard deviation of 103.7 uV. It is shown in Fig. 10.

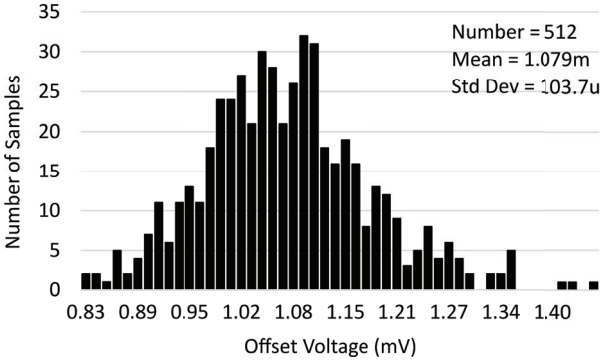

Figure 10: MC test of Offset Voltage

The mean value of the voltage offset from corner analysis is 1.110 mV, which is higher than the MC results.

The comparison between corner and MC analyses must be done carefully as the corner analysis comprises also temperature and supply voltage variations, which especially influence voltage offset.

4 Layout of presented circuit

The layout of the presented integrated circuit is shown on Fig. 11.

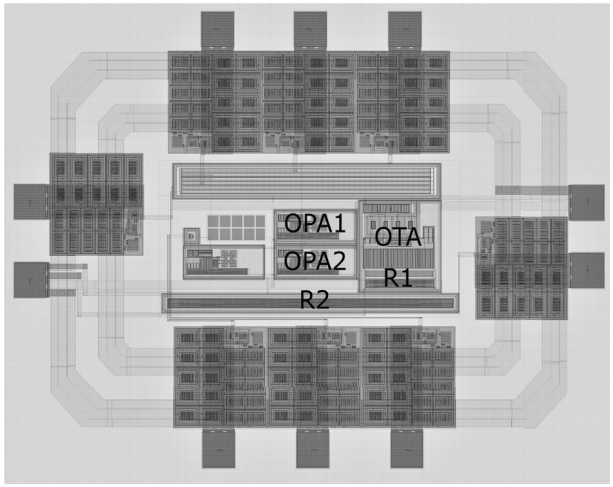

Figure 11: Layout of the integrated circuit

The active area of the circuit, without bonding pads and supply connection rings, is 750 µm x 260 µm. The integrated circuit has been designed with the 0.18 µm BCD technology as a part of the System on Chip (SoC). The BCD technology allows mixed - signal design using low and high voltage transistors (DMOS) on the same die (reduces cost, area and power consumption). The voltage to current converter main part is presented by resistors R1 – N+ poly without salicide and R2 – N+ diffusion without salicide, which means that resistors do not have an additional process mask of salicide, reducing the sheet resistance (Ω/sq) of the resistors. For ASIC area reduction, N – well resistors could be used, but they have high nonlinearity and larger parasitic capacitance between N – well and substrate. The integrated circuit has been sent to the fabrication factory.

5 Conclusions and next steps

The OTA was designed and analyzed using the 0.18 µm BCD technology. The temperature sensitivity of the OTA has been optimized and reduced, using the bias control technique and a stable internal voltage reference. The proposed circuit shows voltage gain variations lower than ±0.3 dB in the temperature range from -40 °C to 125 °C and lower than 0.5 dB when varying the supply voltage in the range from 3 V to 5.5 V. The equivalent input referred noise voltage is simulated to be lower than 10 nV/√Hz at 500 kHz and 25 °C, and voltage offset lower than 2.8 mV. To overcome the problem of process variations, especially the resistors R1 and R2 which are used for compensation current generation and are one of the most critical elements in compensations circuit, the resistance of both R1 and R2 resistors will be precisely trimmed. The issue could be easily solved by employing effective and uncomplicated trimming resistor stage for each of them separately and internal One-Time-Programmable (OTP) memory cells.

6 References

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