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Spintronics as a Non-Volatile Complement to Modern Microelectronics

Viktor Sverdlov[1], Josef Weinbub[2], and Siegfried Selberherr[1]

[1]Institute for Microelectronics, TU Wien, Wien, Austria
[2]Christian Doppler Laboratory for High Performance TCAD, Institute for Microelectronics, TU Wien, Wien, Austria

Abstract: Continuous miniaturization of semiconductor devices has been the main driver behind the outstanding increase of speed and performance of integrated circuits. In addition to a harmful active power penalty, small device dimensions result in rapidly rising leakages and fast growing stand-by power. The critical high power consumption becomes incompatible with the global demands to sustain and accelerate the vital industrial growth, and an introduction of new solutions for energy efficient computations becomes paramount.

A highly attractive option to reduce power consumption is to introduce non-volatility in integrated circuits. Preserving the data without power eliminates the need for refreshment cycles and related leakages as well as the necessity to initialize the data in temporarily unused parts of the circuit. Spin transistors are promising devices, with the charge-based functionality complemented by the electron spin. The non-volatility is introduced by making the source and drain ferromagnetic. Recent advances in resolving several fundamental problems including spin injection from a metal ferromagnet to a semiconductor, spin propagation and relaxation, as well as spin manipulation by the electric field, resulted in successful demonstrations of such devices. However, the small relative current ratio between parallel/anti-parallel source and drain alignment at room temperature remains a substantial challenge preventing these devices from entering the market in the near future.

In contrast, a magnetic tunnel junction is an excellent candidate for realizing power-reducing approaches, as it possesses a simple structure, long retention time, high endurance, fast operation speed, and yields high integration density. Magnetic tunnel junctions with large magnetoresistance ratio are perfectly suited as key elements of non-volatile magnetoresistive memory compatible with the complementary metal-oxide-semiconductor technology and capable to replace dynamic and potentially static random access memories. We review the present status of the technology, remaining challenges, as well as approaches to resolve the remaining problems. Regarding active power reduction, delegating data processing capabilities into the non-volatile segment and combining non-volatile elements with CMOS allows for efficient power gating. It also paves the way for a new low-power and high-performance in-memory processing paradigm-based on an intrinsic logic-in-memory architecture, where the same non-volatile elements are used to store and to process the information.

Spintronics kot trajno dopolnilo moderne mikroelektronike

Keywords: Spintronics; non-volatility; spin field-effect transistors; spin relaxation; magnetic tunnel junctions; magnetic random access memory (MRAM), spin-transfer torque MRAM, spin-orbit torque MRAM; voltage-controlled MRAM; logic-in-memory

Sestavljivi 2D Vernier TDC na osnovi obročnih oscilatorjev

Izvleček: Nenehno zmanjševanje polprevodniških naprav je bila glavna gonilna sila izjemnega povečanja hitrosti in zmogljivosti integriranih vezij. Poleg škodljivega povečevanja aktivne moči majhne dimenzije naprav vplivajo tudi na višje uhajalne tokove in večjo porabo v stanju mirovanja. Visoka poraba energije je postala nekompatibilna z zahtevami vzdržnosti rastoče industrije, zato so potrebne nove rešitve učinkovite rabe energije.

Zelo privlačna možnost zmanjšanja porabe energije je uvedba trajnosti v integriranih vezjih. Ohranjanje podatkov brez porabe energije odpravlja potrebo po osveževalnih ciklih in uhajanjih ter nujnosti inicializiranja podatkov v začasno neuporabljenih delih vezja. Spin tranzistorji so obetavni elementi, ki temeljijo na osnovi naboja z dopolnitvijo vrtilne količine elektrona (spin). Trajnost se ustvari tako, da sta vir in ponor feromagnetna. Nedavni napredek pri reševanju številnih temeljnih problemov, vključno s injektiranjem vrtilne količine iz kovinskega feromagnetika v polprevodnik, vzpostavitev in relaksacija vrtilne količine ter upravljanje vrtilne količine z električnim poljem,

je bil ključen za uspešno demonstracijo takšnih naprav. Kljub temu ostaja relativno majhno razmerje tokov med vzporednim/nasprotnim položajem izvora in ponora pri sobni temperaturi ključen izziv, ki preprečuje vstop teh naprav na trg v bližnji prihodnosti.

V nasprotju s tem je magnetni tunelski spoj odličen kandidat za uresničevanje pristopov zmanjšanja moči, saj ima preprosto strukturo, dolg čas zadrževanja, visoko vzdržljivost, hitro obratovalno hitrost in visoko gostoto integracije. Magnetni tunelski spoji z visokim razmerjem magnetoresonance so idealni za uporabo v trajnih megnetorezistivnih spominih, ki so združljivi s komplementarno kovina-oksid-polprevodnik tehnologijo in sposobni zamenjati dinamičen in statičen spomin z naključnim dostopom. V članku je podan pregled tehnologije, izzivi in postopki, kako rešiti obstoječe probleme.

Zmanjševanje porabe energije se lahko doseže s prenosom obdelave podatkov v trajne segmente in kombinacijo trajnih elementov s CMOS. Prav tako se utira pot novi paradigmi procesiranja v pomnilniku z nizko porabo energije in visoko zmogljivostjo, ki temelji na arhitekturi logike v pomnilniku, kjer se za shranjevanje in obdelavo podatkov uporabljajo isti trajni elementi.

Ključne besede: Spintronika; trajnost; tranzistorji z vrtilnim poljem; relaksacija vrtilne količine; magnetni tunelski spoj; magnetni spomin z naključnim dostopom (MRAM); navor prenosa vrtilnosti MRAM; navor orbite vrtilnosti MRAM; napetostno krmiljen MRAM; spominska logika

** Corresponding Author's e-mail: sverdlov@iue.tuwien.ac.at*

1 Introduction

The breathtaking increase in performance and speed of integrated circuits has been enabled by continuous miniaturization of complementary metal-oxide semiconductor (CMOS) devices. On this exciting path numerous outstanding technological challenges have been resolved. Among the most crucial technological changes recently adopted by the semiconductor industry to boost CMOS performance while maintaining gate control over the semiconductor channel are the introduction of strain [1], high-k gate dielectrics and metal gates [2], and a three-dimensional (3D) tri-gate transistor architecture [3-5]. The successes and innovative solutions developed for the microelectronics technology have been always supported by sophisticated simulation tools, which allow reducing the research and development costs by 35-40% [6].

Although transistor sizes are scaled down, the on-currents cannot be further decreased due to the need to charge/discharge the load capacitances and to maintain the clock, which is saturated at approximately 4.0 GHz. Increasing the clock frequency results in an active power penalty, while continuous transistor scaling results in growing leakages and stand-by power. Novel revolutionary approaches are desperately needed in the long run to sustain the vital societal and industrial progress in computing performance whilst simultaneously reducing power consumption.

The ultimate solution to one of the primary issues – the power reduction – is to introduce non-volatility into the circuits. Non-volatility is the ability to preserve data, when the supply power is turned off. It enables stand-by power-free integrated circuits as no information is lost and there is no need to recover the data, when the power is turned on. Non-volatility is crucial for eliminating the leakage power dissipation and data refreshment cycles. Apart from stand-alone applications, e.g., critical program and data storage devices in extreme environments employed in the air and space industry, it is particularly promising to use non-volatility in the main computer memory as a replacement of conventional volatile CMOS-based dynamic random-access memory (DRAM) [7], which will drastically reduce energy consumption. In modern multicore processors, much of the energy consumption appears in the hierarchical multi-level cache memory structure. To reduce this energy consumption, a viable approach is to replace the caches with a non-volatile memory technology which also offers a reduced memory cell size compared to static random-access memory (SRAM) [7]. This will help bridging the speed gap between the last-level cashes and main memory, since CMOS SRAM is much faster compared to CMOS DRAM.

To be competitive with the traditional volatile memory technologies and also with non-volatile flash memory, emerging non-volatile memories must offer a fast switching time, a high integration density supported with good scalability, a long retention time, a high endurance, and a low power consumption. At the same time, they must possess a simple structure to reduce fabrication costs and the new non-volatile circuit elements must be compatible with CMOS technology to benefit from advantages provided by the well-developed CMOS fabrication technology.

A spin field-effect transistor (SpinFET) is a promising future semiconductor device with a performance poten-

tially superior to that achieved in the present transistor technology. The non-volatility in SpinFETs is added by replacing the non-magnetic source and drain in a FET by its ferromagnetic counterparts. The two ferromagnetic contacts (source and drain) are linked by a non-magnetic semiconductor channel region. Metallic ferromagnetic contacts serve not only as an injector/detector of the spin-polarized electron charge current in the channel, but, because of their magnetization, the source and drain electrodes provide an additional current modulation due to their capabilities to inject/detect spins [8]. Indeed, the electron current gets enhanced in the case of parallel alignment between the source/drain electrodes as electrons are injected with spins parallel to the drain magnetization and can easily escape from the channel to the drain, while the current is suppressed for anti-parallel magnetization alignment [8]. As the magnetization of the source/drain can be manipulated by means of an external magnetic field and/or current (by means of the spin-transfer torque), the two on-current states for parallel/anti-parallel magnetization alignment potentially enable reprogrammable logic [9]. Importantly, the relative magnetization orientation between source and drain is preserved without external power, which makes reprogrammable logic partly non-volatile. Below we discuss recent advances and remaining challenges to realize SpinFET-based logic in detail. We only stress the most important, in our opinion, shortcoming to overcome, namely, a small relative difference between the on-currents in parallel and anti-parallel source/drain alignment.

Magnetoresistive random access memory (MRAM) and in particular spin transfer torque (STT) MRAM possesses many, if not all, of these advantages and is considered as a perfect candidate for future universal memory applications. MRAM is CMOS-integrable, which increases its potential to replace the typical processor-embedded SRAM and DRAM.

With STT MRAM currently emerging as a commercial product for stand-alone applications, it will be critically important to introduce STT MRAM in the main computer memory, i.e., to replace conventional DRAM and SRAM. This will create a new innovative multi-billion dollar industry and will sustain the breathtaking path of electronics by delivering cheaper, faster, and environmentally friendlier compact and mobile devices. Bringing STT MRAM into the vast computer memory market as embedded and stand-alone applications for traditional high-performance and low-power mobile platforms will result in an exponential growth of the non-volatile memory market share in the near future.

Regardless of the first commercial STT MRAM-based products for stand-alone applications being available, one critical aspect of the currently used STT MRAM technology is a relatively high switching current, which again is in sharp contrast to the overall demand for reduced energy consumption. This obviously prevents the MRAM from successfully entering the vast computer memory market. The problem of high switching current and large active writing energy jeopardizes the advantages provided by non-volatility, such as zero stand-by power, no data refreshment, and no data recovery. Several plausible approaches to address these issues are conceivable including the replacement of the in-plane magnetization orientation in magnetic tunnel junctions (MTJs) with perpendicular magnetization, the use of composite free recording layers, decoupling the write and read current paths, controlling magnetization by voltage, and employing new materials with improved properties and characteristics.

2 Spin transistor

In a SpinFET [8] schematically shown in Fig.1 the electrons with spin aligned to the drain magnetization direction can easily leave the channel to the drain thus contributing to the current. The total current through the device depends on the relative angle between the magnetization direction of the drain and the electron spin polarization at the end of the semiconductor channel. The electron spin orientation at the end of the channel is determined by the source magnetization and can be additionally manipulated by the modulation which is achieved by tuning the strength of the effective spin-orbit interaction in the channel induced by the gate voltage. As a non-equilibrium quantity, the injected spin relaxes to its equilibrium zero value while propagating through the channel. Spin relaxation is an important detrimental ingredient as it reduces the current modulation and affects the SpinFET functionality.

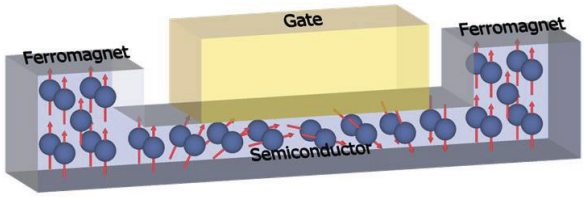

Figure 1: Datta-Das SpinFET [8]. Spin-polarized electrons are injected from a ferromagnetic source and absorbed by in a ferromagnetic drain. The electron spins in the channel are manipulated by means of the gate voltage-dependent spin-orbit interaction.

2.1 Spin-Orbit Interaction

The spin relaxation is governed by the spin-orbit interaction (SOI) and scattering, both spin-dependent and

spin-independent, and manifests itself differently in semiconductors with and without the inversion symmetry [10,11].

In crystals obeying the inversion symmetry (silicon, germanium) the spin relaxation is governed be the Elliott-Yafet mechanism [10,11]. The wave function with a fixed spin projection (defining the quantization axis) is not an eigenstate of the Hamiltonian due to the electron momentum-dependent SOI. In other words, the SOI forces the eigenstate wave function to possess a small but finite contribution with an opposite spin projection in the fixed basis. Therefore, the small but finite amplitude to flip the electron spin appears at every spin-independent scattering event – the Elliott process [12]. This is complemented by the Yafet spin-flip events due to SOI-dependent electron-phonon scattering. In silicon the electron spin relaxation is determined by the inter-valley transitions [12] and can be efficiently controlled by stress [13]. In silicon channels, uniaxial stress generating shear strain is particularly efficient to suppress the spin relaxation [14] as it lifts the degeneracy between the two unprimed subband ladders [15]. In addition, choosing the spin injection direction also boosts the spin lifetime by a factor of two [16], as shown in Fig.2.

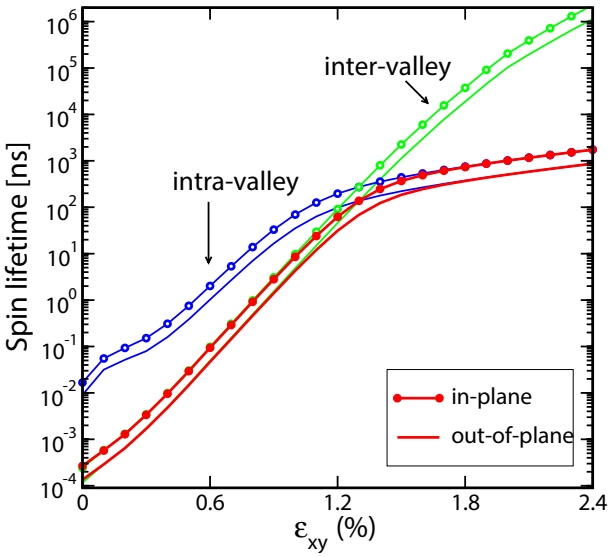

Figure 2: Spin lifetime in (001) thin Si film as a function of shear strain. The spin lifetime is a factor of two longer for spins injected in-plane as compared to the time for spins injected perpendicular to the film. The factor of two is preserved for both inter- and intra-valley scattering and is independent of the scattering mechanism (electron-phonon and surface roughness scattering).

In III-V materials without inversion symmetry the degeneracy between the up and down spin states with the same electron momentum is lifted, and the spin relaxation is governed by the Dyakonov-Perel mechanism [10,11]. However, the SOI does not always play a detrimental role. In semiconductor channels the SOI may also be used efficiently to manipulate the electron spins in the channel [8]. The inversion symmetry in the channel can additionally be violated by applying the gate voltage. In this case the strength of the effective SOI depends on the effective electric field perpendicular to the channel [17]. The strength of the gate voltage-dependent SOI can be used to modulate the current between the ferromagnetic source and drain by means of an additional spin modulation in the channel resulting in a different spin orientation relative to the drain as compared to the case without SOI [8]. Importantly, as the strength of the SOI in the channel depends on the effective electric field, the suggested method provides a purely electrical mean of manipulating the electron spins and thus the current in the channel.

The voltage-induced SOI in III-V materials can be used for an efficient spin injection in the channel from the point contacts [18]. Additional gates are used to create the point contacts to the two-dimensional (2D) electron gas by confining the 2D gas in the III-V channel under the gates. Application of different voltages to these gates generates the spin-orbit Rashba field perpendicular to the point contact. By properly tuning the chemical potential one can achieve that, due to this SOI, all electrons moving to the right are spin-polarized (while electrons moving to the left are polarized in the opposite direction). Thereby an efficient and purely electrical spin injection/detection is achieved. Using this injection scheme, the ever first reliable demonstration [18] of a working SpinFET [8] suggested in 1990 was achieved.

Not long ago, new 2D materials (graphene, transition metal dichalcogenides), become attractive for future microelectronics applications. Recently, a new concept for realizing a spin switch with a graphene channel was demonstrated [19]. Spin-polarized electrons are injected into the graphene, a good spin conductor due to low SOI, and reach the drain electrode, if the electrochemical potential in MoS_2 is tuned into the energy gap. In this case the electrons do not enter MoS_2. The situation is completely changed, if the electrochemical potential is tuned by the gate into the MoS_2 conduction band. In this case a parallel path for electrons through a material with high SOI is open, which results in strong spin relaxation, so that the current reaching the drain is not spin-polarized.

Regardless of the successful demonstration of the SpinFET, the conductance modulations were only resolved at temperatures far below 300K. The spin switch [19] discussed above was demonstrated to work at

temperatures below 200K and requires additional cooling, which modern microelectronics working at room temperature is striving to avoid. Recently, the first successful demonstration of a silicon spin metal-oxide-semiconductor field-effect transistor (SpinMOSFET) at room temperature [20] was presented. In silicon the strength of the Rashba SOI is much smaller compared to that in III-V semiconductors. Therefore, the SOI cannot be used for spin manipulation. Thus, the current modulation in the SpinMOSFET is achieved by altering the relative magnetization between the ferromagnetic source and drain. This way, a high difference between the on-currents in parallel and anti-parallel source/drain configuration was demonstrated. However, the relative ratio of the currents, a characteristic similar to the tunnel magnetoresistance (TMR) ratio, is still several orders of magnitude lower [20] than the TMR in MTJs. Fig.3 shows the TMR in a silicon SpinFET as a function of the SOI strength, for several channel lengths for an ideal case when the spin relaxation is neglected. In order to facilitate the spin injection and detection, delta function-like Schottky barriers between the source, drain, and the channel of the strength $U = \frac{h}{2\pi}\sqrt{\frac{E_F}{2m_F}}$ were h is the Plank constant, E_F and m_F are the Fermi energy and the electron mass in the ferromagnetic contacts, are assumed. Even in this ideal case the TMR is about 10%, much inferior to that in MTJs. A TMR less than 1% was experimentally observed at room temperature [20].

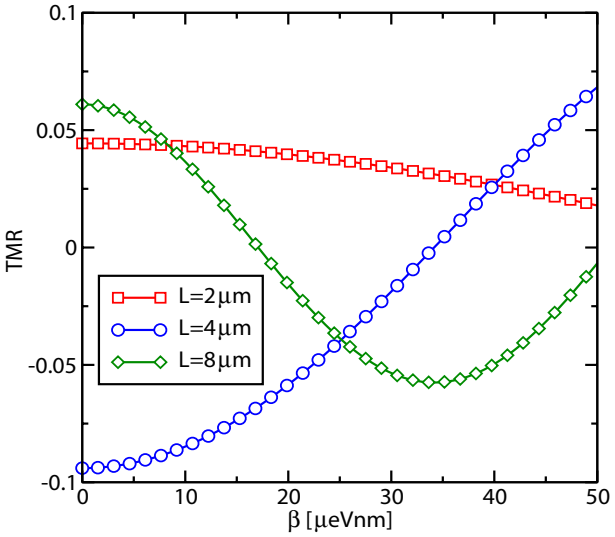

Figure 3: The ratio of the resistance difference in antiparallel and parallel configurations to the resistance in parallel configuration of the source and drain in Si-based SpinFETs as a function of the spin-orbit interaction strength, for several channel lengths.

2.2 Spin Injection and Spin-Dependent Tunneling

The device described above can function only if the electron spins are efficiently injected/extracted in/from the channel. As there are no semiconductor ferromagnets at room temperature, to achieve the efficient injection/detection from metal ferromagnets in the semiconductor channel and vice versa, a thin tunneling barrier must be placed between the electrodes and the channels [21] to mitigate the spin impedance mismatch. However, the signal attributed to the spin injection [22] appears to be much weaker as compared to the large effect [23] currently attributed to the spin-dependent resonant tunneling [24-26], and the development of efficient ways to electrically inject spins from a ferromagnetic metal in a semiconductor has become an area of active research.

To summarize, although many fundamental challenges have been resolved and both a SpinFET and a SpinMOSFET have been successfully demonstrated, an enhancement of the on-current ratio between the parallel and anti-parallel source/drain magnetization alignment at room temperature remains one of the main challenges. In addition, both SpinFET and SpinMOSFET still rely on the charge current to transfer the spin, which may set some limitations for the applicability of such devices in main-stream microelectronics in the future. Non-volatile devices based on MTJs possess the TMR suitable for practical applications and are reviewed below.

3 Magnetoresistive random access memory

Applications driven by magnetic moments and induced magnetic fields have a large share in typical information technology products. Coupling between magnetic fields and currents in coils was employed in the first electronic devices. However, the coupling is relatively weak, resulting in low efficiency and high energy supply costs. An efficient coupling between the electrical and the magnetic degree of freedom is possible on a quantum mechanical level and was discovered in 1986 as a phenomenon called the giant magnetoresistance (GMR) effect. This facilitated a reliable, purely electrical read operation of the information encoded in the magnetization orientation. Based on this principle hard drive storage devices with extremely high density appeared on the market. The enormous impact of this discovery on the development of information technology was recognized by awarding the inventors the Nobel Prize in 2007 [27,28].

The next generation of storage devices with higher density is based on the unique properties of the MTJ. It was discovered that, if the non-magnetic metal layer in a GMR memory element is substituted by a thin dielectric, the tunneling current through the structure strongly depends on the relative polarization of the ferromagnetic contacts (Fig.4). The difference in the MTJ resistivity can reach several hundred percent at room temperature [29]. Thanks to this technology a new generation of hard drives with even higher storage densities has been developed.

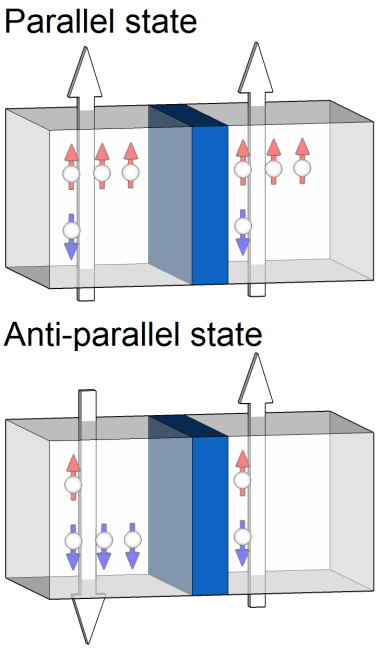

Figure 4: A magnetic tunnel junction possesses low (high) resistance for parallel (antiparallel) relative orientation between the ferromagnetic electrodes.

In order to be used in memories, MTJs must be complemented with the ability to efficiently convert charge information into magnetic moment orientation. Writing the state by the magnetic field is currently used in toggle switching commercial MRAM. This method, however, is not scalable as the magnetic field is generated by the current, which leads to a current increase with scaling [30].

3.1 Spin Transfer Torque Magnitoresistive Random Access Memory

The STT effect [31,32] has been proven to be a perfect alternative to the magnetic field for magnetization switching. The STT is used for purely electrical data writing by passing the current through the MTJ. The memory technology based on MTJs and the STT effect has resulted in the development of STT MRAM. STT MRAM is characterized by lower power-consumption and better scalability than conventional MRAM, where the switching is performed by the magnetic field [33] generated by an electric current passing through the write lines next to the cell. Several cells are arranged in a matrix connected with bit and world lines. A cell in this cross-point architecture is written by simultaneously selecting the cell with current pulses applied to the corresponding world and bit lines. The problem of half-selected cells [30] is solved by the application of a certain pulse sequence to the lines supplemented with a special design of the free layer arranged as a synthetic anti-ferromagnet [34]. This results in a deterministic, toggle-like fast switching of the free layer.

The magnetic field employed for switching prevents MRAM from scaling down beyond 90nm [35] as the current needed for the field generation rapidly increases with scaling. STT [31,32] opened a new way of manipulating magnetization dynamics by using spin-polarized currents instead of magnetic fields. The spin-polarized current allows writing the information into the memory cell by purely electrical means. When electrons pass through a fixed ferromagnetic layer, their spins become aligned with the magnetization. When these spin-polarized electrons enter the free layer, they become aligned with the magnetization of the free layer within a transition layer of a few angstroms. The electron spins change results in a torque exerted on the magnetization of the free layer. This torque causes magnetization switching, if it is large enough to overcome the damping. By altering the current polarity the magnetization of the free layer can be switched from the anti-parallel to the parallel state and back with respect to the reference layer.

The interest in STT MRAM has increased significantly after the observation of spin torque induced switching in AlO_x-based [36] and MgO-based [37] STT MRAM cells. Depending on the orientation of the layer magnetizations the magnetic pillars can be divided into two categories: (1) perpendicular with out-of-plane magnetization direction and (2) in-plane with the magnetization lying in the plane of the magnetic layer. The introduction of STT MRAM with in-plane magnetization orientation to the market has already begun with the first demonstration by Everspin Technologies [38] of a 64Mb chip. The size of the MTJ bits is 80–90nm with an aspect ratio of 2 and 3. An MgO barrier was used and MTJs with a TMR ratio above 110% were exploited. The chip is able to operate within a broad temperature range.

Switching the magnetization can occur spontaneously due to thermal fluctuations. This is an undesired event, which leads to the loss of the stored information. An important parameter of MRAM is the thermal stability

factor which is defined as the ratio of the thermal stability barrier to the operating temperature. For gigabit applications the thermal stability barrier should be at least 80kT to guarantee the required retention time of 10 years. Achieving large thermal stability and a low switching current for fast switching simultaneously represents one of the main challenges to engineer a good MRAM cell. Perpendicular MTJs (p-MTJs) with the thermal barrier equal to the switching barrier are preferred for applications, because they allow to reduce the switching current. In addition, p-MTJs are better suited for high-density memory [39].

Both field-induced and STT switching can be complemented with heat assisted switching [30]. This technology was routinely used in hard drives in order to facilitate writing. Presently methods using thermally assisted switching in MRAM have already been developed. In addition to assisting switching, heat can facilitate new unique functionalities, for instance, using an MRAM cell with a soft reference layer as a magnetic logic unit [40]. This extends the MRAM research and development area towards logic-in-memory architectures and non-volatile computing.

Regardless of the undisputable success of the first MRAM products on the market, several important challenges remain. The general requirements for any memory type including MRAM are:

- ability to write the data with low energy without damaging the device;
- data retention within a given long time interval;
- ability to read the recorded data without destroying the data.

Improving one or two aspects of its functionality usually leads to a degradation of the remaining functionality [30]. Therefore, a careful parameter optimization specific to a particular technology is the main subject which must be addressed in order to facilitate production of high density memory arrays suitable for replacing SRAM caches and DRAM-embedded main computer memory.

One of the main problems of STT MRAM is a relatively high critical current required for STT-induced magnetization switching. This fact has several implications. Firstly, due to the relatively high energy required for writing, the current generation of STT MRAM cannot be used in high-level processor caches due to the high activity factor in these elements and the high level of generated heat. The necessity to switch memory frequently negates the benefits of non-volatility provided by MRAM. Secondly, large switching currents are supplied via an access transistor. This potentially puts scaling limitations on the transistor dimensions of a one-transistor (1T)-1MTJ memory cell. However, a careful and innovative design yielded already a successful implementation of 8Mb 1T-1MTJ STT MRAM embedded in a 28nm CMOS logic platform [41]. Finally, a large switching current density can result in serious reliability issues like MTJ's resistance drift and eventually its dielectric breakdown. The critical current density depends on the switching pulse duration, with a substantial current increase for faster, sub 10ns switching. A plausible way to reduce the switching current density is to work with p-MTJs.

The problem of data retention is related to thermally agitated magnetization fluctuations. During these fluctuations the magnetization can switch spontaneously via a potential barrier separating the two states with opposite magnetization directions. As already noted, for about 10 years data retention the thermal stability barrier must be at least 80kT for gigabit MRAM arrays. However, increasing the barrier also results in an increase of the switching current density, which is proportional to the thermal barrier for p-MTJs. In order to reduce the switching current density and preserve the large thermal barrier at the same time one has to reduce the Gilbert damping and increase the spin current polarization. An interface-induced p-MTJ structure with a composite free layer CoFeB/Ta/CoFeB with two MgO interfaces [42] allows simultaneously boosting the thermal barriers and reducing damping.

For in-plane MTJs, the faster switching can also be achieved, when the composite free layer is made of two half-ellipses separated by a narrow gap. The peculiarities of the magnetization dynamics of the two parts of the composite free layer [43,44], which occur in opposite senses to each other, lead to the magnetization switching in-plane. This way the large demagnetization penalty of the magnetization getting out of plane is avoided, and the switching barrier becomes equal to the thermal barrier. Because the thermal barrier depends on the free layer volume, the required large thermal stability factors of ~80kT are easily achieved in this structure.

A large TMR ratio is needed for reliably reading the information in MRAM. Indeed, the middle reference resistance to which the low and high resistance MTJ states are compared must be well separated from either of them. However, since a bit-to-bit resistance variation within a memory array is increasingly difficult to control with device sizes scaling down, the dispersion increases and so must the TMR. Obtaining a large TMR is more difficult in interface-induced p-MTJs, because the layer width must be reduced in order to boost the magnetic anisotropy; however, a TMR ratio as large as 350% has been demonstrated [45].

With growing data services such as Big Data analysis the need for additional memory capacity and speed as well as in-memory computing has increased dramatically. The last-level cache memory must be increased [46-48] to bridge the memory-bandwidth gap between central processing units (CPUs) and the main memory. The CPU performance can be significantly boosted by using fast non-volatile memories in cache for data storing without the need to address the main memory.

In particular, the use of STT MRAM as the last-level cache memory helps bridging the memory-bandwidth gap between multi-core CPUs and the main memory. Ultra-large volatile DRAM devices are available; however, due to the high refresh rate and thus high power consumption their use as last-level caches has been limited. The introduction of non-volatility to reduce energy consumption in last-level cache memory can increase the CPU performance significantly by using this cache for data storing and processing without the need to address the main memory.

Advanced STT MRAM is characterized by high-speed access with less than 10ns. It is thus suitable for last-level cashes where it guarantees about ten times power reduction [49-51], while other types of non-volatile memories are much slower and cannot provide such a high speed access. 4Gbit density STT MRAM arrays with p-MTJs and compact memory cell were recently reported [39]. On May 26th, 2017, Samsung [52] reaffirmed the beginning of production of embedded STT MRAM based on the 28nm silicon-on-insulator technology node [41] in 2018. On September 15th, 2017, Globalfoundries announced the beginning of embedded STT MRAM production based on the 22nm fully-depleted silicon-on-insulator technology [53]. We are therefore witnessing the beginning of non-volatile STT MRAM entering the DRAM and potentially SRAM markets, traditionally dominated by CMOS-based volatile devices. If successful, it will result in an exponential expansion of the STT MRAM market with a momentous impact on information storage and processing in the near future.

3.2 Advanced MRAM

Although STT MRAM is competitive with DRAM for embedded memory applications and can also be used in level three caches in CPUs, increasing write currents for faster switching prevents it from being used in level one caches, where very fast switching is required. An ultimate swap to p-MTJs and Gilbert damping reduction are two common paths to reduce the switching current; however, these efforts are counteracted by the necessity to maintain high thermal stability which requires high perpendicular magnetic anisotropy [30].

There are indications that by downscaling the p-MTJ diameter the switching current decreases faster than the thermal stability factor, which has been shown to be as high as 120 in p-MTJs with a diameter of 30nm [54]. Nevertheless, it is preferred to have an alternative way to switch the free layer.

Interface-induced perpendicular magnetic anisotropy materials provide a sufficiently large thermal stability factor for free layers with diameters down to 12-14nm. Since the anisotropy is determined by the interface properties, it can be altered by applying an electric field. The electric field polarizes the charge densities of the interfacial atoms, thereby modifying overlap integrals and exchange interactions. This may soften the perpendicular magnetic anisotropy thus reducing the switching energy barrier and even changing it to in-plane. The magnetization can easily be pushed over the barrier by a small current and stabilized in the state with an opposite magnetization after the voltage is removed.

3.2.1 Voltage-controlled MRAM

An MRAM controlled by voltage [55-58] is a viable option for last-level cache applications. The voltage-controlled MRAM switching principle is based on voltage-mediated removal of the potential barrier separating the two stable magnetization orientation states. Without the barrier the magnetization precesses around the effective magnetic field and can be put into the alternative magnetization state, when the potential barrier is re-introduced at the end of the voltage pulse [59].

Because the voltage-induced switching is unipolar, the voltage controlled MRAM is free from the read disturb which is characteristic to STT MRAM. Although voltage controlled MRAM is a two-terminal device, the separation between read and write is performed by alternating the polarities during these two operations.

Voltage controlled MRAM has a few unsolved issues so far preventing it from being broadly used in applications. One of the problems originates in the precession at switching and thus depends on the initial state determined by the fluctuating thermal and unwanted variability. This variability results in write errors and must be suppressed.

The second problem is a larger resistance of the memory cell compared to STT MRAM, which results in smaller currents. Small currents lead to a longer delay while reading the state by a sense amplifier. As it was shown recently [60], both problems can be solved by carefully tailoring and optimizing the entire circuit.

Extending the ideas of voltage-controlled magnetic anisotropy, the voltage pulse can be applied not only to lower the potential barrier between the two magnetization states but also to boost it to make the switching harder [60]. The switching is mediated by a spin-orbit and/or spin Hall torque generated by the current flowing through a conductive line made of a heavy metal underneath the magnetic MTJ, ensuring the write operation without an external magnetic field [61]. If reading is performed by applying the voltage pulse with its polarity opposite to that used for writing, the potential barrier is increased, hardening the cell immunity against read disturb errors.

3.2.2 Spin-orbit torque MRAM

Among the newly discovered physical phenomena suitable for next-generation MRAM are the spin Hall effect and the spin-orbit torque (SOT) switching [62-66]. Current passing in a material with a high spin Hall angle/SOI results in spin-orbit torques capable to switch the free layer of an MTJ. This way the read and write currents are decoupled, which prevents the tunnel barrier from damage and improves device reliability.

The spin Hall effect and/or SOT alone do not provide switching in devices with perpendicular magnetization. To provide switching, it is required to apply an external magnetic field. In addition, innovative materials are required to increase the torques and to boost the switching efficiency. New materials with a strong SOI, e.g., topological insulators, allow the current to flow only at their interface states [67]. Due to the spin-momentum locking characteristic to these states the passing current results in a large spin accumulation at the interface [68,69] and the SOT aids the magnetization to switch.

A potential disadvantage of the write and read current paths' separation is that these devices appear in a three-terminal cell configuration [70]. Therefore, they can be used only for applications in which the density is not the top priority, but for high-speed reliable operation competing with SRAM.

There exists a different design of a three-terminal MRAM cell, where the switching is done by the current induced fast domain wall motion within a ferromagnetic material between the two ferromagnetic electrodes, while reading is done by means of an additional ferromagnetic contact grown on top of the ferromagnetic layer [70]. The domain wall is pushed by both STT and spin SOT, with the relative strength of each contribution tuned by proper engineering the magnetic layer structure. The domain walls can be moved very fast [71,72], which is attractive for high speed applications. However, the critical current densities obtained experimentally are still high. A reduction of the critical currents by minimizing the domain wall pinning in domain wall MRAM may compromise the data retention. Similar to SOT-based MRAM, the reduction of the current density, while maintaining the domain wall speed, remains a critical challenge for domain wall motion based MRAM.

The need to lower the critical current in advanced MRAM accelerates the search for new materials with large SOI. A promising candidate for such a material is a topological insulator, for which a large spin Hall angle has been demonstrated [67]. A general form of the relevant torque terms in the presence of spin-orbit interaction can be determined by symmetry considerations [73,74]. As SOTs appear at the interface between a material with high SOI and a ferromagnet, a description of these torques by means of boundary conditions was recently suggested [75,76]. The corresponding boundary conditions allow to relate the non-equilibrium spin accumulation at both sides of the interface in presence of the in-plane current and couple them to the magnetization dynamics.

4 Non-volatile logic

MRAM is CMOS compatible and attractive to use with CMOS-based logic applications. Fast non-volatile memory combined with non-volatile processing elements is a fertile ground for realizing the first microprocessors with reduced power consumption working on an entirely new principle. In addition, MRAM arrays are embedded directly on top of CMOS logic [77]. This allows reducing the length of interconnects and the corresponding delay time.

4.1 CMOS-MRAM hybrid logic

The computer architecture where non-volatile elements are located on a chip with CMOS devices is traditionally called logic-in-memory, although as of yet no information is processed in non-volatile elements. Power-efficient MRAM-based logic-in-memory concepts have already been demonstrated [78]. They include field-programmable gate arrays and ternary content addressable memory as well as other variants. These CMOS/spintronic hybrid solutions are already competitive in comparison to the conventional CMOS technology with respect to power consumption and speed.

The power consumption problem in modern integrated circuits with ultra-scaled CMOS devices is becoming critical, which prompts various power reduction technologies to be used for keeping the heat dissipation

under control. The techniques based on reduced voltage operation, clock gating, and power gating modes allow to address the problem to a certain extent, however, they also result in an increase of the time delay to get into or out from these modes. The use of non-volatile MRAM-based devices [79-81] with fast access to the stored data allows cutting out the penalty of stand-by power and eliminates the delays when using energy saving modes. The first microcontroller unit with zero standby power featuring non-volatile elements is operating at 8MHz [82]. In order to boost the operating frequency, spin-based non-volatile flip-flops were recently used to demonstrate a power-gating microcontroller unit [78] fabricated with standard 90nm CMOS technology with an additional MTJ process. The chip features a very short delay in entering/exiting power-on/power-off with the potential to be further reduced by optimizing parasitic capacitances.

Another new circuit example is a field programmable gate array built with non-volatile devices. Here, temporal data is quickly saved in magnetic tunnel junctions before the power is turned off. This has a great potential to reduce the power consumption, which becomes a critical issue in conventional SRAM-based gate arrays [83-85]. By using a logic-in-memory structure [86,87], replacing SRAM cells with non-volatile flip-flops [88] and smartly connected redundant MTJs to avoid resistance variations [89], the area of a six-input look-up table is shown to be reduced by about 50% [78].

Ternary content-addressable memory (TCAM) is able to perform a very high-speed search to match an input [90]. CMOS-based TCAM suffers from standby power losses and relatively high costs due to its complex structure [90]. Employing a 2T-2MTJ structure for the equality search logic part reduces the TCAM cell area [91,92]. A 1Mb non-volatile TCAM chip with a 6T-2MTJ cell structure fabricated in 90nm CMOS and perpendicular MTJ technologies has been demonstrated [93], with 9T-2MTJ [94], 7T-2MTJ [95], 4T-2MTJ [96], and 5T-4MTJ [97] modifications for high-speed accessibility and reduced variation effects have been also reported. Currently, the TCAM cell structure design as well as the word segmentation algorithm optimization is under intense investigation [78] in order to increase speed and reduce the area.

With the continued rapid development of smartphones and mobile video applications it becomes necessary to introduce non-volatile elements into important circuits responsible for performance acceleration. A motion-vector prediction circuit is critical for performing mobile video compression by finding motion vectors between two adjacent frames. It has been demonstrated that the introduction of non-volatile elements to implement a full adder helps making the circuit compact, fast, and stable [98-102]. The introduction of non-volatility and a logic-in-memory architecture helps reduce power consumption by 45% [103]. With the activation ratio of embedded clusters decreased a reduction of 97% is possible [78]. Another example of an application specific circuit currently under thorough investigation is a brain-inspired computing network with non-volatile elements, which also demonstrates a large, i.e., more than 90%, power reduction on average when compared to its CMOS based counterparts [78].

4.2 Intrinsic logic-in-memory

The current age of Big Data requires an unprecedented level of data storage capacity complemented with efficient processing capabilities. The data processing is typically confined in large data centers, which appears to customers as a cloud computing environment to enable resource flexibility. The scale of data centers (and their power consumption) is increasing exponentially. One of the limitations of current computing systems is the overhead of transferring data between memory and processors. As already mentioned, the problem can be solved by placing the main memory closer to processors. Another efficient solution will be to perform at least part of the data processing already in the storage by designing a memory architecture with enhanced functionalities capable to directly perform a set of Big Data-oriented, memory-centric operations. This methodology promises a dramatic reduction in the need for data transfers between memory and processor, eliminating the interconnection bottleneck, by creating a new high performance and low power efficient computing paradigm, where the data is not only stored but also analyzed by non-volatile stand-by-power free processing units.

Placing the actual computation into the magnetic domain reduces the need of converting magnetically stored information into currents and voltages for processing and helps not only to simplify the circuit layout but also increases the integration density. The idea is to use MTJs as elementary blocks for non-conventional logic-in-memory architectures. Our invention, which shows that on an MRAM array any two of the coupled 1T-1MTJ cells can serve simultaneously as non-volatile memory and computing units by performing a logical implication operation, has been granted a patent [104]. These structures inherently realize non-volatile logic-in-memory circuits with zero-standby power, where the same elements are used for storing and also processing information. They have a great potential for Big Data storing and computing, as they are also opening a path for developing computing architectures conceptually different from the still standard Von Neumann architecture. A new design of an implication-based full

adder involves six 1T-1MTJ cells with 27 subsequent FALSE and material implication operations [105].

The paradigm of employing memory for information processing is perfectly suited for the Big Data revolution we are experiencing now by providing computation capabilities within memory itself, thus eliminating the need for data communication between memory and the processor. However, precisely because of the absence of a clear division between memory and the computing unit this intrinsic logic-in-memory architecture is completely different from the Von Neumann architecture currently employed, and a development of a conceptually new calculation paradigm using this architecture is needed.

An alternative option is to follow a more conventional path with memory and computing units separated, where, however, both elements are non-volatile and implemented in a magnetic domain. Placing the actual computation into the magnetic domain reduces the need of converting magnetically stored information into the currents and voltages for processing. It also simplifies the circuit layout and boosts the integration density. The idea of combining MTJs with a common free layer enables the realization of an efficient nanooscillator [106] and a non-volatile magnetic flip-flop [107]. The computation unit is represented by the STT based non-volatile majority gate, with non-volatile magnetic flip-flops [107] used as memory registers. Because all the data processing elements are performed in the magnetization domain, the flip-flops could be put at the legs of the majority gates thus removing the need of data transfer and interconnects between the processing unit and memory. By using the non-volatile computation unit the realization of a 1-bit full adder in magnetic domain is demonstrated [108].

Finally, we mention a completely different neural network based approach to calculations. Non-volatile MTJs fit for neural network realizations as they can be considered as a current-driven programmable resistor – memristor – and they significantly advance programming and storage functions. MTJ based neural networks have been demonstrated featuring non-volatile synapses [109] for high-speed pattern recognition with about 70% reduction of gate count and 99% improvement in speed. Neuromorphic computing is becoming a reality, with the first self-learning chip revealed on September 25th, 2017 by Intel [110].

5 Conclusions

Spin transistors have been recently successfully demonstrated, however, an enhancement of the on-current ratio between the parallel and anti-parallel source/drain magnetization configuration at room temperature remains one of the main challenges. As both Spin-FET and SpinMOSFET still rely on the charge current to transfer the spin, it sets limitations for the applicability of such devices in main-stream microelectronics, and new ideas are needed for the future.

Non-volatile devices based on MTJs possess a TMR suitable for practical applications. Several companies announced embedded STT MRAM production in 2018. Although STT MRAM is positioned as a successor not only for flash, but also for CMOS-based main computer memory, the relatively high switching current and power may confine STT-MRAM to replacing flash memory in data-intensive and low-power mobile, automotive, or Internet of Things applications. Because of the large switching currents and insufficient speed, STT-MRAM is unlikely to replace SRAM in high-level core caches. Novel innovative non-volatile devices with improved switching characteristics and low power consumption are required for processor-embedded memories.

Finally, the successful adoption of non-volatility in microelectronic systems by developing various logic-in-memory architectures and in-memory processing will inevitably result in increasing disseminations of this technology for other applications such as ultra-low-power electronics, high-performance computing, the Internet of Things, and Big Data analysis.

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7 References

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