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CMOS RGB Colour Sensor with a Dark Current Compensation Circuit

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Abstract: This article presents the design and development of a Red, Green, Blue (RGB) Colour Sensor with a dark current compensation circuit. The presented design employs a new approach to eliminate the conventional low pass filter, where it is normally required to integrate the pulsating signal. This is accomplished by employing switched capacitor circuit techniques. A covered photodiode is used to derive a proportional to dark current common mode voltage or compensated common mode voltage, Vdvcm. The measured performance of the sensor when it was used as an optical feedback solution for a light emitting diode (LED) backlighting system was very promising. The colour point accuracy, $\Delta u'v'$ = 0.002, while colour point drift over temperature was less than 0.008 at 50 °C. The maximum reduction of 36 mV output voltage error was observed when the Vdvcm was applied to the single to differential circuit. The overall power consumption of the fabricated sensor was 7.8 mW. The whole sensor design was implemented in 0.35 µm CMOS technology. The Vdvcm concept can be applied to other similar circuitry such as temperature-sensitive circuits.

Keywords: Integrated Circuit; RGB Sensor; Current Integration; dark current cancellation

CMOS RGB barvni sensor s kompenzacijskim vezjem temnega toka

Izvleček: Članek predstavlja obliko in razvoj RGB senzorja s kompenzacijskim vezjem temnega toka. Predstavljen dizajn, za eliminacijo pulzirajočega signala ne uporablja klasični nizkopasovni filter temveč tehniko preklopnega kapacitivnega vezja. Za določitev razmerja sofazne napetosti temnega toka ali kompenzirane sofazne napetosti je uporabljena fotofioda. Merjene lastnosti senzorja v uporabi povratne informacije LED sistema so zelo vzpodbudne. Natančnost barvne točke pri temperaturnem driftu pod 0.008 pri 50 °C je $\Delta u'v'$ = 0.002. Največje zmanjšanje izhodne napetosti je 36 mV. Senzor je izveden v 0.35 µm CMOS tehnologiji.

Ključne besede: integrirana vezja; RGB senzor; izničenje temnega

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1 Introduction

There are numerous applications of colour sensors in consumer application industries. Such applications are reflective colour sensing [1] and an optical feedback for RGB light source [2-4]. The latter application requires the system to maintain a given colour of the LEDs over temperature and time. Selecting the colour can be accomplished by specifying the colour coordinates in the CIE colour space. This is achieved via colour coordinate feedback (CCFB) technique.

An example of optical feedback solution [2] required a low pass filter (LPF), a gain stage, an analogue digital converter (ADC) and external RGB sensor. The solution is therefore unacceptable for small or portable devices which require a small footprint [3-5]. The LPF was used to average out pulse width modulation (PWM) voltage can have an effect on the response time of the total solution. Several digital colour sensors which employ light to frequency technique [6, 7] require an advanced processor such as DSP or PC to measure or calculate the frequency [8, 9].

Dark current can be caused mainly by the random movement of carriers (solely on carrier concentration) and the thermal generation combination. Dark current can affect the dynamic range [10, 11] of CMOS image sensors. It is also a subject of study in colour sensors [6] and photodetectors [12].

Reduction of dark current can increase the dynamic range of colour sensors [7]. Two approaches to reduce the dark current, namely through photodetector (photogate) physical modification [13] and secondly through electronic correction, are normally employed in a low dark current colour sensor. The latter approach was a circuit-based approach and it required a dummy photodetector. The real photo current is a result of the subtraction of active current from the photodetector and dark current from the shielded dummy photodetector [7, 14]. The photogate technique [13] required different biasing voltages; therefore, it is quite difficult to be implemented in small colour sensor design. The problem with the shielded dummy approach is that the biased voltage of the shielded photodetector differs from the one applied to the main photodetector. Recent work [15] had improved the work based on the subtraction technique [14]. An integration capacitor is usually used to store voltage, so the leakage due to switching and others has to be reduced in order not to affect the voltage stored in the integration capacitor. Another approach which was based on 'stored' voltage for biasing the current mirror or current source had been developed. This work was based on current steering of dark current to the ground instead of to the output [16]. This work however was prone to device mismatch.

Recent works [17,-19] which are based on the integrating current concept has managed to integrate ADC, RGB sensors and the function of the low pass filter (LPF) and gain stage. The works had eliminated the conventional LPF by employing an integration capacitor (C_{int}). The gain stage was also eliminated by using selectable capacitors and photodiode sizes, but the gain function remains the same. Nevertheless, the works [17], [19] did not employ a dark current cancellation circuit and the measured dark current is within 1 LSB [19]). The dark current limits the signal to noise ratio for sensors operating at high temperature or under low light conditions where the integration time is long.

The objective of this work was to solve the dark current issue in the recent CMOS colour or RGB sensor [17, 19] and improve dark current cancellation work [18]. The solution was not obvious, as either the differential transimpedance amplifier (TIA) or zero biasing technique cannot be employed in the design. The dark current cannot be cancelled at the digital level due to different sampling or integration time issues. An example of the application such as backlighting will also be presented.

This paper is organized as follows. Section 2 discusses the design aspect. It covers backlighting application, concepts, control signals, RGB Photodiode, Integrator (Switches and Capacitor array), dark current cancellation, a single to differential circuit and sample/hold (S/H) buffer amplifier and process, voltage and temperature (PVT) corners analysis. Sensor development and measurement results are discussed in section 3. This paper is concluded in the conclusion section.

2 Design

2.1 Backlighting application

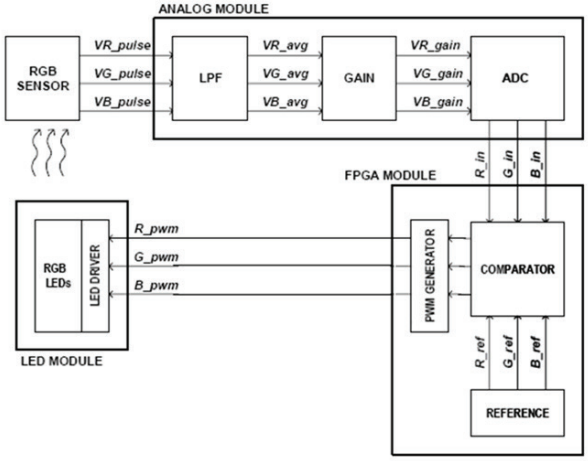

Figure 1: A typical Block diagram LED backlighting solution using optical feedback [2, 20]

The block diagram of the optical feedback system employed in RGB LEDs backlighting is shown in Figure 1. The general flow is as follows: The RGB sensor which is a colour sensor measures the intensity of each colour produced by the LED module. The low-pass filter (LPF) (in this solution only one low pass filter is used) averages the sensor voltage output over time before transferring it to an adjustable gain stage (the objective is to obtain the maximum analogue to digital converter (ADC) code when the LED is at full brightness). The ADC digitizes the averaged sensor voltage and the feedback controller (inside the FPGA) adjusts the PWM output according to the deviation of the measured sensor data from the reference values. The PWM signals are used to drive the external LED drivers, which control the on-time duration of the red, green and blue LEDs. The on-time duration is continually adjusted in real time to match the light output from the LED array to the RGB ratio needed to maintain the specified colour [2]. This measured condition-digitize-adjust is a free running process. A more detailed explanation can be found in Lim *et al.* [2]

2.2 Colour sensor concept overview

The proposed design as shown in Figure 2 is an improved version based on previous works [17 – 19]. It

receives signals from the photodiode array, a programmable setting can be applied to the signals, and it then converts the resulting differential voltage signal into digital words. The programmable settings are integration period, capacitor size and photodiode active area size. The design can sense pulsating light without the need of a filter. This is because the design works on the principle of integrating photodiode current.

Five major blocks are shown in Figure 2: test multiplexer (TEST_MUX), REFERENCE, ADC, TIMING GENERATOR and integrator and sample & hold (INTEG S&H). The TIMING GENERATOR is used to derive the required control signals (see Figure 3). INTGR and PRECHARGE SIGNALS are the inputs to the TIMING GENERATOR. The INTEG S&H block is the point of interest and will be explained in detail in this paper. Photomux shown in Figure 2 is a simplified idea; its function is to select the photodiode active area and channel or colour. Each switch for CHSEL [2:0] consists of three switches for colour selection (RGB). The integration of photo current is accomplished by using an array of capacitors, called integration capacitor, C_{int}, so together with switches (transistor symbol), it forms an integrator.

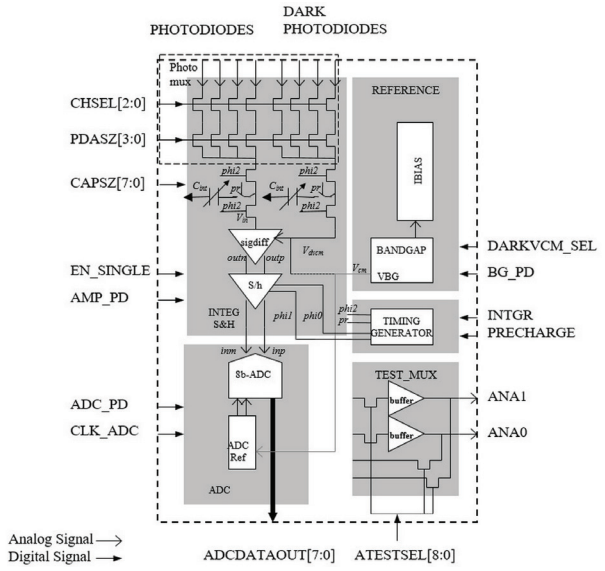

Figure 2: Block Diagram of a novel RGB colour sensor

Table 1 describes the description of the I/O of the proposed design.

Table 1: Pin List

Name	Type	Description
VDDA	P	Analog supply. Nominal 2.6V.
VSSA	P	Analog ground.
PDASZ[3:0]	DI	Photodiode size
CAPSZ[7:0]	DI	Capacitor select.
CHSEL[2:0]	DI	Channel select.
INTGR	DI	Integrating control signal
PRECHARGE	DI	Precharge control signal
EN_SINGLE	DI	Select 7 bit mode (active high)
CLK_ADC	DI	ADC clock
ADC_PD	DI	ADC power down pin (active high)
AMP_PD	DI	Amplifier power down (active high)
BG_PD	DI	Bandgap power down (active high)
DARKVCM_SEL	DI	Select normal V_{cm} (active high)
ATESTSEL[8:0]	DI	Analog test control signal (TSTMUX)
Photodiode pins	ANA	Photodiode connection
ANA1	ANA	TEST PIN1
ANA0	ANA	TEST PIN2.
ADCDATAOUT[7:0]	D0	ADC data out

The simplified integrator output, V_{in} is:

$$V_{in} = V_{prech\arg e} - \frac{I_{photodiode} \times T_{\text{int}egration}}{C_{\text{int}}} \quad (1)$$

where $V_{precharge}$ is the voltage across integration capacitor, C_{int}. The voltage is provided by the REFERENCE block. $I_{photodiode}$ is the photocurrent and $T_{integration}$ is the integration time.

From equation (1), when the light incident on the photodiode is PWM light, the integration phase (see Figure 3) is synchronized to a multiple of the PWM periods, then the voltage V_{in} is inversely proportional to the PWM duty cycle. A single to differential amplifier (sigdiff) is then used to produce the differential voltages for the differential input ADC; these values are later sampled by the S/H amplifier. In the single to differential circuit (*sigdiff)*, a compensated common mode voltage is used for dark current cancellation. The sampled values are held for analogue to digital conversion. At the same time, the C_{int} is charged back to the $V_{precharge}$ value. Details about integrator and sample hold (INTEG S&H) are discussed in Sections 2.5, 2.6, 2.7 and 2.8. A pipeline ADC with 8-bit resolution is used for analogue to digital conversion. The ADC can receive ± 1.2 V, i.e. differential input voltages with the nominal voltage (common mode voltage) of 1.2 V. The relationship of voltages and the ADC output is described in equation (2):

$$\text{ADC Output (DEC)} = \left(\frac{(inp\text{-}inm) + V_{ref}}{2V_{ref}} \right) \times 256 \qquad (2)$$

where *inp* is the positive input of the ADC, *inm* is the negative input of the ADC and V_{ref} is the reference voltage. For output of 0 DEC, the differential voltage is -1.2 V (e.g. inp = 0. 6 V, inm = 1.8 V) while for output 256 DEC (2^8), the differential voltage is 1.2 V.

Both equations (1) and (2) show that the concept is capable of integrating several functions (gain stage and LPF) into a single silicon. The REFERENCE block is used to generate bias voltages (e.g. VBG or V_{cm}) and bias currents for internal usage such as voltage to precharge the C_{int}. The design also includes extensive routing for testability. Each block's input can be overridden and each block's output can be measured. This allows an efficient means of debugging the signal chain within the design should the need arise.

2.3. Control signal

Figure 3 shows the simplified proposed control signal for the INTEG S&H block. 'pr' is the precharge control signal and 'phi2' is the signal to control the integrator switch (see Figure 5). 'phi0' and 'phi1' are signals to control the S/H buffer amplifier (see Figure 9). These signals are depicted in Figure 2.

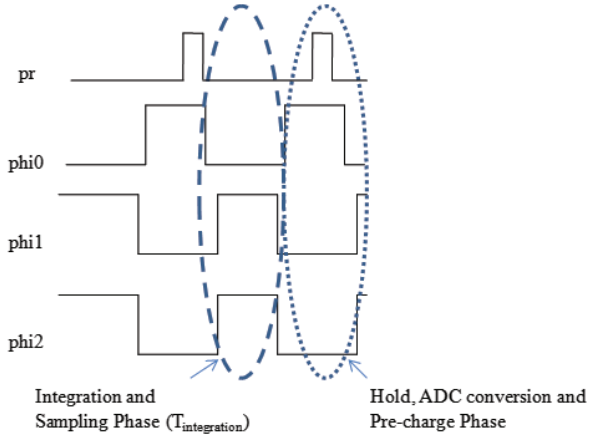

Figure 3: Control signals

2.4 RGB Photodiode

Figure 4 shows the RGB photodiodes. The RGB photodiodes are N-Well type photodiodes with colour photo array (CFA) filters [21], [22]. The RGB filters are arranged in a common centroid pattern. Photodiode sizes can be selected from ¼, ½, ¾, or full size. Light is converted to photocurrent by these photodiodes. An interface circuit called PhotoMux is designed to select photodiode sizes and channels (RGB). The total size of the RGB photodiodes is 400 µm × 400 µm.

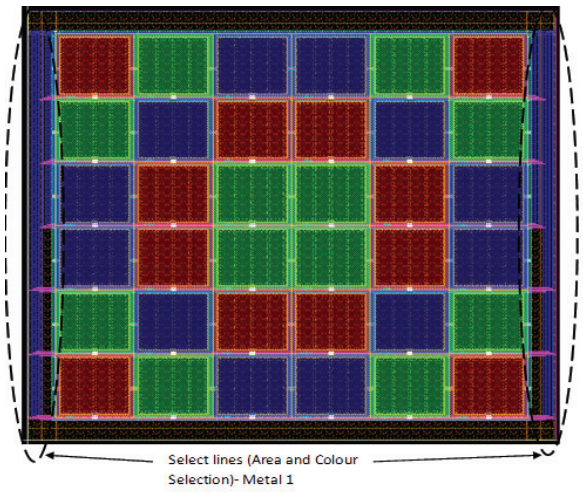

Figure 4: RGB Photodiodes

2.5 Integrator (Switches and capacitor array)

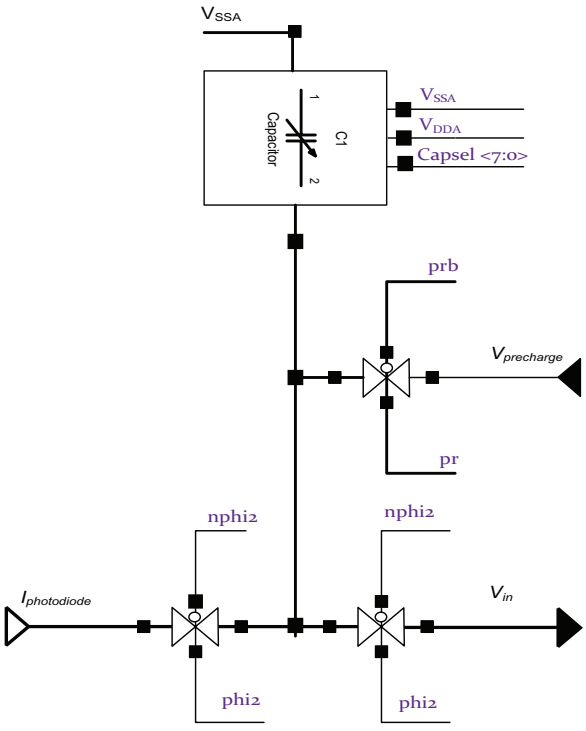

Figure 5: Switches and Capacitor Array (C_{int})

The integrator circuit in Figure 5 employs a capacitor array of 4x8 pF and switches. The value of the capacitance can be selected through the Capsel register. The capacitor block is pre-charged to ~1.8 V ($V_{precharge}$) when the 'pr' signal is high. Before the 'phi2' signal is high, the 'pr' signal is first low. The 'phi2' signal is high when integration is selected. During the integration period,

the pre-charged capacitor voltage starts to decrease as described by equation (1). The capacitor array together with photodiode sizes can be used to adjust the required V_{in}. This is similar to the gain stage function as in a prior work [2].

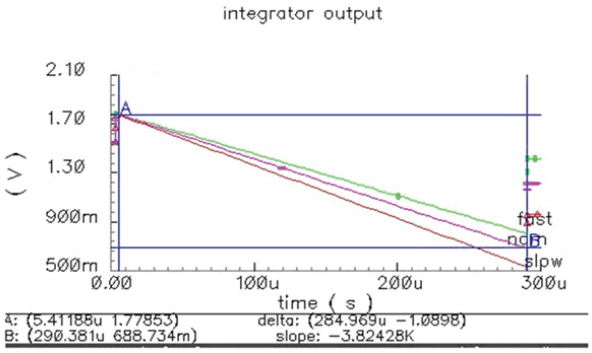

Figure 6: Integrator Output (V_{in}) Simulation at slow, fast and nominal corners

Figure 6 shows the integrator output simulation results; the simulated slope is 3824 V/s. The slope can be calculated based on equation (3):

$$I = C\frac{dV}{dT} \tag{3}$$

where *I* is the photodiode current, *C* represents the integration capacitor value and *dV/dT* is the slope. When all capacitors are selected (32 pF), the photodiode current (*I*) is 125 nA and using equation (3), the slope or *dV/dT* = 3906.25 V/s. The calculated slope is not very different compared to the simulated slope as shown in Figure 6. It is also shown that the capacitor corners (slow = minimum capacitance, fast = maximum capacitance) affect the slope more than transistor corners.

2.6 Dark current cancellation circuit concept

Figure 7 shows the dark current cancellation concept. Two operational amplifiers are used to create a single to differential circuit. The operational amplifier is based on the differential folded cascode amplifier, the concept of which is similar to a reported work [23]. Assuming no current into the negative terminal of the operational amplifier and V_{cm} is selected (DARKVCM_SEL = HI), current flowing into resistor, *R* is:

$$\frac{V_{cm} - V_{outp}}{R} = \frac{V_{outn} - V_{cm}}{R} \tag{4}$$

where V_{cm} is common mode voltage, V_{outp} is voltage of positive output, V_{outn} is voltage of negative output and R is resistor.

Re-arranging equation (4), $V_{outp} = 2V_{cm} - V_{outn}$, the differential output voltage, $V_{diff} = V_{outp} - V_{outn}$, since $V_{outn} = V_{in}$, V_{diff} is:

$$V_{diff} = 2V_{cm} - 2V_{outn} = 2V_{cm} - 2V_{\text{int}\,gr} \tag{5}$$

From equation (5), when V_{cm} is V_{dvcm}, theoretically the differential output voltage would be without a dark current element. This is firstly achieved by precharge an integration capacitor in the dark current circuit with V_{cm}. The stored voltage at the integration capacitor is discharged due to solely dark current. This voltage is now can be called V_{dvcm}. When DARKVCM_SEL is 0 V, the V_{dvcm} is applied to the operational amplifier and the dark current element from the uncovered photodiode can be eliminated. It is also easy to conclude that for the worst offset scenario of the single to differential amplifiers is:

$$V_{diff-offset} = 2V_{cm} + 4V_{offset} - 2V_{\text{int}\,gr} \tag{6}$$

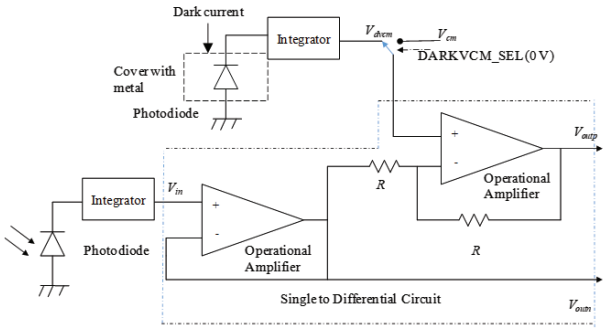

Figure 7: Dark Current Cancellation approach

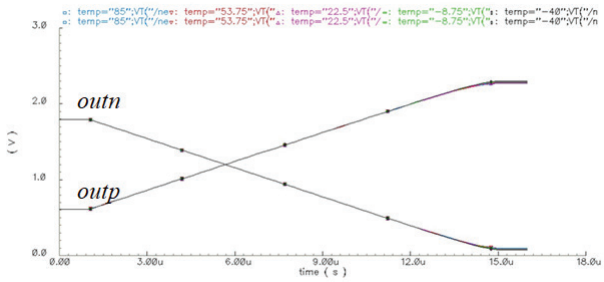

Figure 8: Non-Inverting Output (*outn*) and Inverting Output (*outp*)

The output of the non-inverting amplifier (*outn* = *inm* or input of ADC) will be cut-off at 100 mV as shown in Figure 8, which is due to the amplifier limitation. From equation (2), this corresponds to a maximum digital sensor output of 245 DEC when *outp* (equal to *inp*) is maintained at 1.2 V (a pseudo differential signal to ADC).

2.7 S/H Buffer amplifiers

An S/H buffer amplifier as shown in Figure 9 consists of an operational amplifier (Figure 10), two capacitors and switches. Bottom plate sampling is employed in the design in order to reduce the substrate noise [24].

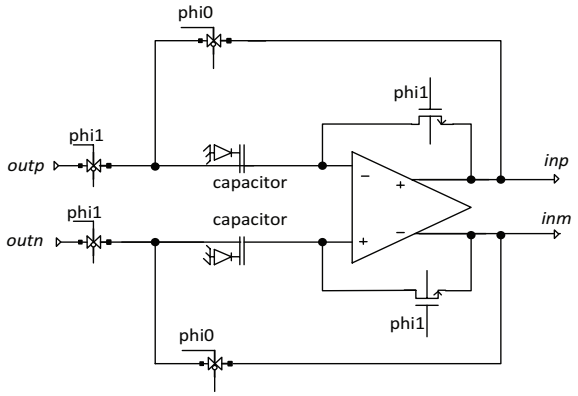

Figure 9: S/H buffer amplifier

The S/H buffer amplifier is used prior to the ADC block due to the ADC that is used in the colour sensor design is a free running ADC. Two capacitors with a value of 100 fF are used as the S/H capacitors. This value is optimized for low kT/C noise.

During the sampling ('phi0' is low) of the differential voltages, the output of the operational amplifier (as shown Figure 10) is shorted to its input and the DC voltage is set at V_{cm} by a common mode feedback circuit [25] in the operational amplifier. During the holding phase (phi1 is low) the output is shorted to the left/bottom plate of the S/H capacitor. By employing the common mode feedback circuit (CMFB), the output of this S/H buffer amplifier is always re-centred at V_{cm}. The CMFB employs the capacitive sensing technique. Two capacitors are used to average out the differential output voltage, the averaged output is connected to the CMFB amplifier input, the CMFB amplifier compares it with V_{cm} (connected to V_{ref}), and adjusts the biasing current until the averaged output is equal to V_{cm}. *ibias* is supplied by the bandgap circuit. V_{sample} is connected to phi1 while V_{hold} is connected to 'phi0'.

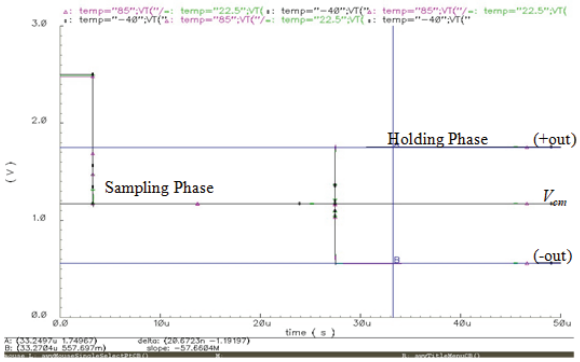

Figure 11: S/H buffer amplifier output at fast corner and vs. temperature

Figure 11 shows S/H buffer amplifier outputs during sampling and holding periods. During the sampling, both outputs are tied to V_{cm} and only during the hold-

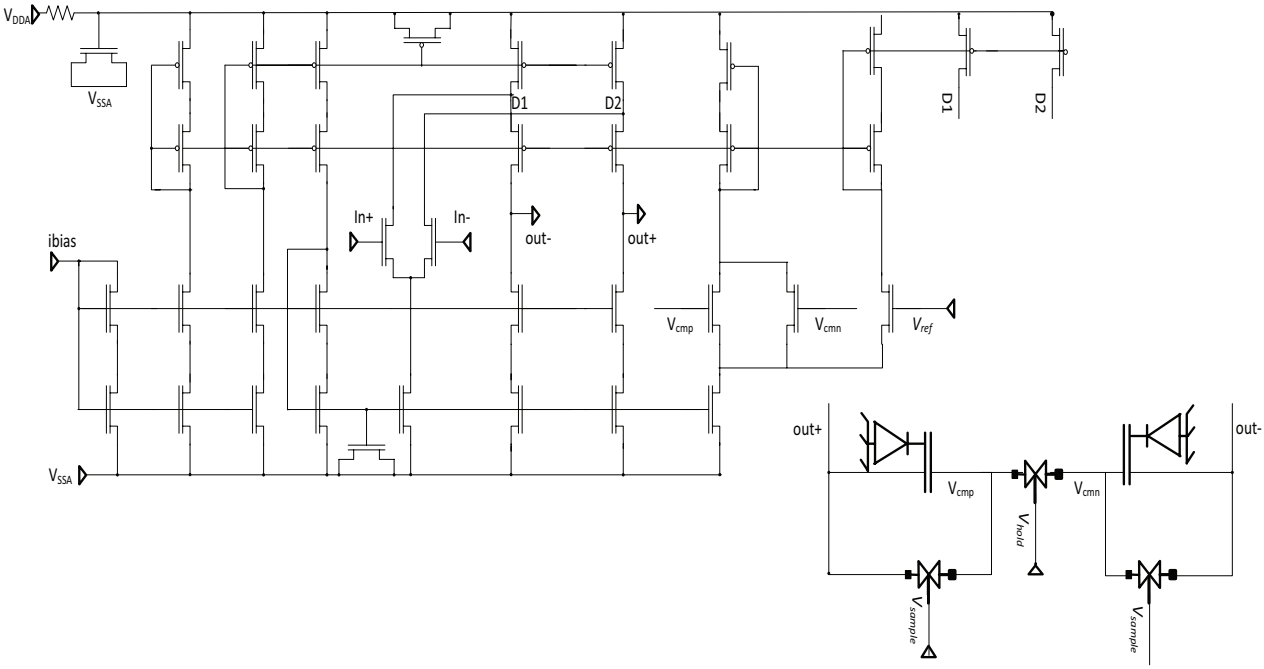

Figure 10: Differential input Operational Amplifier with the CMFB

Table 2: PVT Simulation of Sub-Blocks of INTEG S&H block

Parameter	PVT Min	PVT Nom	PVT Max	Units	Comments
Integrator output voltage	3415	3824	4349	dV/dt	Process variation
Single to differential output voltage			+2mV		From nominal differential signal
S&Hold buffer output voltage			3mV		Worst with Vdd variation

Note:
Temp= -40, 27, 85°C. FET= Fast, Slow, Nom. Resistor/Capacitor =MIN, NOM, MAX. VDD= 2.5, 2.6, 3.6 V. PVT Min = Slow, MAX, 2.5 V, 85°C corners. PVT Nom = Nom, NOM, 2.6 V, 27°C. PVT Max = Fast, MIN, 3.6 V, -40°C.

ing phase are the outputs connected to the sampled signals. Figure 11 also depicts the differential signal at an output of 1.19 V which is achieved whilst the common mode voltage is 1.19 V (V_{cm}). The S/H buffer amplifier seems immune to temperature variation (-40 °C, 22.5 °C, 85°C).

2.8 Process, voltage and temperature (PVT) corners analysis

Table 2 shows the summary of the PVT for the INTEG S& H block.

Table 3 shows the zero code calculation of pre-layout based on the output voltages of Single to differential amplifier and voltage references. The offset voltage of the amplifier is three times of PVT results as shown in Table 2.

Table 3: Zero Code Calculation based on Single to Differential Output

Parameters	Nom	Min	Max
VREFM (V)	0.602	0.57	0.619
Voffset (V)	0.006	0.006	0.006
VREFP (V)	1.750	1.727	1.773
Vcm (V)	1.167	1.151	1.178
Voutp (V)	0.602	0.593	0.601
Voutn (V)	1.744	1.721	1.767
Vref (VREFP- VREFM)	1.148	1.157	1.154
Vdiff-offset (V)	-1.142	-1.128	-1.166
Zero code (LSB)	~0	4	-2

Note: Equation 6 is used to calculate the $V_{diff\text{-}offset.}$ Equation 2 is used to calculate the zero code.

Table 4 shows the summary of the PVT zero code (photodiode current is zero) of post layout (extracted) complete design. At the PVT Nom, the design offset is at least 2 LSB. These offsets can be eliminated at the digital level.

Table 4: Zero Code Post layout Simulation of Complete Design

Parameter	PVT Min	PVT Nom	PVT Max
Integrator Output (V)	1.804	1.770	1.830
Output of single to differential amplifier (V)	1.175	1.179	1.147
Output of S/H buffer (V)	1.171	1.176	1.142
Non-overlapping-Clock, ph0-ph1 (ns)	7.85	4.15	2.94
Clock Delay, ph2-ph1 (ns)	2.83	0.9	1.06
Output ADC code	00000011	00000010	00001000

Note:
Temp= -40, 27, 85°C. FET= Fast, Slow, Nom. Resistor/Capacitor =MIN, NOM, MAX. VDD= 2.5, 2.6, 3.6 V. PVT Min = Slow, MAX, 2.5 V and 85°C corners. PVT Nom = Nom, NOM, 2.6 V, 27°C. PVT Max = Fast, MIN, 3.6 V and -40°C.

3 Sensor development and measurement results

3.1 CMOS Sensor implementation

Figure 12a shows the floor plan of the RGB colour sensor with a dark current cancellation block diagram. A Non-Overlap Block (TIMING GENERATOR) is used to generate 'phi0' and 'phi1' or 'phi2'. Biasing Circuitries (REFERENCE block) are used to provide necessary references such as *ibias*, bandgap voltage (VBG), current sources or sinks to the operational amplifiers and the ADC. VBG is a voltage reference based on bandgap voltage circuitry. The common mode voltage, V_{cm}, is based on this voltage reference. The total size of the basic core layout is 800 µm x 400 µm (without the RGB

photodiodes). Figure 12b shows the final layout of a RGB colour sensor with the dark current cancellation layout. TEST_MUX is not shown in the Figure 12a and Figure 12b. Decoupling capacitors, as shown in Figure 12b, are used to reduce noise from $V_{DD.}$ Figure 12c shows a picture of the fabricated sensor; all blocks or circuits (as in Figure 2) except the RGB photodiode are covered with a metal layer to protect them from light.

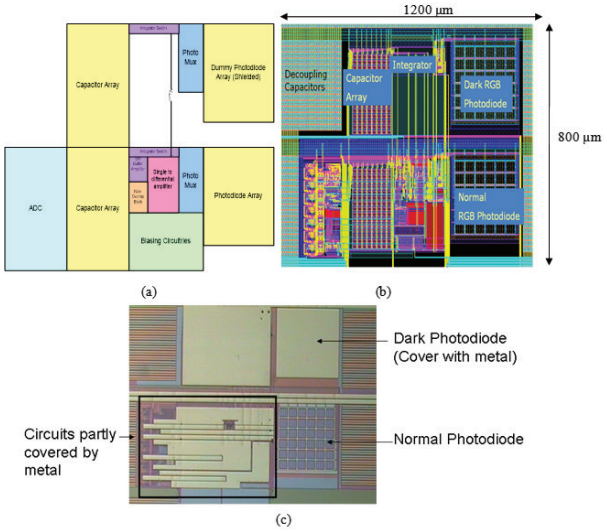

Figure 12: (a) Floor Plan of the novel CMOS RGB, (b) Layout of the implemented design, (c) Microphotograph of the novel CMOS RGB colour sensor with dark current cancellation

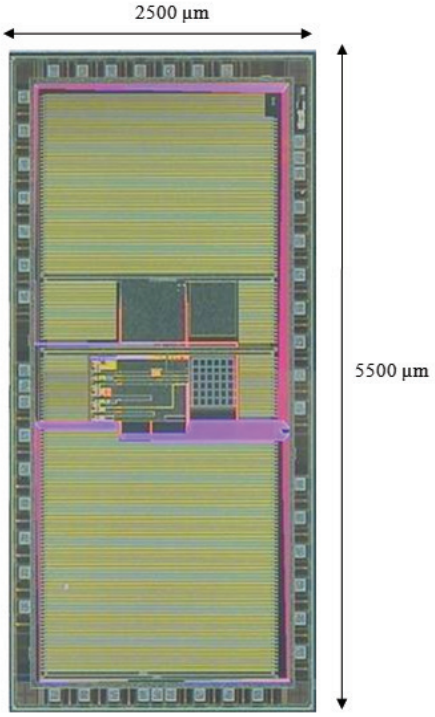

Figure 13: Microphotograph of the prototype CMOS RGB colour sensor with dark current cancellation and I/O pads

Figure 13 shows the complete prototype of the sensor with I/O bondpads. The prototype is I/O pad limited since the size is limited by the size of the I/O pad structure.

3.2 Test boards

Figure 14a shows the test system architecture for the sensor, while Figure 14a and 14b are the DUT board and Test Board respectively. The sensor was packaged in clear 48 pin TSOP and soldered onto the DUT board. Six voltage level shifter ICs (MAX 3001E) were used to connect the sensor and the PC/FPGA. These ICs were soldered onto the Test Board.

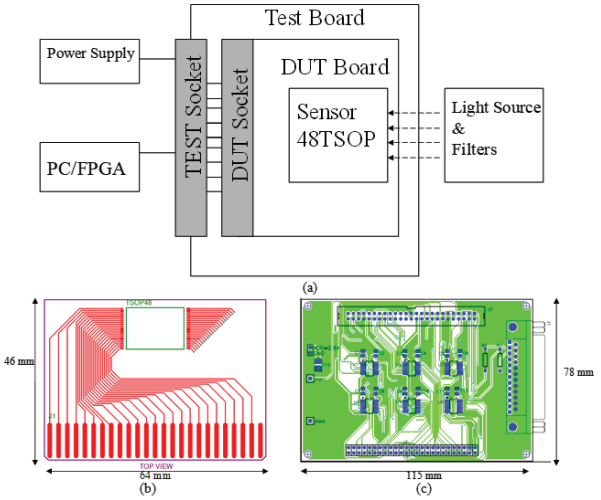

Figure 14: (a) Test System Architecture, (b) PCB drawing of the DUT board, (c) PCB drawing of the Test board

3.3 Measured colour sensor results

Table 5 shows the light intensity vs photodiode current.

Table 5: Light intensity vs photocurrent

Light intensity (lux)	Current (nA)
0	0.4
265	14
528	29
762	40
1049	55
1324	63
1583	78
1822	90

Note: Test condition: Red channel, VDD=2.6V, Integration time=150 µs, Photodiode size=400 µmx400 µm, room temp, C_{int} =32 pF

Table 6 shows the designed C_{int} value versus measured value. The value of smaller capacitors (4 pF and 8 pF), as shown in Table 6, were difficult to be realized, which could be due to a parasitic component associated with selection switches.

Table 6: Value of C_{int}

Designed value (pF)	Measured value (pF)
4	5.76
8	10.6
12	13.5
16	16.9
20	20.8
24	25.5
28	28.9
32	32.7

Table 7 shows the DC value of the voltage references (from biasing circuitries), VBG, VREFP, VREFM and total current consumption, ICC of the sensor across V_{DD} (power supply). The measured current consumption is very close to the simulated current consumption.

Table 7: Analog/bias parameters

	Simulation	Measurement		
	VDD(V)	VDD(V)		
	2.6	2.5	2.6	3.3
VBG(V)	1.167	1.171	1.183	1.171
VREFP(V)	1.750	1.757	1.76	1.75
VREFM(V)	0.602	0.624	0.63	0.617
ICC(mA)	2.856	~2	~3	~4

Based on Table 7, at nominal, the V_{cm} (which is VBG) is 1.183 V and V_{inm} (VREFP) is 1.76 V, and VREFP and VREFM are generated for ADC references. From Figure 7, V_{inp} (depicted as V_{outp} in the figure) is 0.624 V. Thus, using equation (6) and equation (2), the sensor offset is zero. This is agreed as shown in Table 3.

Figure 15 shows the ADC response or settling time (adacdataout<4>) which is 46 ns. The clock is at 4 MHz. The response indicates that the maximum ADC output frequency is approximately 21 MHz.

The results in Table 8 – Table 10 show that the sensor results agree with equations (1)-(3); hence, this has proven that the concept discussed in section 2.2 is fully functioning as designed. Out-V_{dvcm} is the sensor digital output when the V_{dvcm} is applied to the single to differential circuit. Out-V_{vcm} is the sensor digital output when the V_{vcm} is applied to the single to differential circuit. Table 8 also shows that the measured sensor offset is

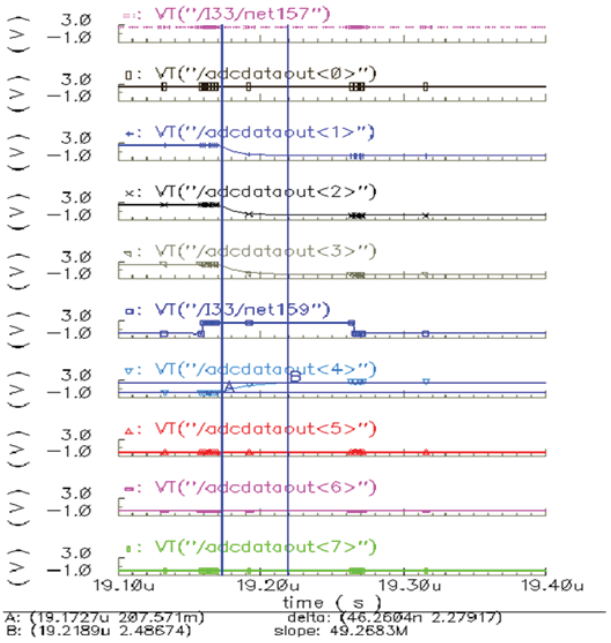

Figure 15: ADC response

similar to the post-layout simulation sensor offset, i.e. when V_{dvcm} is applied to the single to differential circuit.

Table 8: Digital CMOS sensor output vs integration time

	Integration time (unit)				
	0	4	8	12	15
Out-Vdvcm	1	12	23	32	40
Out-Vcm	2	13	23	34	41

Note:
Integration time of 0 = 150 µs.
Test condition: Red channel, VDD=2.6V, Photodiode size =100µmx400µm, C_{int}=32 pF, room temp, 150 lux.
V_{cm} = VBG, V_{dvcm} is V_{cm} generated from the dark photodiode.

Table 9: Digital CMOS sensor output vs photodiode size

	Photodiode Size(µmxµm)			
	100x400	200x400	300x400	400x400
Out-Vdvcm	39	73	105	133
Out-Vcm	39	75	106	134

Note:
Test condition: Red channel, VDD=2.6V, Integration time=15, C_{int} =32 pF, room temp, 150 lux
V_{cm} = VBG, V_{dvcm} is V_{cm} generated from the dark photodiode.

Table 9 indicates that the total integration capacitance increases when a larger photodiode is selected; however, the output is still linearly associated with the size of the photodiode.

Based on equation (2), and from Table 10, the biggest reduction of output voltage error is 36 mV when the compensated voltage common mode, V_{dvcm}, was applied to the single to differential circuit and the C_{int} is 4 pF. This observation of dark current reduction can be verified when ¼ of the dark current value (Table 5) with equation (3), equation (6) and equation (2), the calculated the dark current ADC code is 4 LSB (~36 mV). Overall, it is shown that when V_{dvcm} was applied to the single to differential circuit, an improvement of at least 1-bit resolution is achieved.

Table 10: Digital CMOS sensor output vs $C_{integration}$

	Cintegration (pF)							
	4	8	12	16	20	24	28	32
Out-Vdvcm	118	72	51	40	33	28	24	21
Out-Vcm	122	75	53	42	33	28	25	22

Note:
Test condition: Red channel, VDD=2.6V, Integration time=8, Photodiode size=100µmx400µm, room temp, 150 lux
V_{cm} = VBG, V_{dvcm} is V_{cm} generated from the dark photodiode.

As described in Table 6, the integration capacitance at the lower end is much higher than the targeted value. This will affect the value of output when 4 pF or 8 pF is selected. Nevertheless, the output follows the trend of $1/C_{int}$.

3.4 Colour point of backlighting application results

A digital controller similar to that in Lim *et al.* [2] was implemented and used to configure the basic CMOS RGB sensor as an optical feedback for a PWM-based LED backlighting solution. Several units were tested at 25°C with a power supply of 2.6 V. The colour set point was at CIE x = 0.287, y = 0.296 (9000 K). It was found that the average colour accuracy, $\Delta u'v'$, is 0.002 and the standard deviation was 0.0012.

For colour point stability measurement, RGB LEDs with colour coordinates of Red (x,y) = (0.691, 0.309), Green (x,y) = (0.161, 0.704) and Blue (x,y) = (0.131, 0.073) were used. The R:G:B luminance ratio was 2.6 : 3.9 : 1.0 respectively.

Figure 16a, 16b and 16c show colour drift with temperature (the CMOS RGB colour sensor temperatures are at -20°C, 25°C and 85°C respectively). The LED temperature was varied from 25°C to 70°C. From Figure 16a, 16b and 16c, it is shown that $\Delta u'v'$< 0.008 when the LED temperature is less than 50°C.

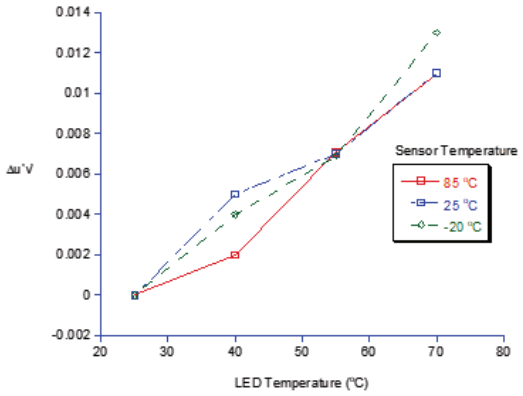

Figure 16 (a): Colour point drift with temperature at 25% duty cycle PWM

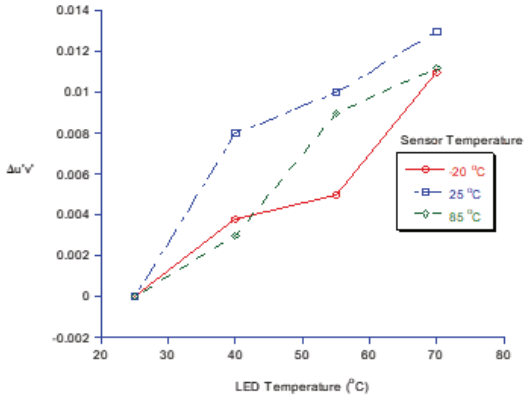

Figure 16 (b): Colour point drift with temperature at 50% duty cycle PWM

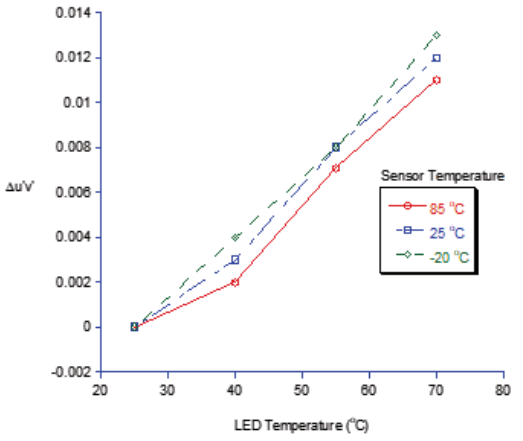

Figure 16 (c): Colour point drift with temperature at 100% duty cycle PWM

Table 11: Comparison of published colour sensors with dark current cancellation circuit

	[13]	[7]	[14]	[15]	[16]	This work
Technique	Photogate bias	Subtraction at digital level	Subtraction	Subtraction	Current source/ steer	Subtraction (modified Vcm)
Dark Current or Dark Signal	0.93 nA/cm^2 or 15 mV/s at 14 V/lux.s	Complete remove	Complete remove	Small	Complete remove. Max range is 12 nA	Complete remove
Dynamic Range (dB)	85	117	N/A	53	N/A	90
Sensor Application	Image	Color sensor	Image	Image	Image	Color Sensor

In Table 11, the performance of the presented design is compared with that of other colour or image sensors in CMOS technology. The presented design is able to completely remove dark current as described in equation (5). The work of Nahtigal and Strle [7] had achieved a very high dynamic range; however, it required a DSP to produce the required RGB colour luminosity; therefore, the work was quite complex and power consuming for portable application. The measured dynamic range (DR) of the design was 90 dB which is comparable to human eye capability. Overall, the performance of the design as a colour sensor was good and comparable to others.

Table 12: Published Colour sensor for backlighting application comparison

	[9]	[26]	This work
Topology	Analog	I-F	Current Integrating and ADC
Technology	LCD and off the shelf components	CMOS	CMOS 0.35 µm
$\Delta u'v'$	0.008	0.006	0.008
RGB	RGB Color Filter	Metal filter	RGB Color Filter

Table 12 shows the comparison of published colour sensors for backlighting application. The presented design has achieved comparable $\Delta u'v'$ results compared with several works [9], [26]. The work in Lee *et al*. [9] did use several off-the-shelf components, which will incur some cost and increase the size. Meanwhile, the work in Gourevitch *et al*. [26] required a DSP to produce the required RGB colour luminosity. The presented design is a complete integrated on-chip solution with real RGB colour signal.

4 Conclusion

In summary, the CMOS colour sensor with integration capacitor had eliminated the need for a low pass filter for detecting PWM light. The gain stage component was also eliminated by using selectable integrating capacitors and photodiode sizes, but the gain function remains the same. Together these techniques had also made the integration of RGB sensor possible. An ADC was integrated together with the circuits into a single silicon in order to produce digital outputs. The measurement results of the fabricated CMOS colour sensor with a dark current cancellation circuit had also proved that the novel dark current cancellation circuit functions as required. The cancellation of dark current was necessary for low value of C_{int} and longer integration time. The implemented CMOS colour sensor in 0.35 µm CMOS technology performed well from –20°C to 85°C as an optical feedback solution where $\Delta u'v' < 0.008$ was achieved at 50°C.

The implication of the research is the technique of using a compensated common mode voltage in the single to differential amplifier. This technique can be applied to other similar circuitries such as temperature-sensitive circuits, and in this case, the common mode voltage is temperature compensated rather than dark current compensated.

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