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Computer Simulation Model for Evaluation of Radiation and Post-Irradiation Effects in Voltage Regulator with Vertical PNP Power Transistor

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Abstract: The aim of the presented research was to develop a faithful SPICE simulation model of radiation and post-irradiation effects in a low-dropout voltage regulator with a vertical serial PNP transistor. The main parameters for the analysis of the circuit's radiation response were the voltage regulator's maximum output current and the minimum dropout voltage, as well as the serial transistor's excess base current. All the data, comprised of the old irradiation and new annealing results, were unified and normalised, in order to enable a broad insight in the radiation tolerance of the examined circuits. Initial radiation effects, as well as the late post-irradiation effects, were successfully simulated using the variations of the maximum forward emitter current gain and knee current of the serial PNP power transistor. Ten-year room temperature annealing led to a significant recovery of the serial transistor's excess base current, yet the maximum output current and minimum dropout voltage, in most cases, expressed further degradation. On the other hand, two short-term, high-temperature annealing periods led to the tremendous recovery of all of the irradiated voltage regulators, reducing the circuit degradation down to the level perceived after absorption of nearly 10% of the total ionising dose.

Keywords: vertical PNP transistor; excess base current; forward emitter current gain; computer simulation; voltage regulator, ionising radiation.

Računalniški simulacijski model za ocenjevanje sevalnih in post sevalnih vplivov na napetostni regulator z vertikalnim močnosnim tranzistorjem PNP

Izvleček: Cilj raziskave je bil razvoj zanesljivega SPICE simulacijskega modela sevalnih vplivov na low-drop napetostni regulator z vertikalnim serijskim tranzistorjem PNP. Glavni parametri analize odziva regulatorja na sevanje je bil največji izhodni tok in najnižja napetostna razlika med vhodom in izhodom (dropout napetost) ter bazni tok tranzistorja. Vsi podatku skupaj z rezultati starega sevanja in toplotne obdelave, so bili poenoteni in normalizirani za lažji vpogled v sevalno odpornost vezij. Začetni sevalni vplivi, kakor tudi post-sevalni vplivi, so bili uspešno simulirani s spreminjanjem ojačenja emitorskega toka in kolenskega toka tranzistorja PNP. Deset letna temperaturna obdelava pri sobni temperature je vodila k očitni ozdravitvi tranzistorskega baznega toka. Največji izhodni tok in najnižja dropout napetost je v večini primerov pokazala dodatno degradacijo. Po drugi strani pa sta dve kratkotrajni visokotemperaturni obdelavi pokazali občutno ozdravljenje obsevanih napetostnih regulatorjev, pri čemer je bila degradacija vezja ob 10% sevalni dozi zanemarljiva.

Ključne besede: vertikalni tranzistor PNP; bazni tok; ojačenje emitorskega toka; simulacije; napetostni regulator; ionsko sevanje.

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1 Introduction

Despite the increasing use of switching power supplies, linear voltage regulators still have a wide area of use in electronic devices, particularly in battery-powered systems [1]. This also applies to radiation-tolerant electronic devices, used in radiation environments such as satellites, nuclear and medical facilities as well as in the military environment. Bipolar transistors [2-5]

and analogue integrated circuits [6, 7] (including voltage regulators [8-11]) have been extensively examined in the radiation fields, particularly following the discovery of the enhanced low-dose-rate sensitivity (ELDRS) in bipolar transistors [12, 13].

Since the cost of dedicated radiation-tolerant integrated circuits is very high, in recent years extensive efforts have been made to identify commercial off-the-shelf (COTS) integrated circuits (and related technology processes) suitable for application in radiation environments [14]. Among the tested circuits is the low-drop-out voltage regulator *STMicroelectronics*® L4940V5, a circuit with a vertical PNP pass transistor [15], founded on the complementary BiCMOS process [16]. The circuit demonstrated unexpectedly high radiation tolerance [17-21], qualifying itself as a serious COTS candidate for use in moderate-dose radiation environments [17, 18]. Nevertheless, there were not enough data to create a faithful computer simulation model. Also, there were no detailed experiments that could quantify the circuit's post-irradiation response.

In order to provide a wider picture on the radiation and post-irradiation effects in the L4940V5 voltage regulator, various isothermal annealing procedures were implemented. After long-term room temperature annealing, two short-term isothermal annealing procedures were performed. Also, a computer simulation model was developed in order to model the response of the vertical serial PNP power transistor. These combined efforts should enable the acquisition of comprehensive knowledge on the L4940V5 voltage regulator's radiation response.

2 Theory

2.1 Radiation effects

Ionising radiation affects silicon bipolar junction transistors mainly through the mechanisms of charge-trapping, both in the oxide and on the semiconductor-oxide interface [14, 22]. The excess base current is the most important measure of the radiation-caused degradation of the bipolar junction transistor. It represents the difference between the base current measured after irradiation (I_B) and the base current prior to irradiation (I_{B0}) [14]:

$$\Delta I_B = I_B - I_{B0} \tag{1}$$

The base current has two components, the ideal one (I_{Bi}), affecting the transistor's current gain, and the recombination component (I_{Br}), being the current of only the internal recombination processes in the base area [8, 23]:

$$I_B = I_{Bi} + I_{Br} = I_S e^{\frac{V_{EB}}{nV_T}} + I_{Se} e^{\frac{V_{EB}}{n_e V_T}} \tag{2}$$

where: I_S – transport saturation current [24], I_{Se} – emitter-base leakage current, V_{EB} – emitter-base voltage, V_T – thermal voltage (being 26 mV at the room temperature of 20°C), n – ideality factor of the ideal base current, n_e – ideality factor of the recombination base current (or, in SPICE models, emitter-base leakage emission coefficient [24]).

Excess base current may be presented as the difference between the pre-irradiation and post-irradiation base currents. The detailed relation for the excess base current is [25]:

$$\Delta I_B = \frac{1}{2} q n_i P_E \left[s'' x_{dB} e^{\left(\frac{V_{eff}}{2V_T}\right)} - s' W_d e^{\left(\frac{V_{EB}}{2V_T}\right)} \right] \tag{3}$$

where: s' – pre-irradiation surface recombination velocity, s'' – post-irradiation surface recombination velocity, W_d – width of the depletion area in the base-emitter area prior to irradiation, q – elementary electron charge ($1.6 \cdot 10^{-19}$ C), n_i – intrinsic carrier concentration in silicon, x_{dB} – location of the depletion region at the surface of the base, P_E – emitter perimeter, V_{eff} – effective voltage (used in place of V_{EB}, in order to include the influence of the oxide-trapped charge on the total voltage on the emitter-base junction) [25]. The excess base current rises proportionally to the difference of the surface recombination velocities existing prior to and after the exposure to ionising radiation. For a heavily-doped emitter and low emitter-base voltage (up to 0.6 V) [26], the excess base current may be considered to be directly proportional to the increase of the concentration of interface traps [26, 27]. Nevertheless, the excess base current cannot be affected only by the interface traps. The influence of the oxide-trapped charge is particularly important in the cases when the emitter was not heavily doped. Build-up of the oxide-trapped charge will increase the surface potential of the P-type emitter area [25]. Therefore, the surface recombination velocity depends on both the interface traps and the oxide traps.

The ideality factor for the ideal base current is $n = 1$, but its value is not constant for the recombination current. Usually, the ideality factor of the recombination current is considered to be $n_e = 2$, the same as during the normal operation of the transistor with a high emitter injection level [22]. Nevertheless, in reality, the re-

combination current ideality factor has variable values between 1 and 2. Despite the long-known fact that the ideality factor is dependent on the applied base-emitter voltage [26], this fact is neglected in standard computer simulation models.

In NPN bipolar transistors, the P-type base, right beneath the isolation oxide, is the most sensitive area. The reason is the relatively low doping concentration of the P-base, in comparison with the N-type collector and emitter. Both oxide-trapped charge and interface traps would negatively affect the P-type base, causing a rise in the excess base current [23]. On the other hand, in PNP transistors, the N-type base is not so endangered, since the positive oxide-trapped charge will cause the electrons to accumulate in the base area, suppressing the negative effects of the interface traps during the initial phase of irradiation [25]. If the emitter area is not heavily implanted, it will be the area most affected by the influence of radiation, experiencing the negative influence of both interface traps (increasing the surface recombination in silicon) and oxide traps (causing the depletion of the emitter area beneath the oxide) [28]. Mutually, these effects cause the depletion region on the base-emitter junction to spread deep into the emitter area, affecting the rise in the excess base current [28]. The mentioned effects depend on many factors, such as doping concentrations, the geometry of the transistors, the quality of oxides and passivation layers, etc.

During the exposure to radiation of the silicon bipolar junction transistors, the initial phase will be dominated by the influence of the oxide-trapped charge [25]. At the same time, the concentration of the charge trapped at the interface between the silicon and silicon-dioxide will rise much more slowly, affecting the rise in the excess base current almost proportionally to the total absorbed dose [25]. Yet, after some time has elapsed in the ionising radiation field, the surface recombination velocity will reach its limit and the excess base current will enter the saturation phase.

2.2 Annealing

Stability of defects in semiconductors and oxides, caused by radiation, depends on time, electric field and temperature [22]. Thus, a concentration of defects in materials may significantly change after irradiation, with tendency to substantially reduce in high-temperature ambient [22]. Depending on the nature of radiation and trapped charge (both in oxide and a semiconductor-oxide interface), bipolar transistors may partially recover or even further degrade its characteristics. Analysis of post-irradiation, time-dependent effects should provide a more detailed insight into the radiation response of the circuits exposed. Thermal excitation usually leads to a significant defect annealing at temperatures of 100°C and greater, while the tunneling is a dominant effect at a room temperature [22]. Several procedures were usually used, based either on isothermal [14] or isochronal [22] annealing. Isothermal annealing procedures are performed at a constant temperature (either room or elevated) [14], and this approach often enables a qualitative evaluation of the radiation-induced defects. On the other hand, isochronal annealing is performed with constant, successive time intervals [22], usually much shorter than the ones used for isothermal examinations. Isothermal annealing is a more realistic test procedure, since it may simulate a real exploitation conditions, in periods from one day up to several years. On the other hand, isochronal annealing procedures may involve high temperatures, yet in much shorter time intervals (in order of minutes).

According to the published data [29], some integrated circuits showed annealing of the trapped holes from the oxide after the end of the elevated temperature (100°C) isothermal annealing, without a significant effect on the interface traps. Therefore, it would be possible for some devices to express radiation-induced degradation originating only from the influence of interface traps [29]!

3 Materials and methods

Analysis of irradiation and isothermal annealing effects was performed on integrated 5-volt, positive voltage regulators *STMicroelectronics*® L4940V5. Samples were irradiated in the ^{60}Co ionising radiation field in the Vinča Institute of Nuclear Sciences, Belgrade, Serbia, in the Metrology-Dosimetry Laboratory [17-19]. The devices absorbed total γ-radiation doses of 500 Gy(SiO_2), at a dose rate of 4 cGy(SiO_2)/s [20, 21]. For nearly ten years, the irradiated samples were kept in the office locker, at a room temperature always kept in the range 15–25°C.

After 85,000 hours, all the samples of voltage regulators were tested in the same conditions as immediately after the irradiation, with a room temperature of 20°C. Shortly afterwards, the L4940V5 voltage regulators were examined to see if it would be possible to recover most of the oxide-trapped charge after one-week's annealing at the temperature of 100°C, with a negligible effect on the interface traps. Consequently, another one-week annealing at 150°C should lead to the complete recovery of all the radiation-induced oxide-trapped charge and most of the interface traps.

The primary examined parameters were the voltage regulator's maximum output current, the serial transis-

tor's minimum dropout voltage and the total circuit's quiescent current. Measurement of the quiescent current enabled the calculation of the serial transistor's base current and, consequently, the serial transistor's forward emitter current gain [18, 20, 21]. Voltage and current vaweforms were recorded using the oscilloscope *Fluke*® 196C.

Several days after completion of the room-temperature annealing experiment, the circuits were annealed in the thermal chamber, at a temperature of 100°C, uninterruptedly for 168 hours. After the seven-day annealing, a new round of experiments was performed, with the same electrical parameters recorded. Finally, a day after the completion of the second round of electrical measurements, a final isothermal annealing sequence was performed, for another 168 hours with the same samples in the thermal chamber, yet this time at a temperature of 150°C. After the completion of the last annealing phase, the final data set on annealed voltage regulators was recorded. The presented sequence of isothermal annealing procedures, with the various temperatures and durations, should enable better insight into the influence of interface traps and the oxide-trapped charge on the radiation and post-irradiation response of a complex integrated circuit. Ten years should be a typical exploitation period for the electronic components in aerospace applications [22].

Since the manufacturer of the circuit L4940V5 did not provide the schematic circuit diagram of this voltage regulator, many efforts were made to gather the necessary data on the internal structure of this device. Using the published papers [30, 31] and patents [16, 32], the author created a basic computer simulation model in the program "LTspice IV" [33]. The created model was rigorously examined and improved until it enabled a pretty good recreation of a wide ensemble of experimental results. There was no intention to recreate all the details of the integrated circuit as made by its manufacturer, so it is not a straight replica of the particular circuit design. Yet, the presented simulation model was good enough to describe the circuit's response to the influence of γ-radiation.

In order to present the circuit's response for various bias and load conditions, previously published results were unified with the data from new experiments. The data on the mean values of the maximum output current [17, 18], minimum dropout voltage [20, 21] and on-line parameters [19, 34], procured immediately after the exposure of the L4940V5 devices, were extensively presented in previous years. However, new experiments on the isothermal annealing of the voltage regulator were done on the same samples, yet this time ten years later. So, in order to avoid the unnecessary repetition of the old data, mostly results normalised to the data on virgin devices are now presented. Yet, the creation of the computer simulation model, as well as in-depth analysis of the perceived radiation effects, was not possible without unification of all the experimental data obtained.

Descriptions of the experiments performed, the radiation sources, and the procedures implemented for procurement of the circuit's electrical parameters are in the detail provided in the references [17–21, 34, 35].

4 Results

Table 1 summarises the results on maximum output current and minimum dropout voltage (for load currents of 100 mA and 400 mA), obtained in the γ-radiation field with various biases and loads during irradiation. From the data on the quiescent current in the examined circuits, as well as from data on unloaded voltage regulators, the values of the serial transistor's base current and the internal control circuit's consumption were calculated (in a positive voltage regulator with the PNP pass transistor, total quiescent current represents the sum of these two currents [18, 21]). Consolidated results were presented, showing, firstly, data on unexposed circuits, then the data procured after absorption of total doses from 50 Gy up to 500 Gy, and, finally, the data procured during the isothermal annealing (long-term room-temperature, followed by short-term 100°C and 150°C annealing). Only the most important data necessary for the circuit response analysis are presented in the table, and all data were normalised to the values of virgin devices. Therefore, since the data on unloaded voltage regulators had basically the same trends in all three cases, only data obtained during the examination of the maximum output current are presented.

As previously reported on its radiation response [17-21], and being valid also following the implemented annealing of the tested circuits, the voltage regulator kept stable output voltage in all the examined operating points, regardless of the bias conditions during previous irradiation. The voltage reference circuit suffered negligible degradation, since the variations of the output voltage in unloaded devices could be measured in millivolts [21, 34]. The waveforms of the input voltage, output voltage and quiescent current, recorded on the laboratory setup, were presented in Fig. 1. Despite the high alternate current components, measured values of direct current enabled successful evaluation of the voltage regulator's radiation response.

Table 1: Relative values of serial transistor's dropout voltage (V_{EC12}; for tests with load current of 100 mA and 400 mA), maximum output current (I_{max}) and no-load quiescent current (I_{Q0}), as well as the accompanying data on the absolute values of the serial transistor's excess base current (ΔI_{B12}) in voltage regulator *STMicroelectronics*® L4940V5. Values were based on data recorded on virgin devices, during the exposure, and after irradiation, for the specified periods and types of isothermal annealing. Experimental results were extended with parameters of the serial transistor (maximum forward emitter current gain (β_{Fmax}) and knee current (I_{kF})), defined in the SPICE simulation models. Simulation models with serial PNP power transistors, having the parameters specified in the last two columns, were ones that reached high agreement with the data procured through all three types of experiment. Successive periods of isothermal annealing were marked as follows: annealing 1 (Θ_a = 20°C, t = 85,000 hours); annealing 2 (Θ_a = 100°C, t = 168 hours); annealing 3 (Θ_a = 150°C, t = 168 hours). Basic values of serial transistor's dropout voltage, base current and no-load quiescent current, experimentally procured on unexposed (D = 0 Gy) L4940V5 voltage regulators, for various bias and load conditions: a) 0 V, 0 A: V_{EC12} (100 mA) = 0.355 V [20], I_{B12} (100 mA) = 0.545 mA [20], V_{EC12} (400 mA) = 1.766 V [21], I_{B12} (400 mA) = 4.627 mA [21], I_{max} = 835.9 mA [18], I_{Q0} = 3.753 mA [18], I_{B12} (max) = 20.397 mA [18]; b) 8V, 1 mA: V_{EC12} (100 mA) = 0.394 V [20], I_{B12} (100 mA) = 0.703 mA [20], V_{EC12} (400 mA) = 1.736 V [21], I_{B12} (400 mA) = 3.824 mA [21], I_{max} = 855.1 mA [18], I_{Q0} = 3.772 mA [18], I_{B12} (max) = 19.028 mA [18]; c) 8 V, 100 mA: V_{EC12} (100 mA) = 0.392 V [20], I_{B12} (100 mA) = 0.734 mA [20], V_{EC12} (400 mA) = 1.763 V [21], I_{B12} (400 mA) = 4.417 mA [21], I_{max} = 852.5 mA [18], I_{Q0} = 3.806 mA [18], I_{B12} (max) = 25.304 mA [18]; d) 8 V, 500 mA: V_{EC12} (100 mA) = 0.378 V [20], I_{B12} (100 mA) = 0.731 mA [20], V_{EC12} (400 mA) = 1.793 V [21], I_{B12} (400 mA) = 5.638 mA [21], I_{max} = 820.5 mA [18], I_{Q0} = 3.806 mA [18], I_{B12} (max) = 25.304 mA [18].

STMicroelectronics® L4940V5		Type of experiment										Simulation	
Operation during irradiation and annealing		V_{EC12} (100 mA)			V_{EC12} (400 mA)			Imax				Parameters of serial PNP power transistor, Q_{12}	
Bias and load during irradiation	Dose, D [Gy]	V_{EC12} [p.u.]	I_{B12} [p.u.]	ΔI_{B12} [mA]	V_{EC12} [p.u.]	I_{B12} [p.u.]	ΔI_{B12} [mA]	I_{max} [p.u.]	I_{Q0} [p.u.]	I_{B12} [p.u.]	ΔI_{B12} [mA]	β_{Fmax}	I_{kF} [A]
0 V 0 A	0	1	1	0	1	1	0	1	1	1	0	270	0.225
	50	1.161	2.422	0.78	1.153	1.813	3.76	0.995	0.981	1.44	8.98	115	0.375
	100	1.144	4.128	1.71	1.208	3.395	11.08	0.956	0.959	1.760	15.49		
	500	1.631	75.43	40.57	1.298	7.478	29.98	0.966	0.874	1.997	20.34		
	Annealing 1	1.27	3.996	1.63	1.265	3.127	9.84	0.862	0.933	2.118	22.8		
	Annealing 2	1.087	3.486	1.36	1.067	2.669	7.72	0.916	0.965	1.567	11.56	67	0.49
	Annealing 3	1.234	2.312	0.64	1.08	1.659	1.82	0.898	0.967	1.28	5.71	125	0.38
8 V, 1 mA	0	1	1	0	1	1	0	1	1	1	0	340	0.225
	50	1.023	1.55	0.39	1.11	1.349	1.34	0.999	0.986	1.089	1.7	180	0.375
	100	0.990	2.119	0.79	1.139	1.938	3.59	0.993	0.976	1.435	8.27	115	0.425
	200	1.000	3.599	1.83	1.127	3.894	11.07	0.980	0.954	1.785	14.94	45	1.1
	300	1.003	5.747	3.34	1.242	6.859	22.41	0.974	0.938	1.870	16.55		
	500	1.251	27.89	18.91	1.347	8.567	28.94	0.958	0.917	1.904	17.2		
	Annealing 1	1.071	5.334	3.05	1.395	7.377	24.39	0.894	0.936	2.27	17.2		
	Annealing 2	1.071	3.115	1.49	1.187	2.712	6.55	0.937	0.962	1.904	11.71	60	0.7
	Annealing 3	1.198	1.508	0.36	1.181	1.42	1.61	0.946	0.973	1.616	2.57	150	0.39
8 V, 100 mA	0	1	1	0	1	1	0	1	1	1	0	340	0.225
	50	1.028	1.88	0.65	1.132	1.607	2.68	0.992	0.983	1.377	6.82	127	0.375
	100	0.987	3.011	1.48	1.161	2.719	7.59	0.968	0.967	1.723	13.08	55	0.75
	200	1.031	6.131	3.77	1.243	7.19	27.34	0.961	0.941	2.027	18.57		
	500	1.372	57.96	41.81	1.284	8.021	31.01	0.954	0.899	2.202	21.73		
	Annealing 1	1.372	11.38	7.62	1.336	7.63	29.28	0.891	0.922	2.065	19.26		
	Annealing 2	1.092	3.856	2.1	1.221	3.337	10.32	0.967	0.951	1.829	14.99	45	1
	Annealing 3	1.115	1.703	0.52	1.188	1.535	2.36	0.934	0.967	1.326	5.9	120	0.4
8 V, 500 mA	0	1	1	0	1	1	0	1	1	1	0	240	0.2
	50	0.971	1.929	0.68	1.085	1.591	3.33	1.007	0.98	1.164	4.15	100	0.375
	100	1.011	3.010	1.47	1.153	2.914	10.79	0.999	0.962	1.289	7.32		
	500	1.704	54.56	39.15	1.267	6.297	29.86	1.01	0.909	1.427	10.8		
	Annealing 1	1.235	13.42	9.08	1.35	5.692	26.45	0.932	0.943	1.432	10.42		
	Annealing 2	1.103	3.844	2.08	1.25	3.663	15.01	0.969	0.956	1.368	9.32		
	Annealing 3	0.997	1.696	0.51	1.161	1.453	2.55	0.942	0.967	1.148	3.76	105	0.375

Basic data on the vertical serial PNP power transistor, obtained using the SPICE simulations, are also included in Table 1. Since the previous research concluded that the control circuit did not have a significant influence on the voltage regulator's radiation response [20, 21], the focus of the computer simulation analysis was on the serial power transistor. The primary influence on the L4940V5 voltage regulator's radiation hardness was the interdigitated structure of its serial PNP transistor [17, 19]. Therefore, the serial power transistor's excess base current was the best measure of the circuit's radiation response.

After careful examination, the results from Table 1 may provide much information about the L4940V5 circuit's radiation and post-irradiation response. All the irradiated circuits expressed lower recovery (from deposition of the total dose of 500 Gy) during the ten-year room-temperature annealing than during the two seven-day high-temperature annealing sequences. Recovery of the circuits after two-week isothermal annealing was not complete, yet the main parameters pointed to circuit damage comparable to the state recorded after the absorption of the total ionising dose of 50 Gy.

Variations of the serial power transistor base current, presented in Table 1, may lead to the identification of two different circuit responses, for the irradiation and post-irradiation periods. The first category of results comprises the initial period of irradiation (up to 50 or 200 Gy, depending on the bias and load conditions), as well as the final periods of high-temperature isothermal annealing. The second category of results comprises the data procured after absorption of higher total doses, as well as the initial annealing periods (particularly the long-term, room-temperature annealing). The main means of identification of these categories is the saturation of the serial transistor's base current, in either of the three data ensembles. The threshold value of the base current, when overcurrent protection is activated, is approximately 35 mA. This value corresponds to the total voltage regulator's quiescent current of nearly 40 mA. When the serial transistor base current is always less than 35 mA, the radiation response of the PNP bipolar power transistor can be modelled with the standard Gummel–Poon model, with variations of only the maximum forward emitter current gain and the knee current. On the other hand, whenever the base current exceeded this threshold voltage, the SPICE model, successfully describing the circuit response for all three types of experiment, could not be made. In some cases, the power transistor base current was higher in control points with the collector current being 100 mA, than in the case when the collector current was 400 mA!

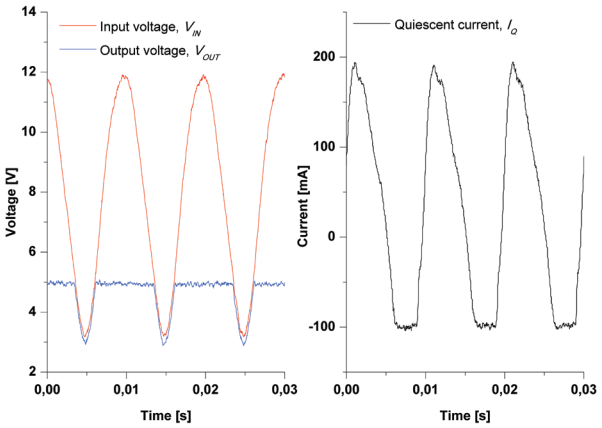

Figure 1: Waveforms of input and output voltage (left) and quiescent current (right), recorded on the unexposed L4940V5 voltage regulator during the examination of the maximum output current

The bias conditions had a great influence on the radiation response of the irradiated circuits. Data from Table 1 show opposite trends of the radiation response of the power transistor, on the one hand, and the rest of the circuit, on the other. While the serial transistor's base current increased, increasing also the voltage regulator's quiescent current, the quiescent current of the control circuit (I_{Q0}) declined [21]. Yet, the primary focus was on the examination of the characteristics of the vertical power transistor, since it had the most obvious effect on the voltage regulator radiation response. So, analysing the variations of the excess base current, shown in Table 1, the clear scale of the radiation sensitivity of exposed circuits may be defined. Gamma-radiation inflicted the greatest damage on biased and heavily loaded voltage regulators (V_{in} = 8 V, I = 500 mA). Lower degradation was seen in unbiased devices, followed by even lower degradation in biased and moderately loaded voltage regulators (V_{in} = 8 V, I = 100 mA). The least damage was expressed by biased and negligibly loaded devices (V_{in} = 8 V, I = 1 mA).

The waveforms of the quiescent current and output current recorded on the laboratory setup are presented in Fig. 1.

5 Discussion

5.1 Computer simulation

Fig. 2 presents a simplified computer simulation model of the L4940V5 voltage regulator, created in the program tool "LTspice IV" [33]. As can be seen from Fig. 2, the voltage reference and the error amplifier were represented only by general models. On the other hand,

the simulation model of the serial PNP power transistor, Q12, was very complex. The main reason is the negligible radiation degradation of the control circuit elements, in opposition to the serious degradation of the serial power transistor. Due to its strong influence on the results obtained, the model included many details on the power supply circuit and the accompanying cables.

Due to the low value of the main filter capacitor (nominally 330 μF), the examined voltage regulators operated in two periods: with the constant output voltage and with its decreased value, falling below the nominal value of 5 V (see Fig. 1). Therefore, the integrated circuit's quiescent current had very rapid variations in these two operation sequences. Also, since the local ground of the examined voltage regulator was separated from the power supply ground by a cable, 10 m long, it also increased the alternating current component of the voltage regulator's quiescent current. In the period of 10 ms, matching the inherent frequency of the single-phase diode bridge, there was, de facto, operation of the voltage regulator with the dominant alternating current superimposed on its direct current component. Relatively low values of the maximum output current (being 720– 850 mA), as well as high values of the minimum dropout voltage, are a direct consequence of the low capacity of the main filter capacitor. Nevertheless, the experimental configuration was not changed, in order to enable mutual comparison of all the obtained and presented data, dating back to 2006 [17]. Yet, even in these circumstances, measurement of the mean values of quiescent currents led to the correct calculation of the serial power transistor's base current and its forward emitter current gain. Despite the high alternate current components, the computer simulation proved that the measured values of direct current, presented in tables 1 and 2, enabled successful evaluation of the voltage regulator's radiation response.

The reaction of the anti-saturation circuit was also important, since it had a substantial influence on the quiescent current response. Whenever the dropout voltage on the pass PNP transistor fell below the threshold level, the anti-saturation circuit reacted in order to prevent the flow of excessive current from the serial transistor to the substrate and, consequently, to the ground contact. Therefore, the anti-saturation circuit was modelled in great detail.

Another important element was the overcurrent protection of the driver NPN transistor, Q13. In order to prevent the voltage regulator's quiescent current rising above its upper limit of 50 mA [15], the transistor Q15 activates and takes the excessive collector current of the driver transistor, indirectly limiting the base current of the serial transistor. The consequence of this protection is the reduction of the voltage regulator's maximum output current. This was exactly the circuit response that was recorded in numerous experiments, particularly after the absorption of the higher total doses of γ-radiation.

As the basic element for modelling the serial vertical PNP power transistor, the SPICE model of discrete transistor BC808-25 was used [36]. This is a discrete PNP transistor with the following nominal parameters: collector–emitter breakdown voltage BV_{CE0} = 25 V, nominal collector current I_C = 500 mA, cut-off frequency f_T = 100 MHz, with the maximum value of the forward emit-

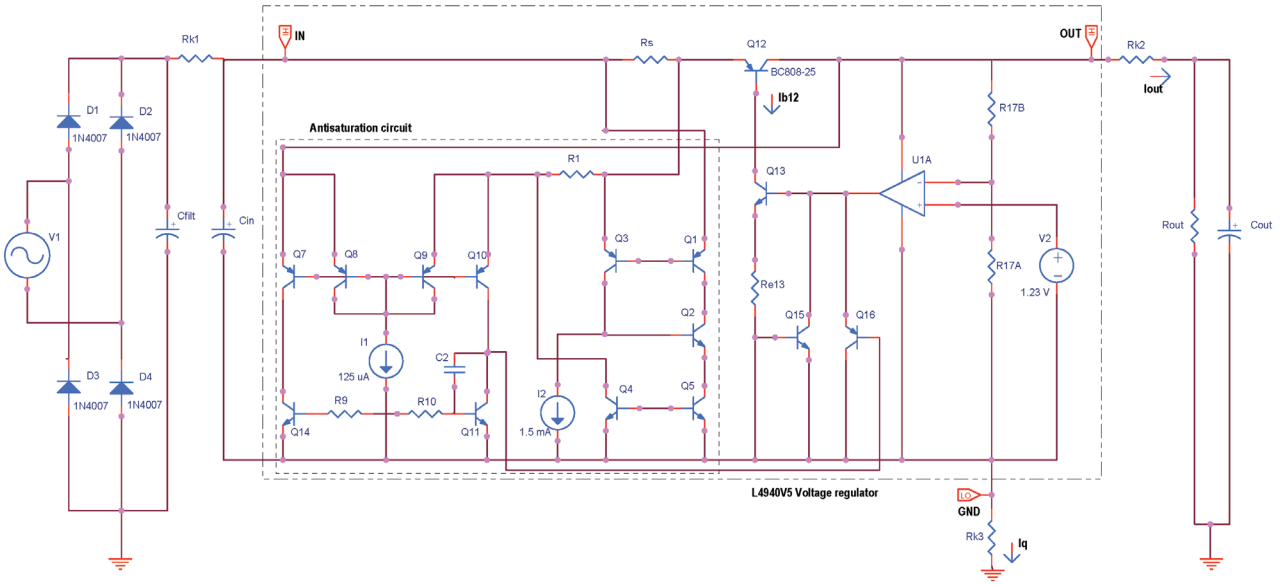

Figure 2: Schematic circuit diagram of L4940V5 voltage regulator

ter current gain being in the range β_F = 160–400 [37]. These data are close to the specified characteristics of the vertical PNP power transistor in device L4940V5 (f_T = 80 MHz, β_F = 50 for the load of 1 A, BV_{CE0} = 20 V) [15, 30].

Table 2 enables mutual comparison of simulation and experimental data on the serial transistor's base current. Simulation data on parameters variations of the vertical serial PNP power transistor are also included in Table 1. Transistor parameters were selected in order to enable the highest possible agreement with the results for all three types of experiments. In the initial period of irradiation, for total ionising doses from 0 Gy up to 200 Gy, the simulation model reproduced the experimental results very well. In the initial phase, a sharp decline of the forward emitter current gain was seen for all the tested operation conditions [17-21]. This decline was successfully modelled in the computer simulation using just the variations of the maximum forward emitter current gain (β_{Fmax}) and the forward knee current (I_{kF}). Variations of the current gain and the excess base current were most successfully modelled for the biased and negligibly loaded voltage regulators. For other devices, both unbiased or biased and loaded with higher currents, procuring a faithful simulation model was much more difficult. Without exception, when the devices reached saturation of the excess base current, precise modelling was impossible. Unbiased and heavily loaded circuits L4940V5 entered this phase after the absorption of low total doses (50 Gy), while the biased and negligibly loaded devices experienced saturation after longer exposure (200 Gy).

Table 2: Mutual comparison of absolute values of serial transistor's base current (I_{B12}) in voltage regulator *STMicroelectronics*® L4940V5, obtained both with SPICE simulation and experiment. Experiments were executed on variations of dropout voltage (V_{EC12}; for tests with load current of 100 mA and 400 mA) and maximum output current (I_{max}), for absorption of total ionising doses up to 500 Gy(SiO_2). The results were extended with parameters of the serial transistor (maximum forward emitter current gain (β_{Fmax}) and knee current (I_{kF})), defined in the SPICE simulation models. Only experimental results that reached high agreement with simulation models were presented. Successive periods of isothermal annealing were marked as follows: annealing 2 (Θ_a = 100°C, t = 168 hours); annealing 3 (Θ_a = 150°C, t = 168 hours).

STMicroelectronics® L4940V5		Simulation and experiment						Simulation	
Operation during irradiation and annealing		V_{CE12} (100 mA)		V_{CE12} (400 mA)		I_{max}		Parameters of serial PNP power transistor, Q_{12}	
Bias and load during irradiation	Dose, D [Gy]	Simulation	Experiment [20]	Simulation	Experiment [21]	Simulation	Experiment [18]	β_{Fmax}	I_{kF} [A]
		I_{B12} [mA]	I_{B12} [mA]	I_{B12} [mA]	I_{B12} [mA]	I_{B12} [mA]	I_{B12} [mA]		
0 V 0 A	0	0.72	0.55	4.67	4.63	20.77	20.4	270	0.225
	50	1.18	1.32	7.72	8.39	27.77	29.38	115	0.375
	Annealing 2	1.88	1.9	11.39	12.35	32.44	31.96	67	0.49
	Annealing 3	1.1	1.18	7.06	6.45	21.57	26.1	125	0.38
8 V, 1 mA	0	0.89	0.7	4.03	3.82	19.06	19.03	340	0.225
	50	1.08	1.09	5.17	5.16	21.53	20.73	180	0.375
	100	1.36	1.49	7.33	7.41	27.73	27.3	115	0.425
	200	2.5	2.53	12.39	14.89	34.39	33.97	45	1.1
	Annealing 2	1.98	2.19	10.85	10.37	31.11	30.74	60	0.7
	Annealing 3	0.94	1.06	5.8	5.43	20.67	21.6	150	0.39
8 V, 100 mA	0	0.89	0.73	4.03	4.42	19.06	18.07	340	0.225
	50	1.09	1.38	7	7.1	26.32	24.89	127	0.375
	100	2.14	2.21	11.51	12.01	33.87	31.15	55	0.75
	Annealing 2	2.52	2.83	12.72	14.74	35.21	33.06	45	1
	Annealing 3	1.13	1.25	7.14	6.78	24.22	23.97	120	0.4
8 V, 500 mA	0	0.79	0.73	5.7	5.64	23.23	25.3	240	0.2
	50	1.35	1.41	8.86	8.97	30.62	29.45	100	0.375
	Annealing 3	1.29	1.24	8.42	8.19	26.31	29.06	105	0.375

Partially unexpected were data on the long-term room-temperature annealing. Initial checks of several irradiated samples led to the assumption that, in the long-term perspective, irradiated L4940V5 voltage regulators would mostly recover [21]. Nevertheless, data obtained after 85,000 hours of room-temperature annealing did not support this hypothesis [34]. Despite the recovery of the serial transistor current gain and reduction of its excess base current, the maximum output current in most cases significantly declined. Yet, two successive one-week, high-temperature annealing sequences (100°C, followed by the 150°C exposure) led to the expressed circuit recovery. In all the examined cases, high-temperature annealing of devices irradiated until absorption of the total dose of 500 Gy led to nearly the same parameters as those recorded after absorption of 50–200 Gy. More important, these conditions could be again successfully modelled only with variations of the current gain and knee current of the serial transistor, just as in the initial period of irradiation.

5.2 Radiation effects

As can be expected from the theory [38], unbiased devices suffer the most obvious damage, while bipolar intergated circuits with a high positive bias voltage during irradiation show much less degradation from the influence of radiation. On the one hand, this could be expected, since the high positive bias voltage injects the electrons in oxide, causing the trapped holes to recombine and consequently reducing the total oxide-trapped charge concentration. Yet, unbiased irradiation cannot enhance the hydrogen ions transport and, therefore, will have less influence on the build-up of interface traps.

A sharp initial decline of the forward emitter current gain, presented in Table 1, points to the dominant influence of the oxide-trapped charge. The current gain declined rapidly, as presented in Table 1 and the maximum value of the forward emitter current gain decreased from 340 down to 55 (for biased and moderately loaded devices), following exposure to only 100 Gy. Also, at the same time the serial PNP power transistor's knee current significantly increased, rising from 0.225 A to 0.75 A. The emitter-base leakage emission coefficient, used in the simulation model of the transistor BC808-25 and, therefore, of the power vertical PNP transistor used in the present simulation, was a constant with a value n_e = 1.568 [36]. Other voltage regulator elementary circuits were not seriously affected by ionising radiation, so the remaining elements of the simulation model were not changed.

This initial rapid degradation of the serial transistor current gain clearly points to the main negative influence of the oxide-trapped charge. Yet, in the previous research it was calculated that the emitter area has a surface doping concentration equal to $3.3 \cdot 10^{17}$ cm^{-3} [21]. This is a relatively high value for a PNP power transistor, and it was therefore assumed that the emitter should not be so much affected by the influence of the oxide-trapped charge, particularly since the emitter crowding was not perceived [21]. Nevertheless, despite such a high impurities concentration for a power device, this value was not so high, particularly in comparison with a small-signal PNP transistor, having an emitter doping concentration up to 10^{20} cm^{-3} [28]. Also, the interdigitated structure of the pass element, with 40 elementary PNP power transistors [30], was another reason for its lower radiation tolerance. Therefore, the main reason for such an obvious rise in the excess base current was certainly primarily related with the emitter, rather than the base area.

After the initial phase of radiation exposure, the next phase showed saturation in the serial PNP transistor's excess base current, particularly after exposure of the samples to 500 Gy [18, 20, 21]. These results point to the reaction of the overcurrent protection of the NPN driver transistor Q13 (Fig. 2), preventing the rise of the voltage regulator's quiescent current above the foreseen maximum of 50 mA [15]. Saturation in the oxide-trapped charge build-up was always perceived for high total doses, being 500 Gy (with the exception of the biased and negligibly loaded samples). Yet, the problem is that it was not possible to create an adequate computer simulation model of the PNP power transistor for higher total doses! Whatever was implemented in the SPICE model of the serial transistor, it was not possible to get mutually faithful results for either the maximum output current (I_{out} = 720 – 850 mA) or the minimum dropout voltages (recorded for 100 mA and 400 mA) using the basic Gummel–Poon models. There were earlier attempts to simulate the increased recombination current in the base area, with the ideality factor of 2 [8]. Other tools, such as additional resistors, current sources, variations of the surface recombination currents or the other power transistor parameters did not help much. The most successful attempt was made with the implementation of a significantly increased base-emitter saturation leakage current (I_{se}). Yet, even in these cases, it was not possible to alter one simple fact: regardless of the output current (100 mA, 400 mA or 800 mA), for a dose of 500 Gy, the base currents were, in most cases, nearly the same, being 35–40 mA. Nevertheless, even with this saturation of the base current, the experiment indicated that the voltage regulator operated correctly, without significant degradation of its output voltage and with only a moderate decline of the maximum output current at some control points. The exponential dependence of the base current on

the emitter-base voltage, accompanied by the successful simulation of the voltage regulator response with high output currents, could not be realised. So, despite the variations of either the emitter-base leakage current (I_{se}) or the emitter-base leakage emission coefficient (n_e), a satisfactory simulation model suitable for the description of the high total-dose response could not be created.

5.3 Post-irradiation effects

Data on the ten-year room-temperature annealing, presented in Table 1, point to a significant recovery of the serial transistor's excess base current, hand in hand with further degradation of the maximum output current and, in some cases, minimum dropout voltage. More important, saturation of the excess base current remained present during the examination with higher currents, making it impossible to create faithful SPICE models of the first phase of annealing. Tremendous recovery of the excess base current may be observed particularly in unbiased devices, reducing the serial transistor's base current nearly twentyfold! Also, in this, the most obvious case, the maximum output current, i.e. the serial transistor collector current, significantly declined. Various previous studies emphasize that, at room temperature, oxide-trapped charge anneals with time, contributing to the recovery of current gain [25], while interface traps in the field oxide often do not anneal [39]. Thus, it may be assumed that, following the ten-year room temperature annealing of the L4940V5 voltage regulators, the oxide-trapped charge partially recovered, while the interface-trapped charge continued to build up. Therefore, the power transistor's current gain recovery was primarily affected by the positive influence of the recovery of the oxide-trapped

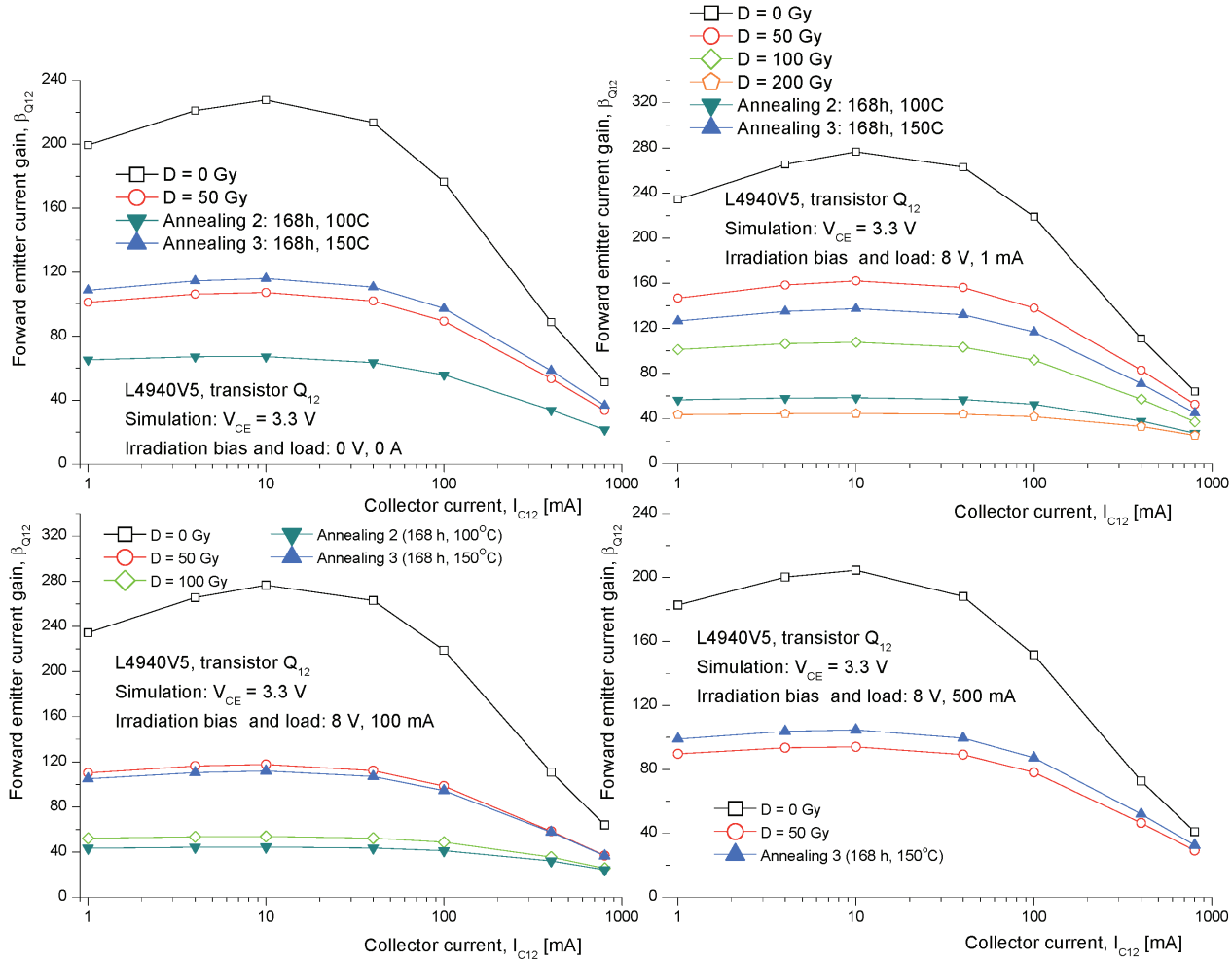

Fig. 3. Variations of the power PNP transistor current gain as a function of the collector current in: a) unbiased circuits (V_{in} = 0 V, V_{out} = 0 A); b) biased and negligibly loaded (V_{in} = 8 V, V_{out} = 1 mA); c) biased and moderately loaded (V_{in} = 8 V, V_{out} = 100 mA); d) biased and heavily loaded circuits during irradiation (V_{in} = 8 V, V_{out} = 500 mA). Diagrams were created for constant collector–emitter voltage, being V_{CE} = 3.3 V. Data were obtained from computer simulation models of the irradiated and annealed voltage regulators, which demonstrated high agreement with the experimental results presented in Table 1.

charge. The negative influence of further interface traps build-up, causing the serial transistor's collector current to decline, had a much less obvious effect on its forward emitter current gain.

The first high-temperature annealing sequence, including one-week at 100°C exposure, reduced the radiation damage to a level slightly above the one observed following the 100-Gy irradiation. The second sequence, involving 168-hour annealing at 150°C, further reduced the radiation damage down to the degradation caused by the total ionising dose of 50 Gy. With the exception of the samples that were heavily loaded during the irradiation, the voltage regulators' characteristics, following the high-temperature annealing sequences, could be successfully modelled, in the same way it was done in the initial phase of irradiation, using the variations of only the current gain and knee current. No sign of heavy saturation was observed in the forward emitter current gain after exposure to higher total doses of γ-radiation. Data on the short-term, high-temperature annealing pointed to a substantial recovery of the irradiated circuits, bringing them close to their pre-irradiation characteristics. Nevertheless, the data in Table 1 show that β_{Fmax} recovered only to 40–50 % of their pre-irradiation values. Yet, even this was enough for a nearly complete recovery of the voltage regulator's output parameters.

Fig. 3 presents diagrams of the serial transistor's forward emitter current gain variation as a function of its collector current, in the range from 1 mA to 800 mA. For the specified collector currents, values of the serial transistor base-emitter voltage were in the range from 620 mV to 830 mV. Diagrams were produced from computer simulation models for all four types of bias and load conditions, briefly described in Table 1. The vertical PNP power transistor operates with output current being at least 1 mA, since this current flows through the voltage divider resistors when the voltage regulator operates without load. All data were obtained with a constant collector– emitter voltage of V_{CE} = 3.3 V. Opposite to the results presented in Table 1, based on the measured mean values, the data presented in Fig. 3 were obtained using the instantaneous values of voltages and currents, at the operation point with constant output voltage (V_{out} = 5 V) and an appropriate input voltage of V_{in} = 8.3 V.

As can be seen from Table 1 and Fig. 3, the three isothermal annealing sequences led to similar characteristics of marginally irradiated and mostly recovered L4940V5 voltage regulators. The computer simulation models for these, principally different, periods, were basically the same. Yet, this could not be used as evidence that the distribution of the trapped charge was the same at the beginning and at the end of this decade-long experiment. Using only SPICE models, the influence of the interface traps and the oxide-trapped charge could not be separated. As already stated, the initial assumption of this research was that, as in the case of MOSFET-based logical circuits [29], most of the oxide-trapped charge would recover after 100°C annealing, while at the end of the 150°C annealing only the interface traps would remain. In discrete bipolar transistors, the interface states would recover first, after the annealing at 100°C–200°C, while the oxide-trapped charge would start to recover at higher temperatures, following the isothermal annealing at 150°C–300°C [14]. Taking into account the arguments presented in the previous chapters and paragraphs of this research, it seems that, indeed, the oxide-trapped charge in the tested circuits, at most, recovered after long-term room-temperature and short-term 100°C annealing. Nevertheless, there were no principal differences in the results obtained at the beginning of irradiation and at the end of the three annealing sequences, either in the model of the serial PNP power transistor or in the response of the entire L4940V5 voltage regulator. So, the results obtained may be used only for characterization of the total power transistor's and voltage regulator's radiation and post-irradiation response, rather than making it possible to qualitatively separate the effects of the interface traps and the oxide-trapped charge.

6 Conclusion

Data on the more than decade long examinations of the radiation tolerance of L4940V5 voltage regulators were unified and extended with the newly procured isothermal annealing results. These COTS, automotive circuits, demonstrated unexpectedly high radiation hardness during the previous experiments, potentially qualifying them as a cheap replacement for specially designed rad-hard power integrated circuits. The same samples, exposed to the γ-radiation more than ten years ago, were further analysed after long-term, room-temperature annealing, followed by two sequences of short-term, high-temperature annealing. The circuit response gave a unique opportunity to analyse exclusively the radiation hardness of the vertical serial PNP power transistor, since the small-signal, control circuit was marginally affected by ionising radiation.

A broad ensemble of the experimental data enabled the creation of a credible SPICE model, successfully describing the circuit response in the γ-radiation field. The initial phase of irradiation, up to 200 Gy, was efficiently recreated using the variations of the maximum forward emitter current gain and the knee current of the serial PNP power transistor. The data and computer simulation showed significant agreement for load cur-

rents of 100 mA, 400 mA and nearly 800 mA, for various input voltages. The subsequent exposure to γ-radiation could not be successfully modelled, due to the expressed saturation of the serial transistor's excess base current. The current limit protection of the driver NPN transistor further affected the circuit response.

Ten-year room-temperature annealing of integrated circuits, irradiated up to 500 Gy, caused the great recovery of the voltage regulator's quiescent current, yet followed by the further degradation of the maximum output current. The primary reason for the described response was the mutual recovery of the oxide-trapped charge and the build-up of interface traps above the emitter area of the serial PNP power transistor. On the other hand, two successive, one-week, high-temperature annealing periods caused the tremendous recovery of all the irradiated voltage regulators, reducing the circuit degradation down to the level specified after absorption of the total dose of 50 Gy.

The initial phase of irradiation caused the voltage regulator to degrade primarily through the influence of the oxide-trapped charge. The second phase of irradiation is a consequence of the activation of the overcurrent protection of the NPN driver transistor, followed by the saturation of the trapped charge density. Despite the relatively high doping concentration of the P-type emitter area in the vertical PNP power transistor, increased surface recombination in the area of the interdigitated emitter was the primary cause of the sharp increase in the serial transistor's excess base current.

Saturation of the serial transistor's excess base current after long-term, room-temperature annealing prevented the efficient modelling of this post-irradiation response. On the other hand, in most cases the response to the high-temperature annealing could be faithfully modelled in the same manner as during the initial phase of the voltage regulator irradiation.

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