Original scientific paper
https://doi.org/10.33180/InfMIDEM2018.401

Informacije MIDEM
Journal of Microelectronics,
Electronic Components and Materials
Vol. 48, No. 4(2018), 197 – 203

Proficient Static RAM design using Sleepy Keeper Leakage Control Transistor & PT-Decoder for handheld application

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Abstract: Due to their large storage capacity and small access time static random access memory (SRAM) has become a vital part in numerous VLSI chips. Low power adequate memory configuration is a standout among the most challenging issues in SRAM design. As the technology node scaling down, leakage power utilization has turned into a noteworthy issue. In this paper a novel power gating technique, namely sleepy keeper leakage control transistor technique (SK-LCT) is proposed for a handheld gadget application. The SRAM architecture has two primary components, specifically SRAM cell and sense amplifier. The proposed SK-LCT technique is applied in both SRAM cell and sense amplifier for a new low power high speed SRAM architecture design. The outline of SRAM architecture utilizing pass transistor decoder (PT-Decoder) gives better outcomes in term of power. Simulation is done using Tanner EDA tool in 180nm technology and the results demonstrate a noteworthy change in leakage power utilization and speed.

Keywords: SRAM; SK-LCT Technique; sense amplifier; Tanner EDA; Leakage Power

Načrtovanje učinkovitega statičenega RAMa z uporabo tranzistorja za kontrolo uhajalne moči z ohranjanjem stanja in PT dekoderja za ročne aplikacije

Izvleček: Zaradi visoke pomnilne kapacitete in kratkih dostopnih časov so statični pomnilniki z naključnim dostopom (SRAM) postali bistveni del VLSI čipov. Nizka moč zadostne konfiguracije pomnilnika je ena od najzahtevnejših problemov v zasnovi SRAM. V članku je predstavljena nova tehnika uporabe tranzistorja za nadzor uhajanja moči z ohranjanjem stanja (SK-LCT) za uporabo v ročnih aplikacijah. Arhitektura SRAM ima dve primarni komponenti, SRAM calico in tipalni ojačevalnik. Predlagana tehnika SK-LCT se uporablja tako v celici SRAM kakor v tipalnem ojačevalniku za novo zasnovano arhitekturo SRAM z nizko močjo. Okvir arhitekture SRAM, ki uporablja prehodni tranzistorski dekoder (PT-dekoder), ki daje boljše rezultate v smislu moči. Simulacija se izvaja z orodjem Tanner EDA v tehnologiji 180 nm, rezultati pa kažejo na opazno spremembo v kontroli uhajanja in hitrosti.

Ključne besede: SRAM; SK-LCT tehnika; tipalni ojačevalnik; Tanner EDA; uhajalna moč

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1 Introduction

Very Large Scale Integration (VLSI) is the way towards incorporating a million of transistors inside a single microchip. Quick advancement in the VLSI design process brings about the expansion of densities of the integrated circuit [1]. With the progression of innovation that are occurring in the universe, the demand for large storage of data is increasing in a way that needs to be faster than the current advancement [2]. At the same time, increment of power dissipation has ended up the major impediment against the further advancement of VLSI circuits. In a computing framework, power utilization because of the memory gets to frequently constitute a prevailing part of the aggregate power utilization [3].

Static Random Access Memory (SRAM) is a critical part in the vast majority of the VLSI chips; it regularly expends a prevailing part of power in each chip. By decreasing the power of SRAM, the overall power of chips can be diminished. Because of the quadratic connection amongst power and supply voltage of transistors [4]; one of the most compelling strategies to diminish the power utilization is by lessening the supply voltage. The strong demand of SRAM memory in handheld gadgets, system on-chip (SoC) & high performance VLSI circuits, the reduction of power utilization is imperative. Owing to high bit-line swing requirement, the leakage power utilization of memory circuit is high. Sleep technique, stack technique, sleepy stack technique, sleepy keeper technique, lector technique, foot switch technique & double switch technique are probably the most regularly utilized power gating for leakage power reduction. To overcome the drawback of the above existing method, a novel strategy is recommended. In computerized frameworks, instructions are conveyed by means of binary levels. The decoder is broadly utilized in memory framework to change over n-bit twofold input code into m yield lines. The address input code from the central processor is utilized to trigger the memory storage location assigned by address code [5].

Low power consumption is essentially crucial parameter, so pass transistor based decoders have been used due to the low leakage and dynamic switching currents. Among the overall power consumption of memory circuit, static power dissipation plays an predominant role. (2) A novel power gating technique, namely SK-LCT technique (Sleepy keeper Leakage Control Transistor Technique) is proposed in order to reduce the static power dissipation. SK-LCT technique is the combination of sleepy keeper and LECTOR technique which is employed in the design of SRAM cell and sense amplifier. The SRAM architecture using a SK-LCT method and pass transistor decoder (PT-decoder) has several advantages over the ordinary SRAM's design with high speed and low power consumption. (1)

2 Literature survey

During standby mode, a large portion of the power is squandered in SRAM design; since leakage power maneuvers an overwhelming part in SRAM power utilization. SRAM cell, sense amplifier & decoder are the indispensable portion of memory design. Improper design of these elements contributes to influence the robustness of the memory device. Both memory access time and memory power dissipation are emphatically affected by a sense amplifier circuitry. The power gating technique such as sleep technique, stack technique, sleepy stack technique, sleepy keeper technique & lector technique are utilized to shrink the static power of the SRAM cell. In order to diminish leakage power & delay of sense amplifier; latch-type sense amplifier is designed using a foot switch technique & double switch Technique.

In sleep technique, "PMOS-S" sleep transistor is embedded between VDD & pull up network and "NMOS-S BAR" sleep transistor is embedded between the pull down network & ground. The wake up time of the sleep method has a considerable impact on the competence of the circuit [6]. Stack technique is state maintenance technique with the detriment of increased delay and area [7]. The divided transistor of sleepy stack technique increases the delay drastically & also limits the convenience of this technique [8]. In Sleepy Keeper Technique parallel connected PMOS and NMOS transistor is embedded between pull up network & VDD and pull down network & ground. Lector technique has two leakage control transistors (LCT1 &LCT2) which are inserted between the pull up & pull down network. It has a very low leakage power which results in a delay penalty [9]. The data retention issue occurs in the circuit, which can be minimized by placing sleep transistor [10].

The footer switch voltage latch sense amplifier (FS-VLSA) senses the voltage difference between the bit line voltage & bit line bar voltage and amplifies it to rail yield voltages. The footer switch current latch sense amplifier (FS-CLSA) senses the current difference produced by ΔVBL and amplifies it. By introducing an extra head switch (i.e. Double Switch PMOS Access & Double Switch NMOS Access) the invalid current paths in FS-VLSA can be expelled which introducing a complementary sense enable signal. Double switch transmission access-voltage latch sense amplifier (DSTA-VLSA) is used to remove the sensing dead zone of the memory [11].

Based on the specific combination of input levels, the decoder is initiated. The most commonly utilized decoders in the design of SRAM architecture are AND decoder, NOR decoder, pseudo NMOS decoder. The speed of the AND decoder is more proficient than other decoders with the disadvantage of high power consumption. The design of decoder using NOR gate prompts low power consumption with increased time lag. In pseudo-NMOS decoder static power dissipation dominates the circuit.

There is an indigence of a novel power gating technique & the decoder circuitry to overcome the disadvantages of the above issue in SRAM architecture. By

appropriate outline of SRAM cell, sense amplifier & decoder; the general execution of memory design can be advanced.

3 SK-LCT technique & PT decoder

SRAM architecture comprises of SRAM cell, sense amplifier, precharge circuit, row/ column decoder and write driver circuit. A novel sleepy keeper leakage control transistor technique (SK-LCT Technique) is proposed in order to design SRAM cell and sense amplifier circuitry. The decoder using pass transistor gives better outcomes in terms of static power. The SRAM architecture for handheld gadget application is designed using the SK-LCT method and pass transistor decoder (PT-decoder) has a few favorable circumstances over the conventional SRAM's outline with high speed and low power consumption.

3.1 Sleepy Keeper Leakage Control Transistor Technique (SK-LCT Technique)

To overcome the problem in SRAM architecture, a novel SK-LCT Technique is applied. The delay & power of the SRAM architecture can be further scaled down and the data retention can be preserved using this novel technique. (3)

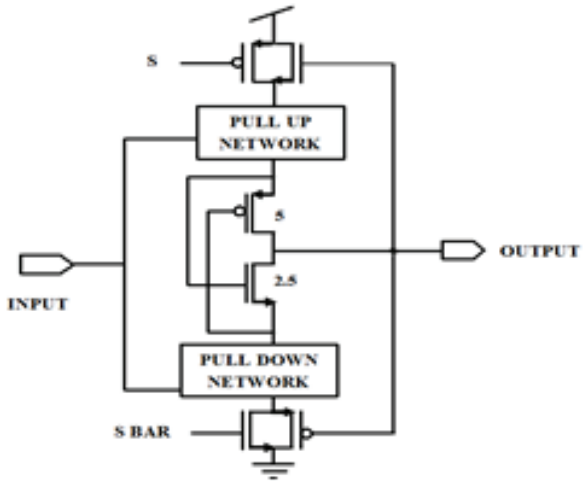

Figure1: SK-LCT Technique

Fig.1 illustrates the sleepy keeper leakage control transistor technique (SK-LCT Technique). Here, leakage control transistor (PMOS-LCT & NMOS-LCT) is placed in between pull up & pull down network. Both PMOS and NMOS are tied up parallel to preserve the stable retention in standby mode. The PMOS-LCT gate is associated with the drain of pull down network and NMOS –LCT gate is associated with the drain of pull up network. Hither, the sleep PMOS (S) transistor is put beneath VDD and sleep NMOS (S BAR) transistor is set over the ground. In sleep mode, parallel connected NMOS is the only terminal between pull up network & VDD and parallel connected PMOS is the only terminal between pull down network & ground. Sleep transistors cutoffs the power rails when the circuit is not in use while the state of circuit is saved by keeper transistors. This leads to the reduction of static power dissipation of memory circuit. The SRAM cell and sense amplifier are the two main fundamental components of SRAM Architecture; by outlining SRAM cell and sense amplifier using sleepy keeper-leakage control transistor (SK-LCT) technique low power high speed memory architecture can be obtained.

3.2 Pass Transistor Decoder (PT-Decoder)

Pass transistor decoder frequently requires less power consumption, runs faster and utilizes fewer transistors than a similar function implemented in complementary CMOS logic. The leakage power dissipation of PT-decoder is completely arrested. Fig. 2 demonstrates the pass transistor decoder.

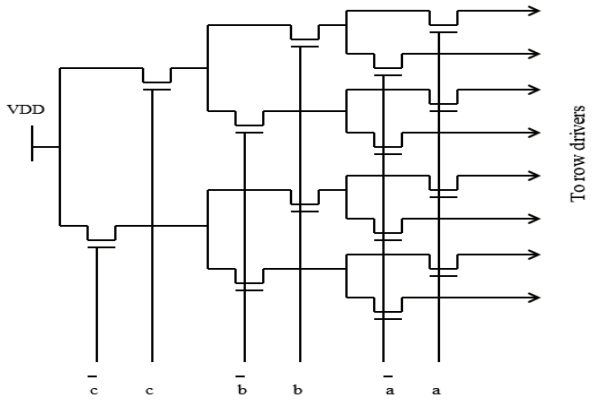

Figure 2: PT-Decoder

In memory design, the decoder is used to translate the given address and enable the particular row & column of the memory cluster. Row and column pass decoder is utilized to enable word line and write enable of a SRAM array. Based on the address line, specific memory cell is chosen and the data is read and written in the memory array.

4 Proficient static ram architecture

The low power and high speed SRAM architecture is outlined using sleepy keeper leakage control transistor (SK-LCT Technique) & pass transistor decoder. Fig. 3 illustrates the block diagram of SRAM architecture using the SK-LCT Technique & PT decoder. Initially, precharge

both the bit lines (BL & BLB) by using a precharge circuit. The storage location inside the memory devices are selected by the pass transistor decoder. By enabling the word line (WL) of the SRAM cell using PT-decoder, the data either '0' or '1' is stored. If data '1' is written in SRAM cell, BLB automatically discharges to '0' & BL remains high and vice-versa. Sense amplifier boosts the data in SRAM cell and acts as a read part circuitry. No change in the memory cell takes place during hold operation.

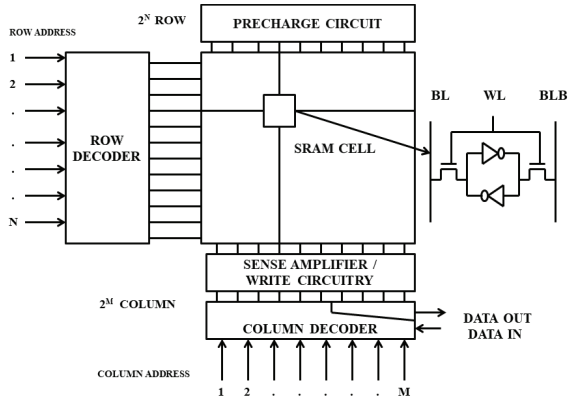

Figure 3: SRAM Architecture

Table 1 demonstrates the read and write operation of SRAM architecture. When word line (WL) and write enable circuitry (WE) is enabled, previous data is modified and new data is written in the memory. When either word Line (WL) or write enable circuitry (WE) is disabled, the previous data is hold in the memory. No change in the memory takes place during hold operation.

Table 1: Read and Write operation of SRAM

WRITE OPERATION		READ OPERATION	
WRITE '1'	Q=0, Q-bar=1 Word Line=1 Bit bar=0 Bit =1	READ '1'	Precharge both the bit lines Word line=1 Bit bar=0 (discharges to 0) Bit=1
WRITE '0'	Q=1, Q-bar=0 Word Line=1 Bit bar=1 Bit =0	READ '0'	Precharge both the bit lines Word line=1 Bit bar=1 Bit =0 (discharges to 0)

4.1 Design of SRAM cell using the SK-LCT Technique

SRAM cell is designed using the SK-LCT Technique to reduce the leakage power dissipation of memory. Fig. 4 illustrates SRAM cell the using the SK-LCT Technique. When word line (WL) is asserted high, access transistors are turned 'ON' for write operation. This connects the cell to two complementary bit lines columns (BL &BLB) and the data either '1' or '0' is written in the memory cell. When WL=0, SRAM cell is being inaccessible from both bit lines; keeping it in standby mode. This keeps prior stored value in the cell unchanged.(5)

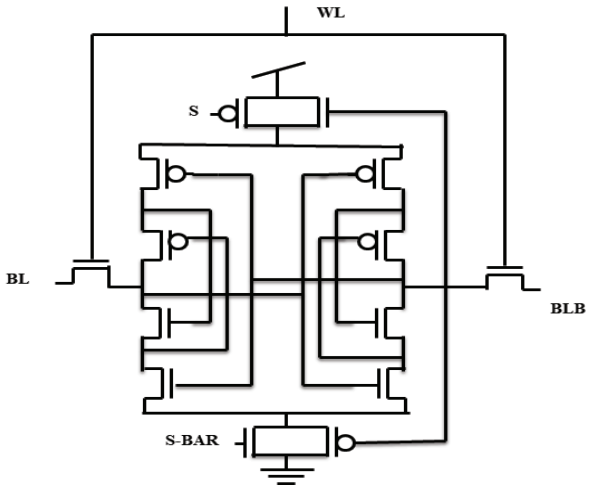

Figure 4: SRAM cell using SK-LCT Technique

4.2 Design of Sense Amplifier using the SK-LCT Technique

The power and delay of the voltage latch sense amplifier (VLSA) is reduced using SK-LCT Technique. Here, the additional transmission gate is inserted along with bit lines. During read mode, the PMOS sleep transistor(S) is activated to high and the NMOS sleep transistor(S-BAR) is activated to low; thus turning on the transmission gate and switching off the PMOS transistor whereas in standby mode the transmission gate is turned off and PMOS transistor turns on. Fig.5 illustrates voltage latch type sense amplifier using SK-LCT Technique.(6)

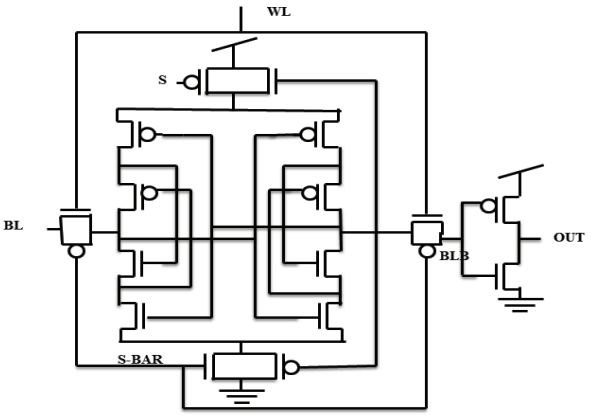

Figure 5: Sense Amplifier using SK-LCT Technique

4.3 Design of SRAM architecture using the SK-LCT Technique & PT-decoder

Fig:6 illustrates 4 bit SRAM architecture using the SK-LCT Technique and PT-decoder for handheld gadget application. Each column has a single precharge circuit in the memory array to precharge both bit lines (BL & BLB) to VDD during read and write operation. The address line of the memory is activated using row/column PT-decoder. SRAM cell using the SK-LCT Technique diminishes the leakage power dissipation of memory. When the word line (WL) is high, NMOS access transistors are turned 'ON' for write operation. This interfaces the cell to two complementary bit lines and the data either '1' or '0' is written in the memory cell. When WL=0, SRAM cell is inaccessible from both bit lines (BL & BLB). The write enable (WE) signal is turned on; when the write operation is intended. Otherwise, the WE signal isolates the bit lines from write drivers. The voltage difference between both the bit lines (BL&BLB) of voltage latch sense amplifier (VLSA) is sensed and amplifies the small voltage signal in the bit lines to conspicuous logic levels.

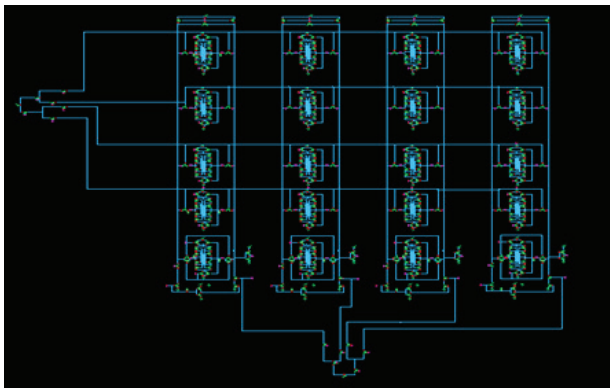

Figure 6: 16 bit SRAM architecture using SK-LCT Technique & PT-decoder

5 Results & discussion

The low power, high speed SRAM architecture is outlined using sleepy keeper leakage control transistor (SK-LCT Technique) & PT-decoder. The entire work is conveyed using Tanner EDA 180nm technology. The simulation result indicates the examination of various parameters like power consumption, leakage power and delay.

5.1 SRAM cell using the SK-LCT Technique

SRAM cell is designed using the SK-LCT technique to diminish the leakage power and improve the speed of the memory. If WL=1 and bit lines BL=1 (remains high, i.e. '1') & BLB=0 (remains low, i.e. '0'), data '1' is written in the SRAM cell. If WL=1 & bit lines BLB=1(remains high, i.e. '1') & BL=0 (remains low, i.e. '0'), data '0' is written in the SRAM cell. Fig.7 illustrates the simulation waveform of SRAM cell using the SK-LCT Technique

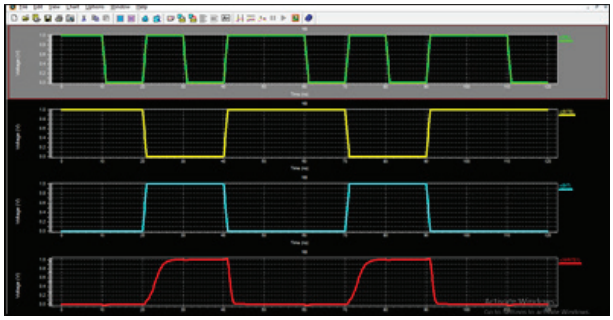

Figure 7: Simulation waveform for SRAM cell using SK-LCT Technique

Table 2 demonstrates the correlation of SRAM cell with power gating technique and without power gating technique. By utilizing the existing technique the static power and delay of the SRAM cell can be upgraded. A new power gating technique, namely SK-LCT Technique is proposed which saves 57.53% of **static power (7)** and 44.70% of delay compared to SRAM cell without power gating.

Table 2: Performance comparison of the SRAM cell

SRAM CELL		POWER	DELAY
WITHOUT POWER GATING		106.7 nW	1.0934ns
WITH POWER GATING	Sleep Technique	45.83 nW	0.7924ns
	Stack Technique	95.86nW	0.9556ns
	Sleepy stack Technique	68.58nW	1.0019ns
	Sleepy keeper Technique	89.18nW	1.0575ns
	LECTOR Technique	57.04nW	0.7069ns
	SK-LCT Technique	45.33nW	0.6041ns

5.2 Sense amplifier using the SK-LCT Technique

The voltage difference between both the bit lines (i.e. BL & BLB complement to each other) of the voltage latch sense amplifier (VLSA) is sensed and amplifies the small voltage signal in the bit lines to conspicuous logic levels. The data in memory cluster are greatly diminished & unstable, which can be boosted by using the amplifier circuitry. The simulation waveform for voltage latch sense amplifier using the SK-LCT Technique is illustrated in Fig.8

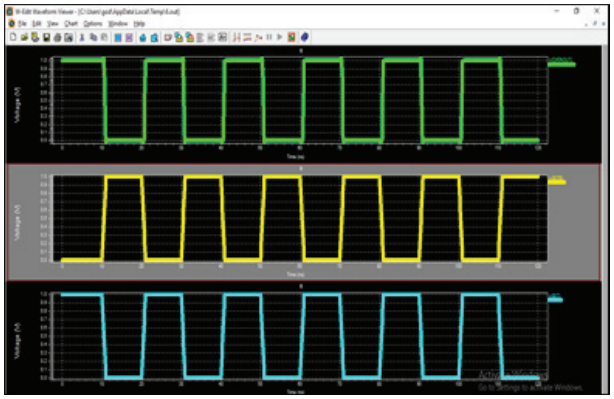

Figure 8: Simulation waveform for sense amplifier using the SK-LCT Technique

The Table 3 demonstrates the correlation of sense amplifier with power gating technique and without power gating technique. By using the existing technique the power and delay of the sense amplifier can be reduced. A novel technique, namely SK-LCT Technique is proposed which saves 93.65% of **static power (7)** and 95.26% of delay contrasted to a differential sense amplifier.

Table 3: Performance comparison of the Sense amplifier

SENSE AMPLIFIER		POWER	DELAY
WITHOUT POWER GATING	Differential Sense Amplifier	0.9034µW	4.2953ns
WITH POWER GATING	Footer Switch-VLSA	0.1556µW	0.25325ns
	Footer Switch-CLSA	0.8592µW	0.25328ns
	DSPA -VLSA	0.1708µW	0.25325ns
	DSNA -VLSA	0.6003µW	0.25325ns
	DSTA -VLSA	0.1401µW	0.23605ns
	SK-LCT Technique(VLSA)	0.0573µW	0.20328ns

5.3 PT-decoder

Based on the address line, particular memory cell is chosen and the data is read and written in the memory cluster. In memory design, the decoder is used to decode the given address and enable the particular row or column of the memory array. Row and column decoder is used to enable word line (WL) and write enable (WE). The speed of the PT–decoder is more proficient than other decoders with the advantage of low power consumption. The simulation waveform of pass transistor decoder is illustrated in Fig. 9.

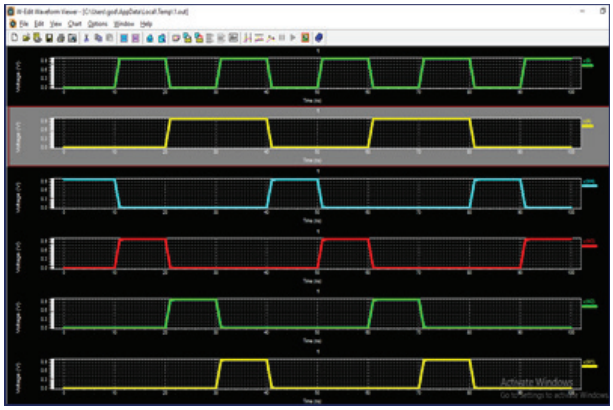

Figure 9: Simulation waveform for PT-decoder

Table 4 demonstrates the comparison of 2:4 decoder. The PT-decoder is more efficient both in power consumption & speed compared to other decoder.

Table 4: Performance comparison of Decoder

DECODER (2:4)	POWER	DELAY
AND Decoder	0.95229 mW	8.5113ps
NOR Decoder	0.23732 mW	29.990ns
Pseudo NMOS Decoder	11.1572 mW	25.206ps
Pass Transistor Decoder (PT-decoder)	8.33171 nW	1.9717ns

5.4 SRAM architecture using SK-LCT technique & PT-decoder

Figure 10: Simulation waveform for SRAM architecture

4 bit, 16 bit & 64 bit SRAM architectures are designed using the proposed SK-LCT technique & PT-decoder provides considerable reduction in leakage power and delay. Fig.10 illustrates the simulation waveform of SRAM architecture using write and read mode. By enabling the PT-decoder, data is written in any one of the memory cell (SRAM cell) and remaining SRAM cell is in hold mode (shut down mode). (4) The data is read by sense amplifier circuitry.

Table 5: Performance comparison of SRAM architecture

SRAM architecture	Without SK-LCT Technique & PT-Decoder		With SK-LCT Technique & PT-Decoder	
	POWER	DELAY	POWER	DELAY
4bit	37.422µW	25.458ns	9.7465µW	11.794ns
16 bit	53.526µW	46.736ns	13.615µW	22.571ns
64 bit	94.63µW	92.219ns	29.607µW	47.383ns

Table 5 demonstrates the performance comparison of 4 bit, 16 bit & 64 bit SRAM architecture using sleepy keeper leakage control transistor & PT decoder. The power & delay of memory architecture are limited using this novel technique. About, 68.71% of **static power (7)** & 44.83% of delay is reduced, which is more attractive than conventional SRAM architecture design.

6 Conclusion

SRAM cell design using the novel SK-LCT technique saves 57.53% of power and 44.70% of delay. Similarly, the sense amplifier design using the novel SK-LCT technique saves 93.65% of power and 95.26% of delay compared to conventional method. SRAM architecture using PT-Decoder is effective compared to other decoders. 4 bit, 8 bit & 64 bit memory architecture save 68.71% of power & 44.83% of delay and are intended for low power application such as handheld gadget. Therefore, from the simulation results it is observed that low power, high speed SRAM architecture for low power application is obtained using SK-LCT technique & PT-decoder.

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Arrived: 25. 04. 2018
Accepted: 11. 09. 2018