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Design of Low Power and Low Phase Noise Current Starved Ring Oscillator for RFID Tag EEPROM

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Abstract: Power dissipation of CMOS IC is a key factor in low power applications especially in RFID tag memories. Generally, tag memories like electrically erasable programmable read-only memory (EEPROM) require an internal clock generator to regulate the internal voltage level properly. In EEPROM, oscillator circuit can generate any periodic clock signal for frequency translation. Among different types of oscillators, a current starved ring oscillator (CSRO) is described in this research due to its very low current biasing source, which in turn restrict the current flows to reduce the overall power dissipation. The designed CSRO is limited to three stages to reduce the power dissipation to meet the specs. The simulated output shows that, the improved CSRO dissipates only 4.9 μW under the power supply voltage (VDD) 1.2 V in Silterra 130 nm CMOS process. Moreover, this designed oscillator has the lowest phase noise -119.38 dBc/Hz compared to other research works. In addition, the designed CSRO is able to reduce the overall chip area, which is only 0.00114 mm^2. Therefore, this proposed low power and low phase noise CSRO will be able to regulate the voltage level successfully for low power RFID tag EEPROM.

Keywords: CMOS, RFID, EEPROM, CSRO, power dissipation

Načrtovanje tokovno omejenga oscilatorja nizkih moči in nizkega faznega šuma za RFID EEPROM nalepke

Izvleček: Poraba moči CMOS IC je izredno pomembna pri napravah nizkih moči, posebej še pri spominu RFID nalepk. V spošnem, spomin nalepk, kot je elektronsko izbrisljiv in programirljiv EEPROM, potrebuje generator interne ure za reguliranje internega napetostnega nivoja. Poleg številnih tipov osclatorjev je v članku opisan tokovno omejen obročni oscilator (CSRO), saj zaradi omejitve toka, ki zmanjšuje porabo moči. Načrtan CSRO uporablja tri stopnje za doseganje specificirane porabe moči. Simuliran oscilator potrebuje 4,9 μW pri napajalni napetosti 1,2 V in realizaciji v 130 nm Silterra CMOS tehnologiji. V primerjavi z drugimi oscilatorji ima najnižji fazni šum -119,38 dBc/Hz in majhno površino 0,001144 mm^2. Predlagan oscilator je sposoben regulirati napetost EEPROM RFID nalepk.

Ključne besede: CMOS, RFID, EEPROM, CSRO, poraba moči

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1 Introduction

Radio frequency identification (RFID) is a detection system, where communications happen through radio waves to complete the data transmission/ reception process between the reader and tag [1]. In an RFID system, transponder contains an electronic microchip with three main blocks; like front-end digital baseband processor and the memory, where the product information's are stored inside the tag memory. The microchip is fabricated as a low power integrated cir-

cuit (IC), which employs a memory depending on the device features like ROM, RAM, non-volatile memory (EEPROM, Flash) and data buffers [2-4]. At present, a key design aspect for RFID transponder IC is the low power dissipation and low cost. Therefore, EEPROM is the most used tag memory, which is easily applicable to an RFID tag, DC-DC converter, SOC and FPGA system due to its advantages of low cost, low power and compatibility with the standard CMOS process [1].

In RFID, tag EEPROM, a clock driving circuit is required to maintain the internal voltage regulation. The clock signal in RFID systems is generated using a low power on-chip oscillator. In EEPROM, the oscillator is the major circuit that is required to generate a clock signal internally to regulate the voltages. Generally, the output frequency of the oscillator is a linear function of its control voltage. Therefore, the output frequency should be a function of the control voltages, which has a tunable range [5].

Among all the voltage-controlled oscillators (VCOs), current-starved ring oscillator (CSRO) has the popularity due to their easy integration. Moreover, this CSRO is an essential building block in EEPROM, which is commonly used in the clock generation. This internal clock generation is required to provide the input clock signals for voltage boost up the process. In addition, a very low current biasing source is required in CSRO to restrict the current flows in inverters inside the oscillation process to reduce the power dissipation [6].

This paper presents an improved CSRO circuit, which is suitable for the EEPROM voltage regulator in RFID tags. The design of a CSRO involves many important factors like frequency, power dissipation, chip area, phase noise etc [6]. Therefore, the design method of CSRO is discussed in this research, illustrates a three-stage CSRO. This paper is organized with the design method of the CSRO followed by the results and discussions. Finally, the comparison table is presented to show the better performance results compared to other research works.

2 Methodology

The memory of the RFID transponder requires a clock driving circuit to provide the clocks for the charge pump/voltage boost up circuit. The clock signal in EEPROM is generated using either the incoming carrier or an on-chip block [6]. Therefore, a ring oscillator is essential to get the low power on-chip and stable clock signals for RFID transponders memory performances. Moreover, a very low current biasing source is allowed through the inverters, which limits the current flow and reduces the power dissipation. A typical ring oscillator is constructed with a number of delay stages, where the output of the last stage feedback to the input of the first stage. In this scheme, the rings need to generate a phase shift of 2π, which should have the unity voltage gain in the oscillation frequency. In this research, a three-stage CSRO is proposed as shown in Figure 1, which follows the same operating phenomenon.

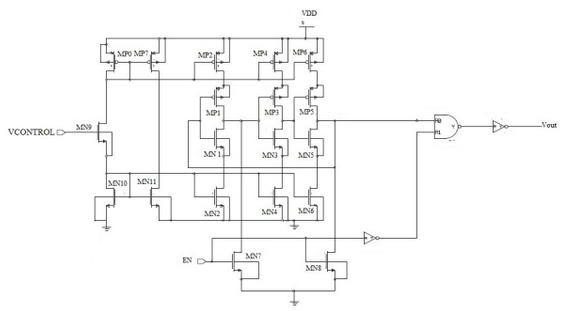

Figure 1: Schematic diagram of the proposed CSRO

MN1/MP2 is used to act as an inverter in the proposed design. On the other hand, MN2/MP2 acts as the mirror current source to limit the current flow through the inverter MN1/MP1. MP0, MP7, MN9, MN10 and MN11are required constructing a biasing circuitry for the oscillator. In this design, MP7/MN11 has the equal drain current, which is controlled by the input voltage VCONTROL and is mirrored to each level of the oscillator. In this proposed oscillator, an input pin EN is embedded with the main circuitry, which generates the reset signal for the chip. Moreover, when a power failure occurs from a certain level, this EN pin disconnects the chip. If the power supply voltage exceeds the required threshold, this EN pin generates a command signal to enable the chip operation. Therefore, the overall frequency of the proposed oscillator can be defined by the following equation.

$$f = \frac{1}{NT_D} = \frac{I_D}{NC_{equ}V_{DD}} \quad (1)$$

where, N is the stage number, T_D is the delay, C_{equ} is the single stage output equivalent capacitance, and VDD is the supply voltage.

In this proposed work, a three-stage CSRO is illustrated where some current starved inverters are involved to generate the oscillation frequency. In addition, to provide the bias current to the delay elements, an internal biasing circuitry with power switching in the conventional design is biased through this internal bias unit. This biasing circuitry delivers a range of control

voltages and helps to enhance the biasing voltage of the CSRO with maximum voltage variation, which ultimately elevates the sensitivity of the CSRO by engendering greater oscillation frequencies. On the other hand, designing a CSRO with frequency stability against temperature variation is another challenging task. Mostly, the threshold voltage in MOS transistors is one of the temperature dependent factors, which affects the oscillation frequency. As a result, to overcome this problem, the designed CSRO need to be controlled by a temperature independent source. Therefore, in this proposed design, a biasing unit is involved that generates the control voltage to the CSRO with minimum threshold voltage dependency and minimum temperature dependency.

3 Result and discussion

The proposed CSRO is designed and simulated in Mentor Graphics tool using Silterra 130 nm CMOS Process. To determine the operating frequency of the proposed CSRO circuit, the pre-layout simulated output frequency of the CSRO is shown in Figure 2. The operating temperature of the circuit is set to 27 ^{0}C.

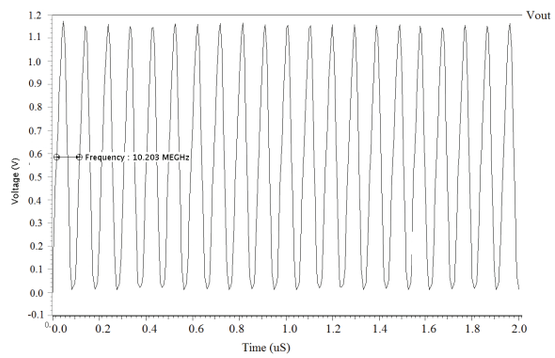

Figure 2: The simulated output of the proposed CSRO

From Figure 2 it is shown that, the proposed CSRO is achieved 10.2 MHz frequency when the control voltage is set to 1.2 V. The different transistor sizes of the proposed CSRO make it possible to get this desired frequency from the power supply voltage at 1.2 V. The operating temperature of the circuit is set to 27 ^{0}C. It is also illustrated from the figure that, the pre-layout simulation results also able to provide a full-swing oscillation signal with a supply voltage of 1.2 V.

To validate the proposed CSROs frequency range the design is simulated at different control voltages. Figure 3 shows the frequency deviation of the proposed CSRO circuit in terms of power supply deviations. Applying a range of power supply variation generates a frequency variation from 7 MHz to 11 MHz as shown in Figure 3. In this proposed design, it is observed that a non-linear relationship has been established due to the sensitivity of output frequency with respect to power supply variations. However, designing a CSRO with frequency stability against temperature variation is another challenging task

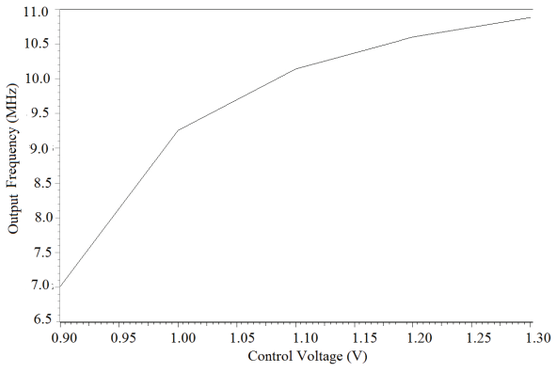

Figure 3: Tuning range of the proposed CSRO at 27 ^{0}C

As the improved CSRO is aimed to offer low power dissipation, the result shows that the power consumption of this design is only 4.9 µW. This result is superior to any recently published research works for RFID transponders memory clock generation. In our design, we have achieved a single side-band phase noise of −119.38 dBc/Hz at a 1MHz offset from the carrier as shown in Figure 4.

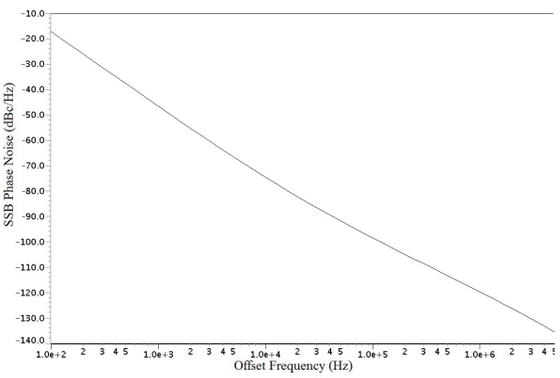

Figure 4: Single sideband (SSB) phase noise (PN) of the CSRO

In this design, a statistical analysis named Monte Carlo simulation is needed to calculate the impact of transistor and process variation mismatch. Therefore, a Monte-Carlo simulation with 100 runs is performed to validate the impacts. The results, shown in Figure 5, reveal that the designed current starved oscillator has an average frequency of 10.66 MHz with a standard deviation of 0.375 MHz.

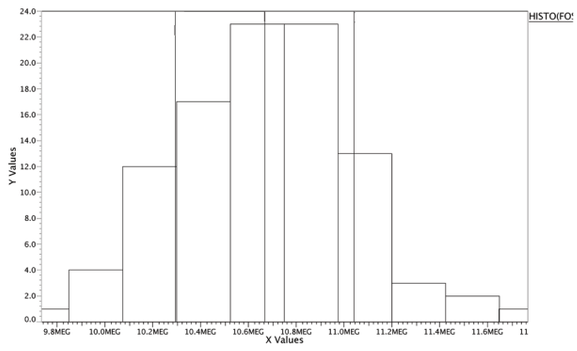

Figure 5: Monte Carlo simulations for oscillation frequency for ring oscillator

The principle of industry-oriented EDA tools (such as Mentor Graphics, Cadence, etc.) is expected to have the closest simulation result to the experimental result. Here, we have used Mentor Graphics to design, simulate, and draw the layout of our proposed design of CSRO. Therefore, the post-layout simulation will be expected to agree with the actual measurement result after IC fabrication. The layout design (Figure 6) has been sent for fabrication using standard 0.13 μm CMOS process including PADs and buffer circuit. A layout of the chip is shown in Figure 6, where the CSRO core occupies an area (without PADs) of 0.00114 mm^2. In this research, all the transistors have been placed in a way so that the mismatches and the area of the design can be reduced.

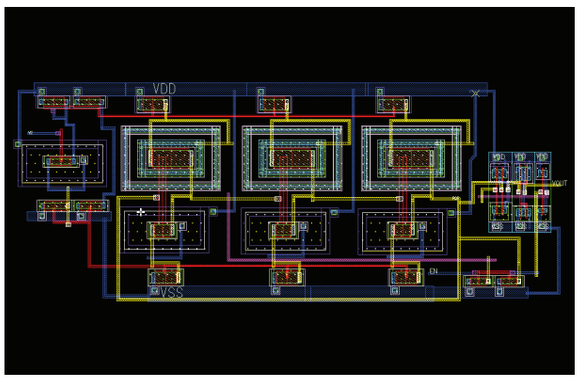

Figure 6: The layout of the proposed CSRO

Table 1: Performance comparisons of CSRO

References	Process (μm)	Power Supply (V)	Frequency (MHz)	P_{DC}, core (μW)	Phase noise (dBc/Hz)
[5]	0.13	1.3	28.2MHz-3.5GHz	590.88	-118@1MHz
[7]	0.18	0-1.8V	25.70 - 222.53	105.2	-
[8]	0.13	1.8	15.57	6000	-116.6@1MHz
[9]	0.18	1.8	1.02 GHz -3.99 GHz	7490	-80.17@ 1MHz
This Work	0.13	1.2	7-11	4.9	-119.38@1MHz

Table 1 summarizes the performance of the proposed CSRO along with other research works. In this research, a 10.2 MHz clock frequency is required to mitigate the requirements of the low power RFID tag EEPROM memory. Compared to all the research works shown in Table 1, the proposed CSRO has the lowest phase noise -119.38 dBc/Hz, which is the lowest compared to recently published research works with 10.2 MHz oscillation frequency. In addition, the proposed design has the lowest power dissipation only 4.9 μW compared to other research works, which makes the proposed design superior for low power applications. From the comparison in Table 1 it is found that, the proposed design has a small layout area, which eventually reduces the production cost.

In CMOS ring oscillators (single-ended or differential); a most common concern is the preferred method to generate better performance in terms of jitter, phase-noise, and total power dissipation. Single-ended CMOS ring oscillators phase noise and jitter are not strong functions of the number of stages [10-12]. However, the design is not done symmetrically or the design produces large noise, then a larger N will reduce the jitter. In general, the choice of the number of stages must be made based on several design criteria, such as 1/f noise effect, the desired maximum frequency of oscillation, and the influence of external noise sources.

4 Conclusion

An improved low power, low phase noise current-starved ring oscillator is presented in this research works. The design has only three inverter stages with the internal biasing method, which is required lower power, compared to other research works. The statistical analysis shows that the modified oscillator is able to produce the desired clock signal properly with different transistor sizing. Moreover, the comparison study shows that, the design has a lower phase noise -119.38 dBc/Hz@1 MHz offset from the carrier frequency. In addition, the simulated output shows that, the improved CSRO consumes only 4.9 μW power under supply voltage (VDD) 1.2 V in Silterra 130 nm CMOS process, which

is the lowest among previous research works. Finally, the working frequency for clock generation, which is 10.2 MHz and the small chip are make this proposed CSRO suitable for the voltage regulation of the low power application like RFID tag EEPROM.

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