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Design and Performance Analysis of Hybrid SELBOX Junctionless FinFET

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Abstract: In this work, the performance of selective buried oxide junction-less (SELBOX-JL) transistor at a FinFET structure is analysed using numerical simulations. The proposed structure exhibits better thermal resistance (R_{TH}), which is the measure of the self-heating effect (SHE). The DC and analog performances of the proposed structure were studied and compared with the conventional and hybrid (or inverted-T) JLFinFETs (JLTs). The I_{ON} of the hybrid SELBOX- JLFinFET is 1.43x times better than the ION of the JLT due to the added advantage of different technologies, such as 2D-ultra-thin-body (UTB), 3D-FinFET, and SELBOX. The proposed device is modeled using sprocess and simulation study is carried using sdevice. Various analog parameters, such as transconductance (g_m), transconductance generation factor (TGF = g_m/I_{DS}), unity current gain frequency (f_T), early voltage (V_{EA}), total gate capacitance (C_{gg}), and intrinsic gain (A_0), are evaluated. The proposed device with a minimum feature size of 10nm exhibited better TGF, f_T, V_{EA}, and A_0 in the deep-inversion region of operation.

Keywords: Junctionless FinFET, Hybrid SELBOX-JLFinFET, Self heating, f_T, TGF.

Analiza zasnove in učinkovitosti hibridnega brezspojnega SELBOX FinFET-a

Izvleček: V članku je analiziran brezspojni SELBOX-JL transistor v FinFET strukturi. Predlagana struktura izkazuje boljšo termično upornost, ki je merjena preko lastnega segrevanja. DC in analogne lastnosti predlagan strukture so primerjanes konvencionalnimi in hibridnimi strukturami. Tok hibridnega SELBOX-JLFinFET je 1.43-krat boljši kot pri JLT zaradi uporabe drugačne tehnologije, kot je 2D ultra tanko ohišje, 3D-FinFET in SELBOX. Ocenjeni so številni parametri, kot je transkonduktanca, generacijski faktor transkonduktance, frekvenca tokovnega ojačenja, zgodnja napetost, skupna kapacitivnost vrat in osnovno ojačenje.

Ključne besede: Brezspojni FinFET, hibridni SELBOX-JLFinFET, lastno segrevanje, f_T, TGF.

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1 Introduction

Silicon on insulator (SOI) MOSFETs has numerous advantages over bulk MOSFETs such as low parasitics, better isolation, radiation hardness, improved speed, ability to operate at low V_{DD} and higher environmental temperatures [1, 2]. The improved gate control over the channel causes FinFETs to demonstrate reduced short channel effects (SCEs), such as drain-induced barrier lowering (DIBL), when compared to MOSFETs [3,4]. However, the performance of the conventional FinFETs is overshadowed by hybrid FinFETs by effective utilization of the device area. A higher drain current is attained in hybrid FinFET by employing the unused area in conventional FinFET. The added advantages of the SOI and ultra-thin body (UTB) technologies enable the hybrid FinFET to have more drain current for the same fin width (W_{fin}) and gate length (L_g) when compared to conventional FinFETs. Zhang et al. proposed hybrid FinFET [5] and was later explored by Fahad et al. in [6]. Subsequently, the impact of high-k symmetric and asymmetric spacer, fin shape, and temperature on the performance of the hybrid FinFETs were analyzed by Pradhan et al. [7,8,9,10]; and the effect of self-heating on the performance of hybrid FinFETs was studied by Nelapati et al.[11].

Continuous scaling of electronic devices led to the difficulty of having sharp doping profiles in inversion mode (IM) transistors. Consequently, this led to the invention of the transistor without junctions. Colinge et al. [12] demonstrated a junctionless transistor (JLT), which is free from the junction and any doping gradients. A

comparative study of SOI-JLT and bulk JLT was carried in [13]. SOI-JLT is better than the bulk JLT but lacks in thermal conductivity due to the presence of silicon dioxide as a buried oxide. Self-heating in SOI devices can be reduced by replacing silicon dioxide with better thermally conductive materials or by modifying the device structure [14, 15]. Narayanan *et al.* proposed a modified SOI device structure for reducing the self-heating effect [16]. In this structure, the buried oxide is patterned in the selective region under the source and drain, and not continuously, which is referred to as the SELBOX structure. Uzma *et al.* presented a comparative study of planar SELBOX and SOI junctionless transistors [17].

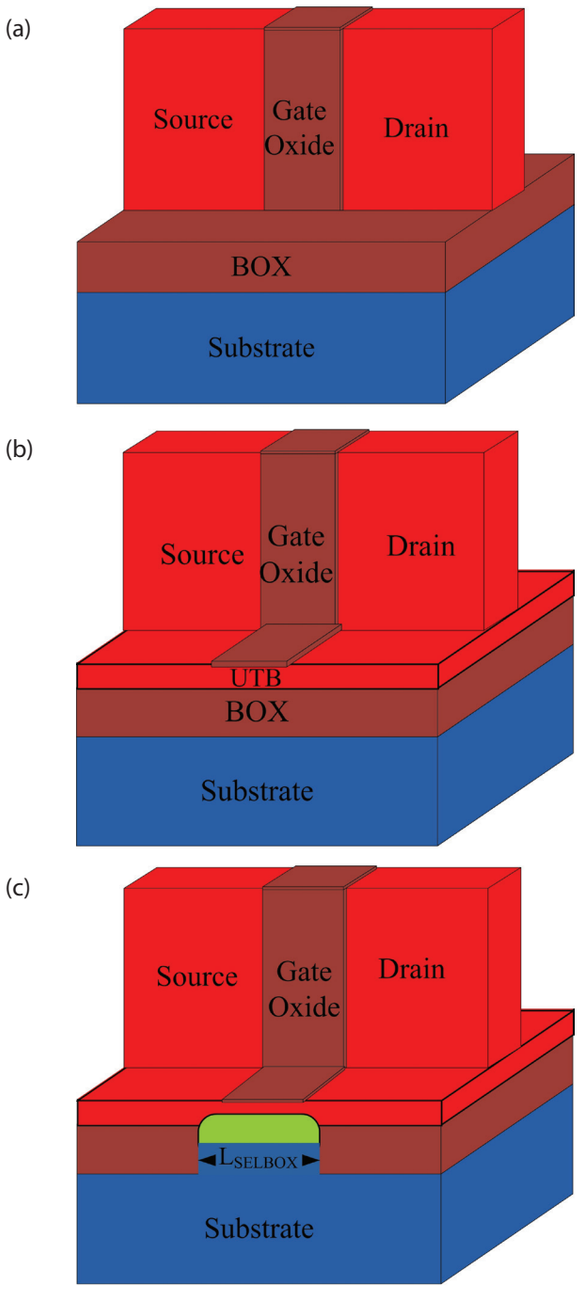

Figure 1: (a) Coventional JLT (SOI-JLT) (b) HJLT (c) HSJLT.

In this work, we analyzed the performance of hybrid SELBOX-JLFinFET (HSJLT), which is immune to self-heating and delivers higher drain current. The proposed structure adds the advantage of UTB, SOI technology, and SELBOX structure. Figure 1 depicts the 3-D view of conventional JLT, hybrid JLFinFET (HJLT), and HSJLT. The DC and analog performance of HSJLT are evaluated and compared with conventional and hybrid JLTs. The rest of the paper is organized as follows: Section 2 discusses the process flow of the proposed device and the simulation setup. Section 3 discusses the DC characteristics, self-heating effect, and analog performance of HSJLT and the comparison of simulation results with conventional and hybrid JLTs. The conclusions are drawn in Section 4.

2 Process flow and Simulation Setup

Figure 2 shows the process flow adopted for modeling the proposed HSJLT using sentaurus process (sprocess) [18]. Silicon material is defined as a substrate with underlying doping of boron ($5x10^{18}$ cm^{-3}). The insulating material, SiO_2, is deposited as a buried oxide on the selective regions by masking. The device structure after the BOX patterning is shown in Figure 2(a). The silicon material for the fin is deposited as shown in Figure. 2(b) with uniform doping of arsenic ($1x10^{19}$ cm^{-3}) and by masking, followed by etching the fin of the transistor is defined as shown in Figure. 2(c). HfO_2 is deposited as shown in Figure 2(d), which serves as the gate dielectric. Figure 2(e) shows the device structure after the deposition of the gate metal and spacer material. Finally, the metallization is carried for the contact of the source and drain, as shown in Figure 2(f).

Table 1 shows the device specifications and doping profiles of the three devices considered for the simulation. The OFF current (I_{OFF}), of the three devices shown in Figure 1, is adjusted to ≈ 1pA by tuning the gate metal work function (GWF). The GWF for conventional JLT, HJLT, and HSJLT is 4.72eV, 4.87eV, and 4.7eV, respectively. The GWF of HJLT is larger because the ultra-thin body transistor in hybrid devices will be turning on early when compared to fin transistor [6]. The GWF of HSJLT is smaller when compared to HJLT because the planar transistor's gate is depleted in HSJLT by both GWF and the depletion region formed by the oppositely doped substrate [19].

The sentaurus device (sdevice) is used to conduct device simulations [20]. Mobility degradation models,

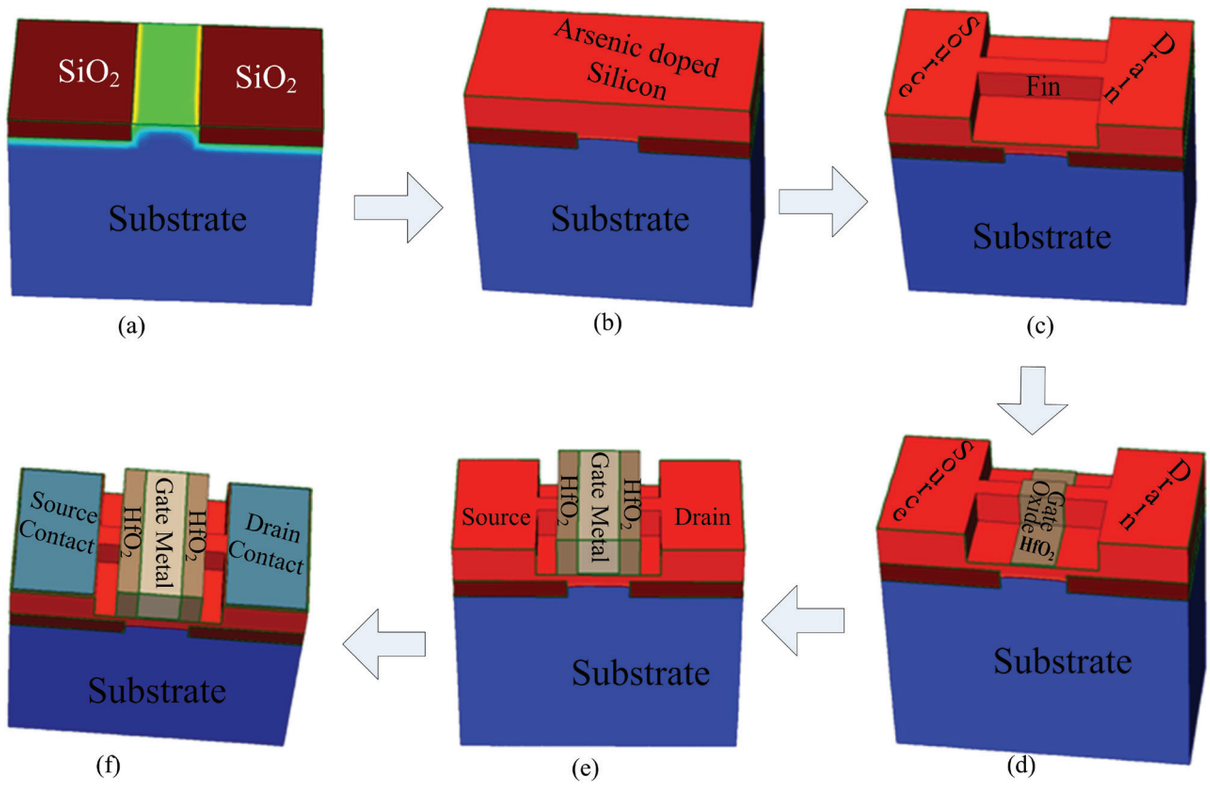

Figure 2: The process flow of the proposed HSJLT using Sprocess, device structure (a) after deposition of the buried oxide (b) after epitaxial growth of silicon for fin (c) after definition of the fin (d) after gate oxide (HfO_2) deposition (e) after gate metal and spacer deposition (f) after contact definition

such as transverse field (to account for degradation at interfaces), high field saturation (to account for velocity saturation effect), and doping dependence (to account for impurity scattering effect), are considered along with default carrier transport model for the device simulation. Shockley – Reed – Hall (SRH) recombination and Auger recombination models are included to account for the recombination of electrons and holes. Old-slotboom band-gap narrowing model is incorporated due to the high doping of the channel. The self-heating effect is accounted for by the inclusion of Auger recombination models, SRH (temperature dependent), and the thermodynamic model for carrier transport. The simulator is verified by the excellent fitting of transfer characteristics of SOI junctionless transistor with the experimental data presented in [12]. Figure. 3 shows the calibration of simulation results with experimental data.

Table 1: Device parameters and doping profiles.

Parameter	JLT	HJLT	HSJLT
Gate length (L_g)	20nm	20nm	20nm
Fin height (H_{fin})	20nm	Hfin–UTB = 16nm	Hfin–UTB = 16nm
Fin width (W_{fin})	10nm	10nm	10nm
Effect oxide thickness (EOT)	0.9nm (HfO_2)	0.9nm (HfO_2)	0.9nm (HfO_2)
Ultra-thin body (UTB) thickness	-	4nm	4nm
Spacer length	10nm (HfO_2)	10nm (HfO_2)	10nm (HfO_2)
Selbox length (L_{SELBOX})	-	-	10nm to 40nm
BOX thickness	10nm	10nm	10nm
Fin dopants (Arsenic)	1 X $10^{19}cm^{-3}$	1 X 10^{19} cm^{-3}	1 X 10^{19} cm^{-3}
Substrate dopants (Boron)	1 X 10^{15} cm^{-3}	1 X 10^{15} cm^{-3}	5 X 10^{18} cm^{-3}
Gate metal workfunction (GWF)	4.72eV	4.87eV	4.7eV

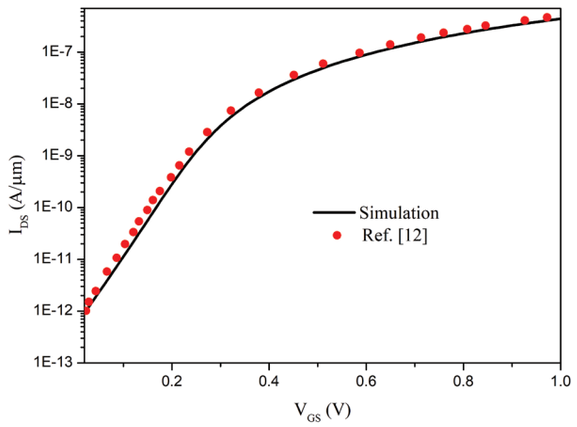

Figure 3: Calibration of I_{DS} – V_{GS} characteristics of the SOI junctionless transistor with the experimental data [12] at V_{DS} = 1V and L_g = 1μm.

3 Results and Discussions

Figure 4 shows a comparison of the transfer characteristics of the three device structures calibrated to the same I_{OFF}. Figure 4 shows that the HJLT and the HSJLT deliver maximum drain current due to the added advantage of UTB and fin structures. HSJLT delivers more drain current than HJLT because of the lower threshold voltage (V_{TH}) and low GWF.

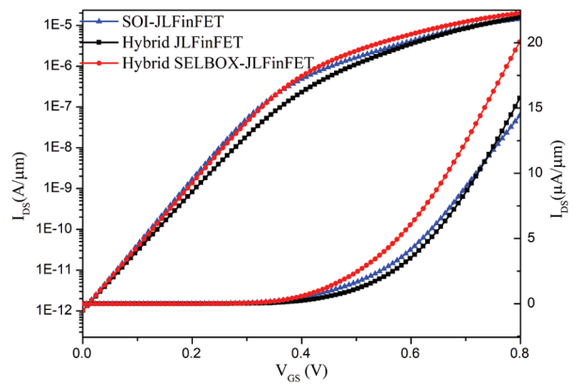

Figure 4: Comparison of transfer characteristics of SOI-JLFinFET, hybrid JLFinFET, and hybrid SELBOX-JLFinFET at L_{SELBOX} = 20nm, V_{DS} = 0.8V and calibrated to same I_{OFF} = 1pA.

3.1 DC performance of HSJLT

In this section, the DC performance of the HSJLT is studied for different SELBOX lengths (L_{SELBOX}) at the same V_{TH}. The variations of ON current (I_{ON}), I_{OFF}, sub-threshold slope (SS), DIBL, lattice temperature, and R_{TH} in HSJLT are presented for different L_{SELBOX} and compared with the conventional and hybrid JLTs.

Figure 5 shows the variation of I_{ON} with the increase in L_{SELBOX}. L_{SELBOX} is the gap between the edges of the BOX material shown in Figure 1(c). As L_{SELBOX} increases, the I_{ON} of the HSJLT decreases due to the penetration of the depletion region into the active area. HJLT is a particular case of HSJLT, in which the L_{SELBOX} is zero. In hybrid transistors, the conduction of current is due to UTB transistor and fin transistor, and the UTB transistor turns on earlier than the fin transistor [6]. For the same threshold voltage, the GWF required for HSJLT is lower than the HJLT due to the depletion region provided by the SELBOX structure. Comparatively low GWF of HSJLT makes its fin transistor to turn early when compared to the fin transistor of HJLT, due to which the I_{ON} is less in HJLT when compared to HSJLT for L_{SELBOX} being < 40nm.

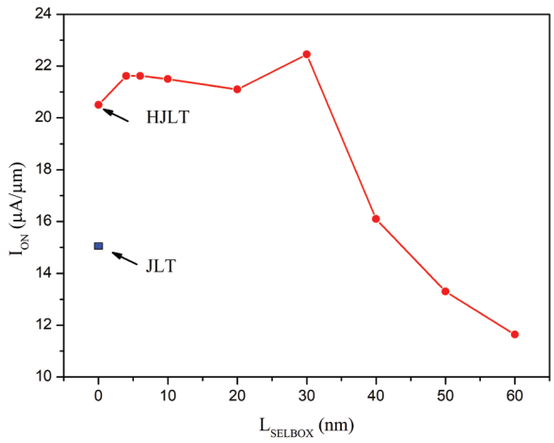

Figure 5: Variation of I_{ON} for different L_{SELBOX} of HSJLT at L_g = 20nm, V_{DS} = 0.8V, and V_{GS} = 0.8V.

Figure 6 shows the variation of I_{OFF} and I_{ON}/I_{OFF} for different L_{SELBOX}. I_{OFF} decreases as L_{SELBOX} increases due to the tight control of the GWF at the top and the depletion region at the bottom of the planar transistor [17].

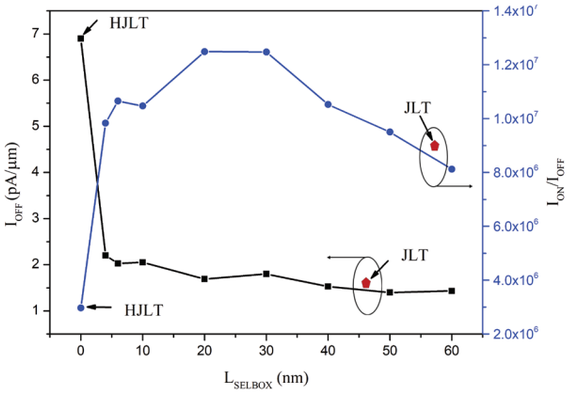

Figure 6: Variation of I_{OFF} and I_{ON}/I_{OFF} for different L_{SELBOX} of HSJLT at L_g = 20nm, V_{DS} = 0.8V.

Initially for L_{SELBOX} < 30nm, I_{ON}/I_{OFF} ratio increases with an increase in L_{SELBOX} and this ratio decreases for L_{SELBOX} > 30nm because I_{ON} drops significantly compared to I_{OFF}.

Figure 7 and Figure 8 show the variation of the SS and DIBL for different L_{SELBOX} of HSJLT. SS and DIBL decrease as the L_{SELBOX} increases due to the increase in gate control over the active region caused by an effective increase in the depletion region provided by the SELBOX at the bottom of the UTB transistor. SS and DIBL in HJLT are high because of non-uniform V_{TH} [6].

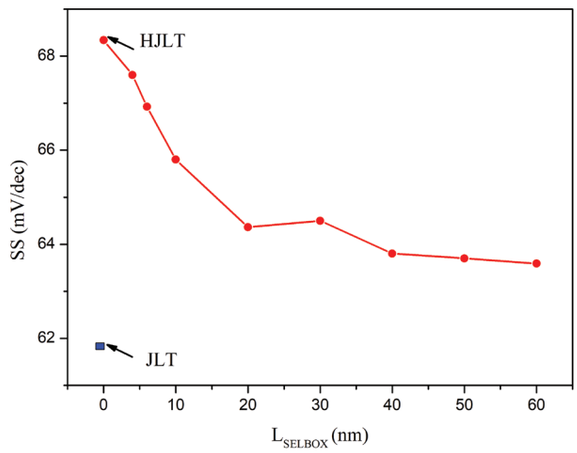

Figure 7: Variation of SS for different L_{SELBOX} of HSJLT at L_g = 20nm, V_{DS} = 50mV.

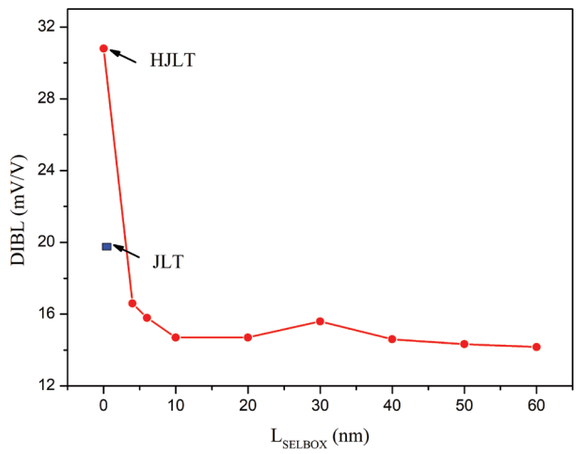

Figure 8: Variation of DIBL for different L_{SELBOX} of HSJLT at L_g = 20nm, $V_{DS,linear}$ = 50mV, $V_{DS,saturation}$ =0.8V.

Figure 9 and Figure 10 depict the variation of thermal resistance (R_{TH}) and lattice temperature for different L_{SELBOX}. Thermal resistance can be used to measure the immunity to self-heating of the device; more RTH, less immunity to self-heating. R_{TH} depends on the power dissipated ($P_{dissipated}$ = V_{DD} x I_D) and lattice temperature ($T_{lattice}$), as shown in Eq. (1). Thermal resistance and lattice temperature decrease with an increase in L_{SELBOX}. An increase in LSELBOX results in an increase in the cross - section area for heat to dissipate into the substrate. In conventional JLT, the lattice temperature is lower compared to hybrid SELBOX - JLTs due to the former transistor's low drain current.

$$R_{TH} = \frac{(T_{lattice} - 300)}{P_{dissipated}} \quad (1)$$

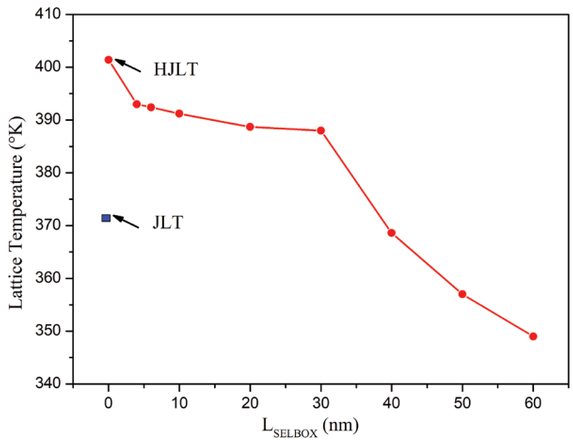

Figure 9: Variation of lattice temperature for different L_{SELBOX} of HSJLT at L_g = 20nm, V_{DS} = 0.8V, V_{GS} = 0.8V.

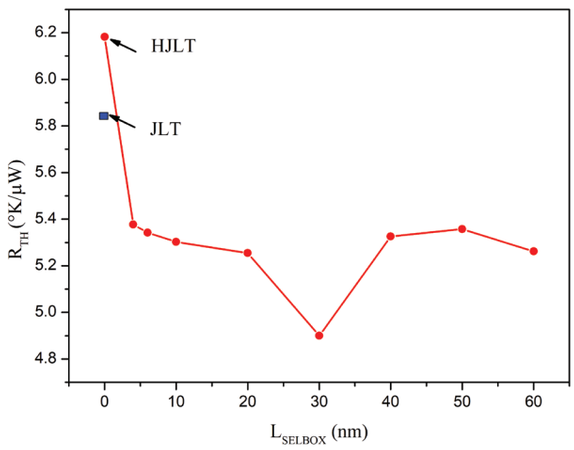

Figure 10: Variation of thermal resistance for different L_{SELBOX} of HSJLT at L_g = 20nm, V_{DS} = 0.8V, V_{GS} = 0.8V.

From the simulation results discussed in section 3.1, it can be observed that the HSJLT exhibits a better performance at $L_{SELBOX} \approx L_g$, i.e., 20nm. It exhibits high I_{ON}, improved DIBL, and low R_{TH} when compared to conventional JLT.

3.2 Analog Performance of HSJLT

This section presents the analog performance of HSJLT at L_{SELBOX} = 20nm. The analog figure of merits (FOM),

such as transconductance (g_m), unity gain frequency (f_T), transconductance generation factor (TGF), early voltage (V_{EA}), and intrinsic gain (A_0) of HSJLT, are compared with conventional and hybrid JLTs.

Figure 11 shows the transconductance variation concerning the change in the gate voltage of the three devices for the same I_{OFF}. The transconductance of HSJLT is higher than conventional and hybrid JLTs because of the high-low field mobility of the former transistor. The higher the g_m, the better the device's analog performance. Figure 12 shows the variation of the transconductance generation factor of the three devices with the change in I_{DS}. TGF is the measure of the efficiency of the transistor to convert the drain current into transconductance; it also indicates the region of operation of the device [21]. From Figure 12, it can be observed that HSJLT exhibits a higher TGF than conventional and hybrid JLTs at the same drain current when the devices are in moderate or strong inversion (i.e., I_{DS} > 1E-7 A/μm).

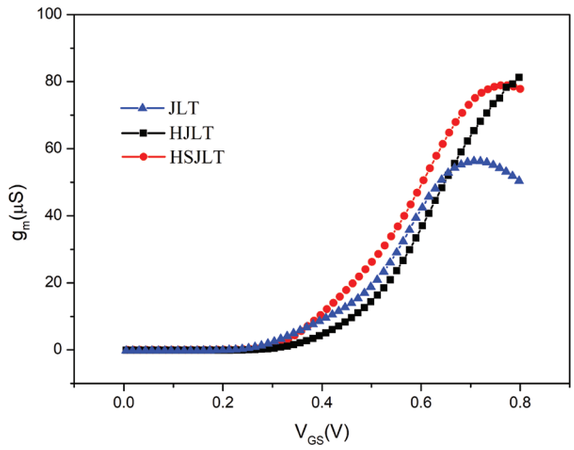

Figure 11: Transconductance variation of JLT, HJLT, and HSJLT with a change in the gate voltage.

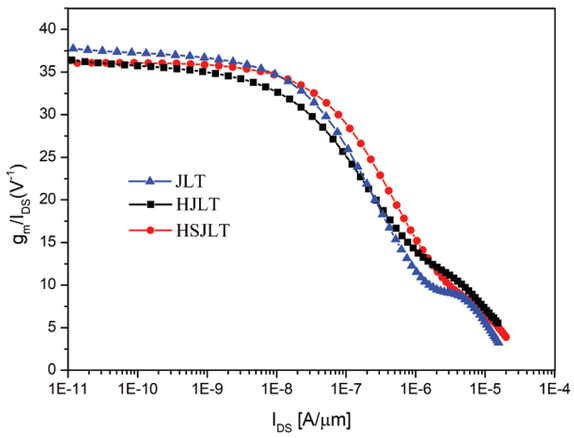

Figure 12: TGF as a function I_{DS}/(W/L) in JLT, HJLT, and HSJLT.

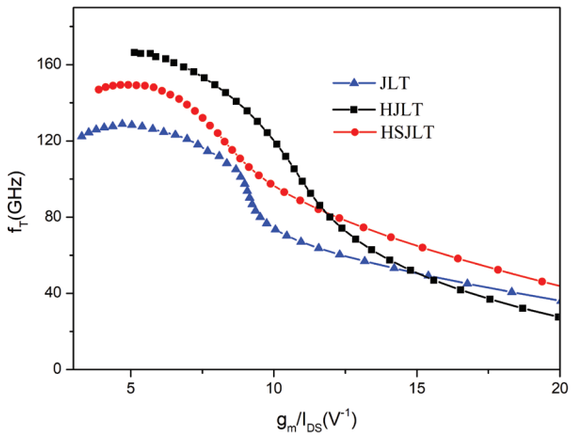

Figure 13: Variation of f_T as a function of TGF in JLT, HJLT, and HSJLT.

Figure 13 shows the variation of f_T as a function of g_m/I_{DS}. f_T depends on the total gate capacitance and transconductance, as shown in Eq. (2). HSJLT exhibits higher f_T than conventional JLT, but lower f_T than HJLT at moderate or strong inversion (i.e., g_m/I_{DS} < 10) due to the large gate capacitance of theHSJLT, as shown in Figure 14, and dipping of the transconductance. In deep-strong inversion (i.e., 10< g_m/I_{DS} >20), f_T of HSJLT is higher when compared to the other two devices because of higher g_m.

$$f_T = \frac{g_m}{2\pi C_{gg}} = \frac{g_m}{I_{DS}} \bullet \frac{I_{DS}}{2\pi C_{gg}} \quad (2)$$

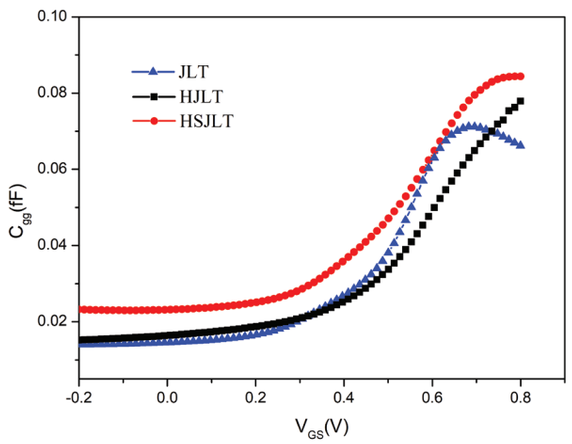

Figure 14: Gate capacitance dependence on the gate voltage in JLT, HJLT, and HSJLT.

Figure 15 shows the variation of early voltage (V_{EA}) as a function of TGF for JLT, HJLT, and HSJLTs. V_{EA} is the drain current - to - drain conductance (g_d) ratio and is an important analog performance metric as it determines the transistor's intrinsic gain if TGF multiplies it.

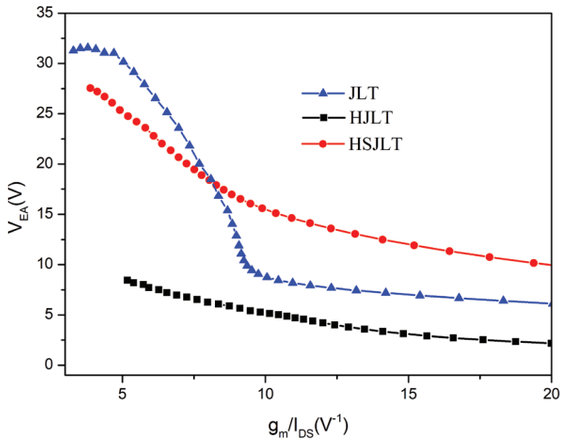

Figure 15: Early voltage dependence on the TGF in JLT, HJLT, and HSJLT.

It can be observed from Figure 15 that in a moderate or strong inversion region, conventional JLT has larger V_{EA} than the HSJLT, because of the low drain conductance of the conventional JLT. In a deep-strong inversion region, HSJLT exhibits higher V_{EA} than conventional JLT, due to the high drain current and nearly the same drain conductance as shown in Figure 16.

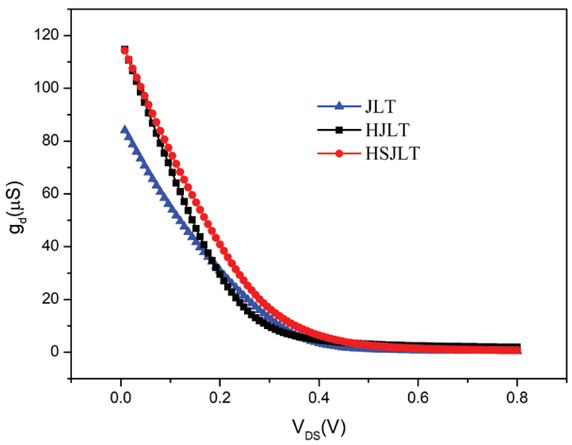

Figure 16: Drain conductance versus drain voltage of JLT, HJLT, and HSJLT.

Figure 17 shows the variation of intrinsic gain (A_0) as a function of TGF. Due to better transconductance generation factor and early voltage, conventional JLT provides high intrinsic gain compared to HSJLT in moderate or strong inversion region. HSJLT has a high intrinsic gain in the deep - strong inversion region than the other two devices.

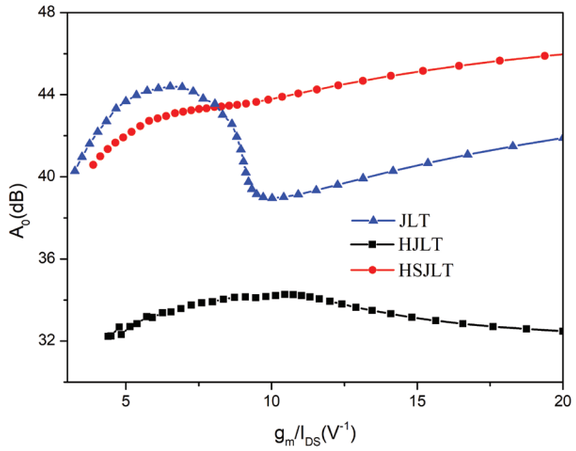

Figure 17: Variation of intrinsic gain in JLT, HJLT, and HSJLT as a function of TGF.

4 Conclusions

In this paper, the DC characteristics and the analog performance of the proposed HSJLT are presented. This paper illustrates the impact of variation in L_{SELBOX} of the proposed structure on the I_{ON}, I_{OFF}, SS, DIBL, and thermal resistance. It is found from the simulation results that the proposed device architecture shows better DC performance for $L_g \approx L_{SELBOX}$. Within the same device area, the proposed device delivers 1.43 times higher drain current compared to conventional JLT due to combined technologies (UTB, FinFET, SELBOX). Simulation results show that the hybrid SELBOX- JLFinFET exhibits better immunity to self-heating when compared to conventional and hybrid JLFinFETs. The analog figure of merits, such as TGF, early voltage, and intrinsic gain, is evaluated through the simulations. It can be concluded from the simulation results that the hybrid SELBOX-JLFinFET is an option for high-performance applications due to higher I_{ON} and it exhibits better g_m/I_D, f_T, V_{EA} and intrinsic gain than the conventional and hybrid JLFinFETs.

5 References

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