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An LTspice simulation model of gamma-radiation effects and annealing in a voltage regulator with a lateral serial PNP transistor with round emitters

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Abstract: The aim of this paper was to determine the reasons for a complex radiation response of the commercial-off-the-shelf LM2940CT5 low-dropout voltage regulator. Examination of this circuit in a gamma-radiation environment disqualified its use when operated with relatively high output currents, while its radiation tolerance was satisfactory when load current was approximately one-tenth (or lower) of the nominal value. In order to obtain a more thorough insight into the radiation response of this integrated circuit, a detailed SPICE model was developed. This model enabled mutual comparison of the influence of serial and driver PNP power transistor parameters: forward emitter current gain, knee current and emitter resistance. The serial lateral PNP power transistor with round emitters was identified as the weakest element that crucially affected the entire circuit radiation tolerance. The effects of gamma-radiation were examined for total doses up to 500 Gy followed by three sequences of annealing. Detailed characteristics of Beta(Ic) were procured for four different kinds of bias and load conditions during irradiation. The emitter resistance increase of the serial power transistor was a primary reason for the low radiation tolerance of the entire voltage regulator; it was much more influential than the perceived decline of the PNP power transistor forward emitter current gain.

Keywords: lateral PNP transistor; radiation effects; annealing; SPICE model; voltage regulator

LTspice simulacijski model vplivov gama žarkov in žganja v napetostnem regulatorju z lateralnim PNP tranzistorjem z okroglimi emitorji

Izvleček: Namen članka je določitev vzrokov kompleksnega sevalnega odziva napetostnega regulatorja LM2940CT5. Regulator je v okolju z gama radiacijo in relativno visokimi izhodnimi tokovi neuporaben, pri izhodnem toku pod desetino nazivnega pa je njegova uporaba zadovoljiva. Za natančno analizo je bil zgrajen natančen SPICE model. Model omogoča medsebojno primerjavo parametrov serijskega in napajalnega tranzistorja. Izkazalo se je, da je serijski lateralni tranzistor najšibkejši člen vezja. Analize so bile opravljene za dozo radiacije gama žarkov do 500 Gy. Izrisane so bile natančne karakteristike za štiri kombinacije napajanja in bremena. Primarni vzrok netolerance na gama žarke je dvig upornosti emitorja.

Ključne besede: lateralni PNP tranzistor; vpliv radiacije; žganje; SPICE model; napetostni regulator.

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1 Introduction

Voltage regulators are widely used for electronic circuit power supply in aerospace, nuclear and military systems [1-4], where a harsh radiation environment heavily affects the electron devices' reliability [5]. Low-dropout voltage regulators are particularly important in battery-powered systems [6].

Usually, low-dropout voltage regulators are bipolar or BiCMOS circuits, which are based on bipolar transistors as the basic components. A considerable part of the voltage regulator chip is occupied by power transistors [3, 4], in both serial and driver element roles. PNP power devices are usually used to achieve a very low dropout voltage on the serial transistor. Due to the large area

of these transistors, high perimeter-to-area ratio and thick isolation oxide, in many cases power transistors are considered to be the most vulnerable elements of power integrated circuits to ionising radiation [7]. Vertical power transistors are generally preferred to lateral ones due to their lower vulnerability to radiation effects that affect the oxide above the base area [8]. Nevertheless, in some cases the use of power integrated circuits with lateral PNP transistors cannot be avoided; further, there are specially designed radiation-tolerant analogue integrated circuits based on these power elements [9-11].

During the previous years, detailed research was conducted in order to define the topologies of cheap, commercial-off-the-shelf (COTS) low-dropout voltage regulators suitable for implementation in radiation environments instead of specially designed "rad-hard" components [12-17]. Among these candidates was a LM2940CT5 voltage regulator, an automotive circuit with lateral PNP power transistors with round emitters. Nevertheless, experimental results clearly indicated that these commercial integrated circuits had low radiation tolerance [12-14, 16]. In the same period, examinations indicated that the specially designed, rad-hard LM2941W circuits exhibited high radiation tolerance [11]. This circuit is, in its basic topology, very similar to the LM2940CT5 circuit, so it would be justified to expect the COTS voltage regulator to demonstrate much higher radiation tolerance than what was recorded. Thus, an effort was made to examine the reasons for the low LM2940CT5 voltage regulator radiation tolerance, and this effort led to the development of a detailed simulation model of this integrated circuit.

2 Theory

Ionising radiation primarily affects bipolar transistors by reducing their forward emitter current gain, namely by a base current (I_B) increase. This excess base current (ΔI_B: difference between base current, created by the influence of radiation, and its pre-irradiation value, I_{B0} [7]) is a direct consequence of charge trapping in the isolation oxide above the base area as well as the charge trapped in the interface between the silicon and silicon dioxide. Excess base current may be approximated by the following equation [18, 19]:

$$\Delta I_B \approx \frac{qV_T n_i P_E \Delta s(D)}{2E_M} e^{\left(\frac{V_{EB}}{2V_T}\right)} \quad (1)$$

where: q – elementary electron charge ($1.6 \cdot 10^{-19}$ C), n_i – intrinsic carrier concentration in silicon, P_E – length of the emitter perimeter, $\Delta s(D) = s(D) - s(0)$ – change of the surface recombination velocity, a function of the absorbed total dose of ionising radiation D, V_{EB} – emitter-base voltage, E_M – electric field at the point of the maximum recombination of the space charge region and V_T – thermal voltage (25.9 mV at 20°C).

General expression regarding a concentration of the oxide-trapped charge, N_{ot}, is [20]:

$$N_{ot} = \sqrt{\frac{2\varepsilon_{Si} n_S}{q}\left(V_T \ln\left(\frac{n_S}{n_i}\right) - \frac{V_{tr}}{2}\right)} \quad (2)$$

where: ε_{Si} – permitivity of silicon ($1.04 \cdot 10^{-12}$ F/cm), n_S – surface electron concentration in the base area, V_{tr} – emitter – base transition voltage from the ideality factor $m < 2$ to $m = 2$. Transition voltage is defined for the surface potential in the base area ψ_s, being $\psi_s = V_{EB}/2$.

Using relation (2), a simplified model for a maximum electric field in the space-charge region was developed [18]:

$$E_M = \sqrt{\frac{2qn_S}{\varepsilon_{Si}}\left(V_T \ln\left(\frac{n_S}{n_i}\right) - \frac{V_{EB}}{2}\right)} \quad (3)$$

Therefore, in model, basically found on equations (1) and (3), excess base current is directly related to the surface recombination velocity and, consequently, to the interface traps concentration [18]:

$$\Delta N_{it} \approx \Delta I_B \frac{2E_M}{q\sigma v_{th} V_T n_i \pi P_E} e^{\left(\frac{V_{EB}}{2V_T}\right)} \quad (4)$$

where: σ – carrier capture cross section, v_{th} – carrier thermal velocity.

Nonetheless, limitation of the model described by equation (4) is taking into account only the surface recombination effects, thus neglecting the effects of the oxide trapped charge above the base area, as well as the effects of interface traps on the semiconductor surface potential. In order to take into account also some other effects, improved model for the excess base current was recently introduced [21], emphasizing the effects of interface traps on the N-type base area surface potential, ψ_S [21]:

$$\Delta I_B = \Delta I_{R-SCR} + \Delta I_{R-NBS} = \frac{qV_T \pi n_i P_E \Delta s(D)}{2E_M} e^{\left(\frac{V_{EB}-R_S I_E}{2V_T}\right)} + \\ + \frac{qn_i^2 P_E W_B \Delta s(D)}{2n_S(\psi_S)} \left[e^{\left(\frac{V_{EB}-R_S I_E}{2V_T}\right)} - 1 \right] \quad (5)$$

where: $\Delta I_{R\text{-}SCR}$ – surface recombination base current, $\Delta I_{R\text{-}NBS}$ - neutral-base-surface recombination current, R_s – the series resistance between the base and emitter, I_E – emitter current, W_B – base width.

As may be seen from equation (5), even this sophisticated model primarily takes into account interface traps [21]. Thus, its authors frequently neglected the influence of the oxide-trapped charge on the excess base current, since a positive charge trapped in the oxide layer opposes the electrostatic impact of the interface traps on the surface carriers recombination [21].

The next cause of transistor parameter degradation is charge trapping in oxide and at interfaces above emitter areas, yet the influence of these effects is not as well defined as charge trapping above the base area [19]. In PNP transistors, oxide trapped charge (during the initial period of irradiation) suppresses the negative effects of interface traps, primarily due to the accumulation of N-type base [9]. On the other hand, oxide trapped charge and interface traps have additive negative effects on the P-type emitter area [8]. Unbiased bipolar PNP transistors are the most sensitive to ionising radiation [8]. Further, high load current, which can significantly increase the chip temperature, leads to the tremendous recovery of the trapped charge and, therefore, may prevent irradiated circuit failure [4]. These effects are even more prominent in lateral PNP transistors, where both base and emitter areas are situated directly below the oxide.

After ionising radiation exposure, post-irradiation effects commence in bipolar transistors and related integrated circuits [22]. At room temperature, trapped charge tunneling is a dominant effect, while at approximately 100°C a more pronounced oxide trapped charge recovery commences [7]. Interface traps are more stable defects, so their annealing happens at 150-250°C and higher temperatures [7]. In some bipolar integrated circuits it is possible to roughly exclude the oxide trapped charge influence, where oxide trap annealing occurs at approximately 100°C. Applying even higher temperatures therefore leads to partial recovery of the interface traps [22]. The bipolar integrated circuit degree of recovery (or further degradation) after irradiation also depends on bias conditions (both during the irradiation and the following annealing), absorbed total dose, dose rate (particularly due to enhanced low-dose-rate sensitivity (ELDRS) effect), a quality of the implemented oxides, technological processes, concentration of impurities, et cetera [7].

3 Materials and methods

3.1 Experiment

A COTS LM2940CT5 circuit was used as a representative of a low-dropout voltage regulator with lateral PNP power transistors. This circuit, made by *National Semiconductor*®, has two power transistors, comprised of a multitude of parallel connected elementary lateral PNP transistors with round emitters: the serial and driver transistor [23]. The serial transistor is comprised of 350 elementary transistors, while the driver transistor is made by parallel connection of 70 PNP transistors of the same type [23, 24]. Each elementary transistor has a structure with a round emitter (13 μm in diameter) and may provide an output current of nearly 3 mA [24].

Voltage regulators were exposed to ionising radiation in the Vinča Institute of Nuclear Sciences, Belgrade, Serbia. Samples were irradiated in the vicinity of a ^{60}Co gamma-radiation source, at a dose rate of 40 mGy(SiO_2)/s. After absorption of the predefined total doses, irradiation was temporarily interrupted, and electrical characteristics of samples were examined. Then, irradiation was continued and this procedure was repeated until samples absorbed a total dose of 500 Gy(SiO_2). Integrated circuits were irradiated with various bias and load conditions: without bias during irradiation (V_{IN} = 0 V, I_{OUT} = 0 A), then with input bias voltage and negligible load (V_{IN} = 8 V, I_{OUT} = 1 mA), moderate load (V_{IN} = 8 V, I_{OUT} = 100 mA) as well as with input bias voltage and high load current (V_{IN} = 8 V, I_{OUT} = 500 mA).

Following absorption of the specified total dose, irradiated integrated circuits were kept in an office locker at room temperature for nearly ten years. After 85,000 hours, samples were again tested with the same laboratory setup in order to examine the influence of the long-term room-temperature annealing. Then, a seven-day annealing in a thermal chamber was performed at 100°C. After another round of experiments, a final annealing sequence in a thermal chamber was performed for 168 hours at 150°C.

Electrical characteristics of LM2940CT5 voltage regulators were obtained through examination of maximum output current and minimum dropout voltage (at two operating points: output currents of 100 and 400 mA). The maximum output current was detected for an in-

put voltage of 8 V DC, when output voltage declined to 4.7 V DC [12, 13]. Minimum dropout voltage (for I_{OUT} = 100 mA) was determined for a constant output current and the output voltage of 4.9 V [12, 15]. For the second operation point, when I_{OUT} was 400 mA, most of the performed measurement output voltages did not reach 4.9 V. Accordingly, results were recorded for the maximum available output voltage [16].

More details about the experimental procedures, dosimetry and radiation sources may be found in the literature [12-17, 25, 26].

3.2 Computer simulation

Previous research demonstrated myriad possibilities for the use of the open-source SPICE simulation tools for examination of radiation effects in bipolar integrated circuits [27-29]. Thus, a detailed computer simulation model was created with *LTspice IV* software [30], according to the schematic circuit diagram published in the manufacturer's data sheet [23]. The focus in the simulation model was on analysis of radiation and post-irradiation power transistor responses, i.e., serial and driver transistors. For every predefined absorbed ionising dose and period of annealing, forward emitter current gain, knee current and emitter ballasting resistance were changed for both serial and driver transistors.

Since the filter capacitor of the power source had a low value (nominally 330 µF [14, 17]), there was a large AC component of the input voltage. Due to the influence of parasitic capacitances and inductances of the power supply cables (10 m long), as well as the inevitable difference between the simulation model and the real integrated circuit, it was not sufficient to simply transfer measured filter capacitance to the *LTspice* model. Thus, in order to establish a faithful simulation model, the filter capacitor value was adjusted until the AC component of the input voltage measured during the experiment and the voltage obtained by simulation matched exactly for all the examined cases (this value was 440 µF for all the tested LM2940CT5 circuits).

Simulation of the maximum output current proceeded when the adequate filter capacitor was determined. Output current, as well as input and output voltages in the simulation model had to be approximately the same as in every particular point of the experiment. Serial and driver transistors had the same values for the forward emitter current gain, but different values for knee current and emitter resistance. Since the serial transistor had five times more elementary PNP transistors than the driver transistor, the driver transistor knee current was five times lower, whilst its emitter resistance was five times greater than for the serial transistor. In order to obtain an exact match between experimental and simulation results on the maximum output current (approximately V_{IN} = 8 V DC, V_{OUT} = 4.7 V DC), the values of the emitter resistance were precisely determined, with the accuracy in the range of 0.1 mΩ.

When these three parameters were successfully selected (forward emitter current gain (β_F), knee current (I_{KF}) and emitter resistance (R_{E12})) and simulation of the maximum output current experiment was evaluated as acceptable, simulations then determined the minimum dropout voltage. The same schematic circuit diagram had been used for two further simulations, regarding the dropout voltage with constant output currents, being 400 mA and 100 mA. If there were unacceptable disagreement in these two models with experimental results, simulation of the maximum output current was repeated, and β_{F12}, I_{KF12} and R_{E12} were determined again. Only when simulations of all three types of experiments were estimated to be satisfactory, parameters of the serial and driver transistors were accepted as true values that enabled successful modelling of γ-radiation and post-irradiation effects at all the measurement points, for all absorbed total doses and types of annealing. The above procedure was performed for all predefined control points for both irradiation and post-irradiation periods. Thus, according to the implemented simulation models, $\beta(I_c)$ characteristics were generated for all four bias and load conditions for the serial power transistor.

4 Results

The results that unify examination of the maximum output current and minimum dropout voltage, recorded in LM2940CT5 voltage regulators, are summarised in Table 1. Previously published results were complemented by the new experimental results on post-irradiation effects. Since the internal consumption currents, i.e., the voltage regulator no-load quiescent currents (I_{Q0}), were in all cases approximately the same, only the values, procured during examination of the maximum output current, are presented in Table 1. In order to obtain a complete review of the LM2940CT5 voltage regulators, the basic parameters of the serial and driver transistors, obtained by computer simulations, are included in Table 1.

As seen in Table 1, dropout voltage varied modestly, both during the irradiation and annealing. On the other hand, maximum output current variations were more substantial. Nevertheless, output voltage values decreased below the minimum acceptable value of 4.9 V while operating with a load current of 400 mA. There-

Table 1: Absolute values of input voltage (V_{IN}) and output voltage (V_{OUT}), procured during the experiment for determination of the serial transistor's minimum dropout voltage (V_{EC12}; tests with load current of 100 mA and 400 mA), as well as output current (I_{OUT}) and no-load quiescent current (I_{Q0}), procured during maximum output current (I_{MAX}) examination. Also the accompanying data on the serial transistor's excess base current (ΔI_{B12}) in the LM2940CT5 *National Semiconductor*® voltage regulator were enclosed, being a consequence of the exposure to the ionising radiation. Experimental results were extended with parameters of the serial and driver transistors (maximum forward emitter current gain (β_{Fmax}), knee current (I_{KF}) and emitter resistance (R_E)), defined in the *LTspice* simulation models. Successive periods of annealing are marked as follows: Ann.1: the first period of annealing (Θ_a = 20°C, t = 85,000 hours); Ann.2: the second period of annealing (Θ_a = 100°C, t = 168 hours); Ann.3: the third period of annealing (Θ_a = 150°C, t = 168 hours). Experimental values of I_{MAX}, V_{IN}, V_{OUT} and I_{Q0}, procured during the irradiation of LM2940CT5 voltage regulators, for total doses up to 500 Gy(SiO_2), were used from references [13], [15] and [16].

National Semiconductor® LM2940CT5		Type of experiment								Computer simulation				
Operation during irradiation and annealing		V_{EC12} (100 mA), V_{OUT} = 4.9 V		V_{EC12} (400 mA)			I_{MAX}			Parameters of PNP power transistors, Q_{12} and Q_2				
										β_{Fmax}	Parameters of the serial transistor, Q_{12}		Parameters of the driver transistor, Q_2	
Bias and load during irradiation	Dose, D [Gy]	V_{IN} [V]	ΔI_{B12} [mA]	V_{IN} [V]	ΔI_{B12} [mA]	V_{OUT} [V]	I_{OUT} [mA]	I_{Q0} [mA]	ΔI_{B12} [mA]		I_{KF12} [A]	R_{E12} [Ω]	I_{KF2} [A]	R_{E2} [Ω]
0 V,0 A	0	5.505	0	7.316	0	4.903	744.2	9.82	0	175	0.135	0.085	0.027	0.425
	50	5.501	0.06	7.485	0.11	4.782	424	9.73	-11.62	136	0.145	0.365	0.029	1.825
	100	5.439	0.24	7.921	0.08	4.785	439.4	9.61	-10.31	126	0.16	0.3457	0.032	1.7285
	200	5.471	0.45	7.39	1.47	4.721	391.5	9.37	-11.96	110	0.15	0.395	0.03	1.975
	300	5.465	0.7	7.169	2.41	4.72	392	9.13	-11.17	98	0.155	0.3798	0.031	1.899
	400	5.436	1.06	7.191	3.40	4.718	390.1	8.87	-10.33	78	0.17	0.35	0.034	1.75
	500	5.449	1.28	7.266	4.11	4.691	351.6	8.6	-11.76	66	0.17	0.3903	0.034	1.9515
	Ann.1	5.55	0.97	8.247	1.21	4.835	503.9	9.02	-4.91	84	0.22	0.238	0.044	1.19
	Ann.2	5.55	0.84	7.914	1.28	4.757	432.7	9.3	-9.37	96	0.195	0.3405	0.039	1.7025
	Ann.3	5.515	0.58	7.874	0.64	4.765	453.7	9.53	-9.1	107	0.185	0.319	0.037	1.595
8 V, 1 mA	0	5.569	0	7.468	0.00	4.904	702	9.43	0	170	0.14	0.112	0.028	0.56
	50	5.535	-0.06	7.902	-0.02	4.859	490	9.49	-7.76	165	0.13	0.29	0.026	1.45
	100	5.549	0.03	7.944	0.37	4.850	474.1	9.35	-7.96	157	0.13	0.304	0.026	1.52
	200	5.484	0.24	7.935	1.17	4.840	480.7	9.19	-6.76	143	0.13	0.284	0.026	1.42
	300	5.52	0.51	7.902	1.81	4.814	457.8	8.96	-6.86	114	0.16	0.306	0.032	1.53
	400	5.528	0.72	7.901	2.40	4.817	473.9	8.79	-5.35	93	0.2	0.28	0.04	1.4
	500	5.502	0.89	7.712	3.68	4.796	444.6	8.56	-5.94	78	0.22	0.3	0.044	1.5
	Ann.1	5.611	0.89	7.684	3.47	4.697	440.1	8.78	-6.34	78	0.235	0.316	0.047	1.58
	Ann.2	5.581	1.02	7.721	2.55	4.741	416.3	9	-8.37	72	0.26	0.35	0.052	1.75
	Ann.3	5.547	0.45	7.704	1.64	4.75	446.4	9.33	-8.07	116	0.175	0.3344	0.035	1.672
8 V, 100 mA	0	5.596	0	7.516	0	4.9	833.8	9.778	0	205	0.15	0.0415	0.03	0.2075
	50	5.578	0.27	8.007	-0.12	4.898	524.2	9.5	-8.26	160	0.145	0.263	0.029	1.315
	100	5.571	0.44	8.177	0.17	4.871	500.7	9.34	-8.56	151	0.145	0.2816	0.029	1.408
	200	5.536	0.82	8.077	1.68	4.863	495.2	9.08	-7.49	143	0.13	0.265	0.026	1.325
	300	5.519	1.08	7.903	2.66	4.845	488.9	8.81	-6.65	131	0.135	0.2648	0.027	1.324
	400	5.491	1.40	8.010	3.23	4.847	484.9	8.57	-5.80	105	0.16	0.2552	0.032	1.276
	500	5.496	1.64	7.871	4.14	4.847	495.8	8.37	-4.35	90	0.18	0.2269	0.036	1.1345
	Ann.1	5.705	1.37	7.695	4.61	4.681	433.8	8.55	-7.45	95	0.185	0.3263	0.037	1.6315
	Ann.2	5.632	1.32	7.847	3.27	4.692	401.1	8.86	-10.36	100	0.18	0.3877	0.036	1.9385
	Ann.3	5.624	1	7.905	2.11	4.724	428.3	9.2	-10.03	114	0.16	0.3473	0.032	1.7365

8 V, 500 mA	0	5.557	0	7.768	0	4.9	524	9.6	0	168	0.14	0.2638	0.028	1.319
	50	5.558	0.32	7.409	1.18	4.899	572.9	9.51	2.69	143	0.15	0.203	0.03	1.015
	100	5.56	0.49	7.602	1.45	4.9	575.9	9.34	4.01	136	0.145	0.187	0.029	0.935
	200	5.517	0.93	7.676	2.48	4.9	562.8	8.95	5.08	116	0.155	0.1821	0.031	0.9105
	300	5.556	1.02	7.867	2.98	4.87	518.1	8.63	4.22	92	0.185	0.208	0.037	1.04
	400	5.530	1.53	7.611	4.60	4.9	578.4	8.35	9.34	76	0.21	0.065	0.042	0.325
	500	5.508	1.81	7.704	4.96	4.9	569.1	8.17	9.56	66	0.25	0.03	0.05	0.15
	Ann.1	5.575	1.75	8.055	4.39	4.773	466.5	8.25	3.78	61	0.29	0.2438	0.058	1.219
	Ann.2	5.602	1.48	7.715	4.70	4.734	400.4	8.55	-0.57	66	0.22	0.332	0.044	1.66
	Ann.3	5.54	0.91	7.837	2.65	4.732	439	9.11	-0.48	89	0.22	0.3322	0.044	1.661

fore, these results highlight that, if the LM2940CT5 voltage regulator operated with only 10 % of the load current, it would be acceptable for implementation in a moderate radiation environment.

Taking into account data on the circuits, biased and heavily loaded during irradiation, the LM2940CT5 voltage regulator was acceptably radiation tolerant; its output voltage was maintained near the threshold of 4.9 V, while its characteristics sharply degraded only after removal from the radiation environment! There was also an unusual response of the excess base current (ΔI_B) during examination of the maximum output current. Excluding the heavily loaded circuits during irradiation, all other samples demonstrated negative values for the excess base current! Usually, in the radiation environment, base current increases as a consequence of ionising radiation exposure and then decreases during annealing. Such a response was indeed recorded during minimum dropout voltage examination (see Table 1), but the completely opposite response was recorded when voltage regulators were examined with the maximum output current.

In order to provide answers to these, seemingly contradictory results, a detailed computer simulation model was developed.

5 Discussion

5.1 Computer simulation

Detailed schematic circuit diagram that unified the experimental setup and LM2940CT5 voltage regulator internal structure is presented in Fig. 1, while a simplified version of the same test circuit was presented in Fig. 2. As a basis for development of the *LTspice* model of power transistors, the model of the discrete D45H11 PNP power transistor was used [31, 32]. This component is a 10 A power transistor with the following electrical characteristics: forward emitter current gain β_F = 40–60, emitter-collector breakdown voltage BV_{EC0} = 80 V and transition frequency (or gain-bandwidth product) f_T = 40 MHz [32]. Basic D45H11 transistor *SPICE* model was modified in order to meet the requirements

Table 2: SPICE parameters for serial (Q_{12}) and driver (Q_2) PNP power transistors based on the D45H11 transistor model [31]. Since the values of the forward emitter current gain (BF) and the forward knee current (IKF) were changed for every predetermined dose, their values are not included in the table.

SPICE parameters of PNP transistors Q_{12} and Q_2											
Parameter	Value	Unit	Parameter	Value	Unit	Parameter	Value	Unit	Parameter	Value	Unit
IS	7.8998e-11	A	Eg	1.1222	eV	TF	3.8976e-09	s	Cje	1.0308e-09	F
NF	0.851		BR	1.962		ITF	0.99999	A	Vje	0.6517	V
VAF	10.7084	V	Rb	4.7117	Ω	XTB	0.1376		Mje	0.3531	
Ise	4.797e-14	A	Rbm	0.2039	Ω	XTI	1.0316		Cjc	5e-10	
Ne	4		Irb	0.1086	A	XTF	1.3572		Vjc	0.4265	V
Nc	3.5938		Re	0.0001	Ω	VTF	0.9957	V	Mjc	0.2428	
Nr	1.295		Rc	0.1223	Ω	TR	4.9098e-07	s	Xcjc	0.8031	
VAR	23.2874	V	Vceo	80	V	PTF	0		Cjs	0	F
IKR	9.9963	A	Icrating	10	A	KF	0		Vjs	0.75	V
Isc	4.797e-14	A	FC	0.5335		AF	1		Mjs	0.5	

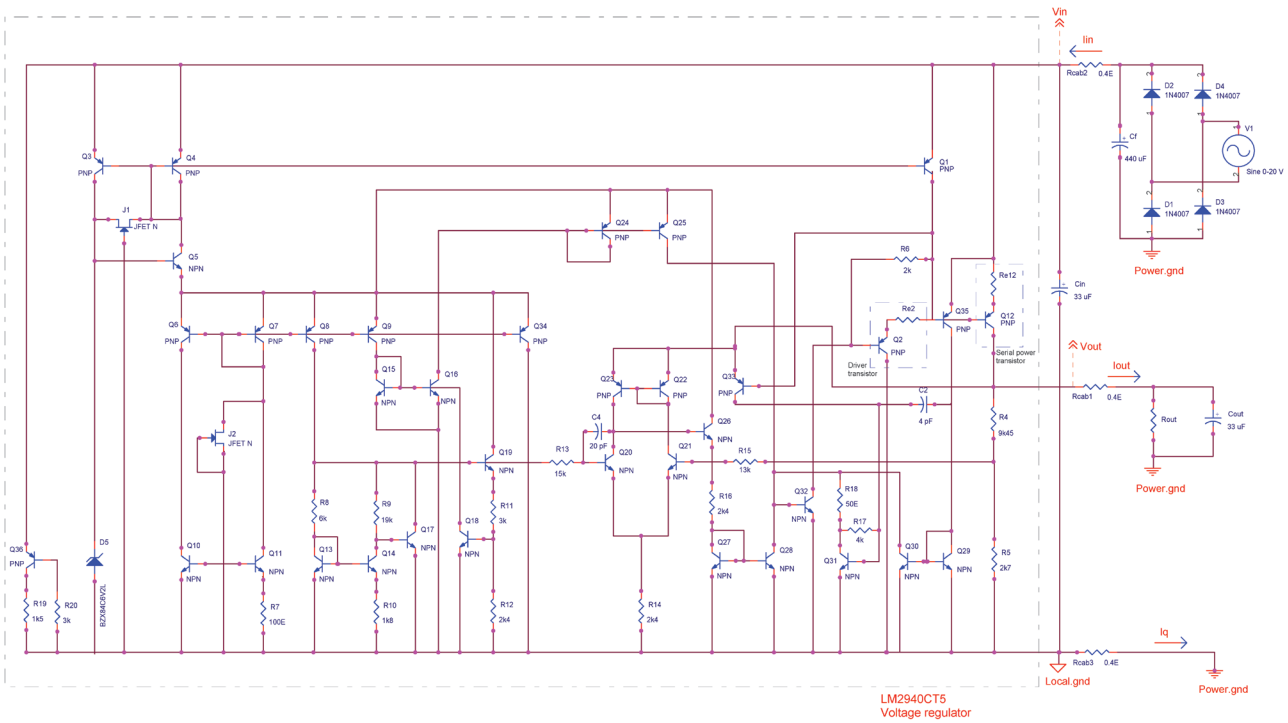

Figure 1: Detailed schematic circuit diagram of the simulation model, which was generated for examination of radiation and post-irradiation effects in the LM2940CT5 voltage regulator

for successful simulation and its harmonisation with the procured experimental results.

In order to obtain a faithful model of the implemented LM2940CT5 circuit PNP power transistor, additional resistors, R_{E12} and R_{E2} (see figures 1 and 2), were added to the serial and driver PNP power transistor emitters. The emitter resistance value of the power transistor in its *LTspice* model was kept at a constant value, while only external emitter resistance was changed, a feature that simulated radiation and post-irradiation effects in the emitter area of power transistors. *SPICE* parameters of the power transistors, the serial, Q_{12} and the driver one, Q_2 (see Fig. 1), are presented in Table 2. Most of the parameters from the original D45H11 model were not changed, but parameters related to the base resistance (Rb and Rbm) were increased twofold in order to obtain a faithful simulation of the Q_{12} power transistor response. Meaning of parameters, specified in Table 2, is given in the SPICE manual [33].

At first, a possibility was considered for significant influence of the operational amplifier output stage, supplying the driver transistor, as previously described in the literature [28]. Thus, possible influence of the output stage transistor (Q32 in Fig. 1) was evaluated on the perceived reduction of the maximum output current in LM2940CT5 voltage regulator. As in the case of all the other NPN transistors in the voltage regulator control circuit, transistor Q32 was selected as a basic model, having forward emitter current gain β_{F32} = 100. Influence of γ-radiation on the output stage transistor, Q32, was simulated by reduction of its current gain. None-

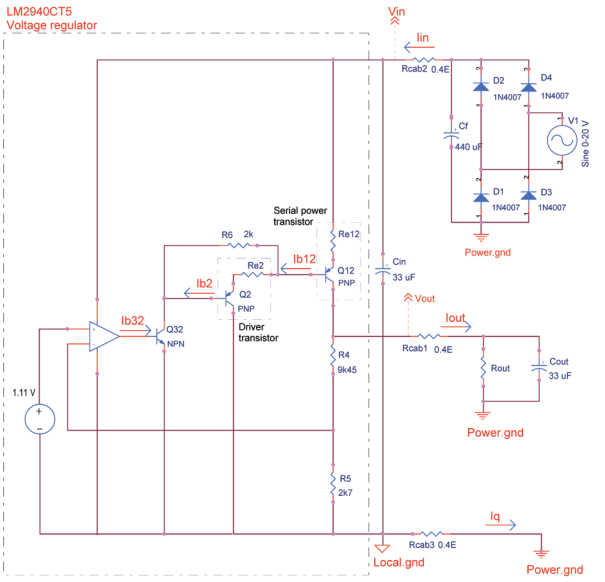

Figure 2: Simplified schematic circuit diagram of the simulation model presented in Fig. 1. The most important elements and nodes used for the analysis of the LM2940CT5 voltage regulator, presented in Table 1, are emphasized in the plot

theless, procured results led to the conclusion that the parameters of the transistor Q32 had negligible effect on the serial transistor's base current and the voltage regulator maximum output current. Even a fivefold reduction of its current gain (down to β_{F32} = 20) led to only 0.5 % reduction of the serial transistor base current, whilst keeping the voltage regulator maximum output current almost unchanged.

Therefore, according to the previous analysis, as well as the published data [12-16], it was assumed that the elements of the control circuit would have constant values, while the values of two power transistors (serial and driver PNP transistors) were changed for every control point. Comparison of the experimental and simulation data for the base current of the serial PNP power transistor, I_{B12}, are presented in figures 3 - 6. Used parameters of the serial and driver transistors, for every predetermined irradiation and annealing point, are presented in Table 1. Successive periods of annealing are marked in the same way as in the capture of Table 1.

Thus, the data presented in Table 1 and figures 3 - 6 indicate the relatively small influence of radiation and post-irradiation effects on the serial power transistor knee current, a much greater effect on its forward emitter current gain and, finally, a substantial influence on emitter resistance. This last parameter crucially affected the radiation hardness of the serial power transistor and, consequently, the radiation response of the LM2940CT5 voltage regulator.

In general, for increased total ionising dose, the current gain of power transistor declined, knee current increased and, usually, emitter resistance increased.

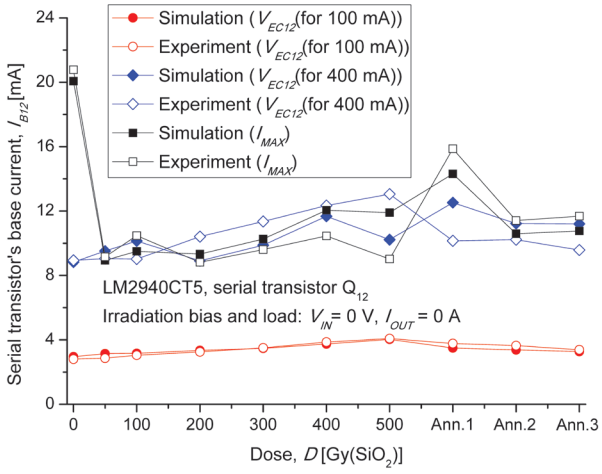

Figure 3: Variations of the serial transistor's base current as a function of the total ionising dose and type of annealing: comparison between simulation and experimental results. Bias conditions during irradiation: V_{IN} = 0 V, I_{OUT} = 0 A.

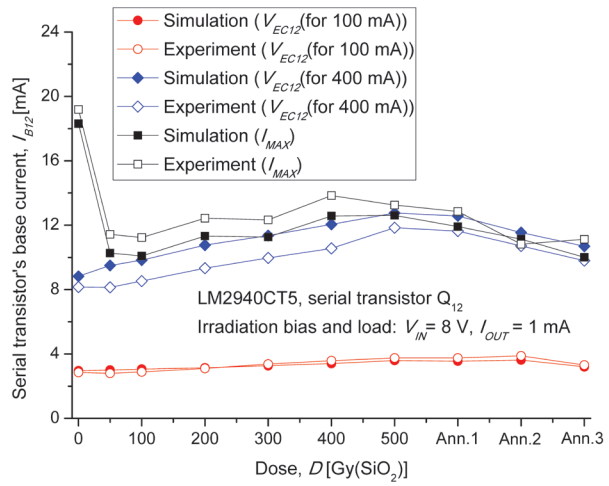

Figure 4: Variations of the serial transistor's base current as a function of the total ionising dose and type of annealing: comparison between simulation and experimental results. Bias conditions during irradiation: V_{IN} = 8 V, I_{OUT} = 1 mA.

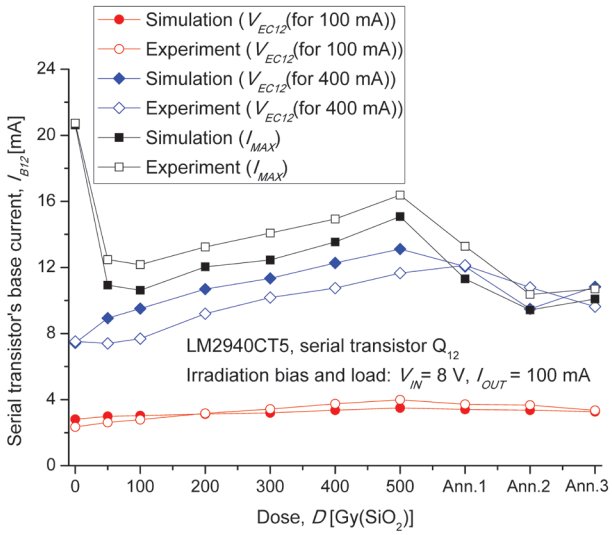

Figure 5: Variations of the serial transistor's base current as a function of the total ionising dose and type of annealing: comparison between simulation and experimental results. Bias conditions during irradiation: V_{IN} = 8 V, I_{OUT} = 100 mA.

When knee current was too low, for simulation of the maximum output current, base current of the serial transistor was too large. If a current gain would be too high, a base current (for minimum dropout voltage with output current of 100 mA) would be too low, in comparison with experimental values. If emitter resistance would not match exactly with the filter capacitor, the input (≈ 8 V DC) and output voltage (≈ 4.7 V DC), obtained experimentally, could not match the simulation results when the maximum output current was ex-

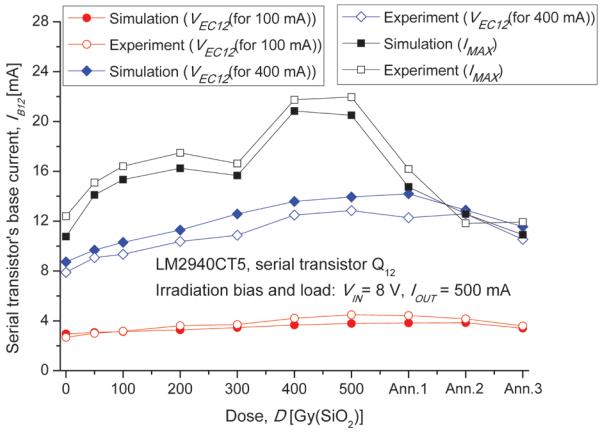

Figure 6: Variations of the serial transistor's base current as a function of the total ionising dose and type of annealing: comparison between simulation and experimental results. Bias conditions during irradiation: V_{IN} = 8 V, I_{OUT} = 500 mA.

amined. Therefore, using a procedure of trial and errors, acceptably good combination of the serial power transistor parameters β_{F12}, I_{KF12} and R_{E12} have been achieved.

Criterium for the acceptable deviation of simulation results from the experimental ones was mainly defined as a compromise between overshoot of the simulated base current, obtained during examination of the minimum dropout voltage (for I_{OUT} = 400 mA), and undershoot of the same simulated value, procured whilst maximum output current was determined. Thus, the parameters of the serial lateral PNP transistor were changed until a balance was achieved between deviation of base currents (I_{B12}), procured during an experiment and simulation. An effort was made to keep the deviation between experimental and simulation results of base currents up to 10 – 15 %. Only in several extreme points (see, for instance, Fig. 3: D = 500 Gy (SiO$_2$)) this range was exceeded, when the deviation reached, at most, 30 %.

At last, when simulations of all the experiments were finished, for all the total doses and annealing sequences, new simulations had been made. These characteristics, presented in Fig. 7, were produced for serial transistor collector currents, which ranged from 1 - 400 mA, and for a constant emitter-collector voltage of 3.3 V. Since the maximum output current for samples of unbiased voltage regulators in many cases declined below 400 mA, simulation results for 300 mA were also included.

5.2 Radiation effects

Bias conditions implemented during irradiation primarily affected variations of the serial transistor's emitter resistance, R_{E12}. On the other hand, bias condition influences were less apparent on variations of the forward emitter current gain and knee current, since these measures were primarily affected by the absorbed total ionising radiation dose. Deposition of the total 500 Gy dose in all cases decreased forward emitter current gain by 54 - 62 %. The knee current was more sensitive to the bias conditions, since it increased by 20 - 80 %. Nevertheless, emitter resistance variations exhibited a wide range of behaviour; they sharply increased when the circuit did not operate with high load current during the irradiation and steadily decreased when integrated circuits were biased and heavily loaded during gamma-radiation exposure. $\beta_F(I_{C12})$ characteristics were generated for I_{C12} collector currents between 1 – 400 mA (Fig. 7). Simulation results revealed that, simultaneously, collector current of Q_2 driver transistor changed only from 1.6 mA up to 12 mA. For the specified range of collector currents of the serial power transistor, and taking into account all the control points, the computer simulation provided emitter-base voltage values (V_{EB12}) between 355 and 691 mV.

The marked differences between the emitter resistance variations, recorded for various bias conditions, demonstrate different dominant mechanisms of the charge buildup in oxides and interfaces of irradiated integrated circuits. Based on the data presented in Table 1 and figures 3 - 6, one can conclude that the serial power PNP transistor emitter area was, for the first three cases, primarily affected by the initial buildup of the oxide trapped charge following the absorption of 50 Gy radiation. This initial absorbed dose significantly decreased the maximum output current and, consequently, the entire voltage regulator radiation tolerance. Nevertheless, this phenomenon did not occur for the samples that were heavily loaded during irradiation. In these circuits, emitter resistance steadily decreased as the absorbed dose increased, and declined nearly ninefold after 500 Gy radiation absorption. At the same time, the serial transistor forward emitter current gain decreased by 60 %. Data on the maximum output current and minimum dropout voltage (for total ionising dose of 500 Gy) revealed that the overall performance of heavily loaded voltage regulators slightly improved (see Table 1). This result suggests that the voltage regulator radiation tolerance was more affected by the positive influence of the serial transistor emitter resistance decline than by the negative influence of the serial transistor current gain reduction.

It is important to define the reason for the maximum current improvement of the samples heavily loaded during irradiation. As previously mentioned, high load current may significantly increase chip temperature and thus lead to oxide-trapped charge annealing. Nev-

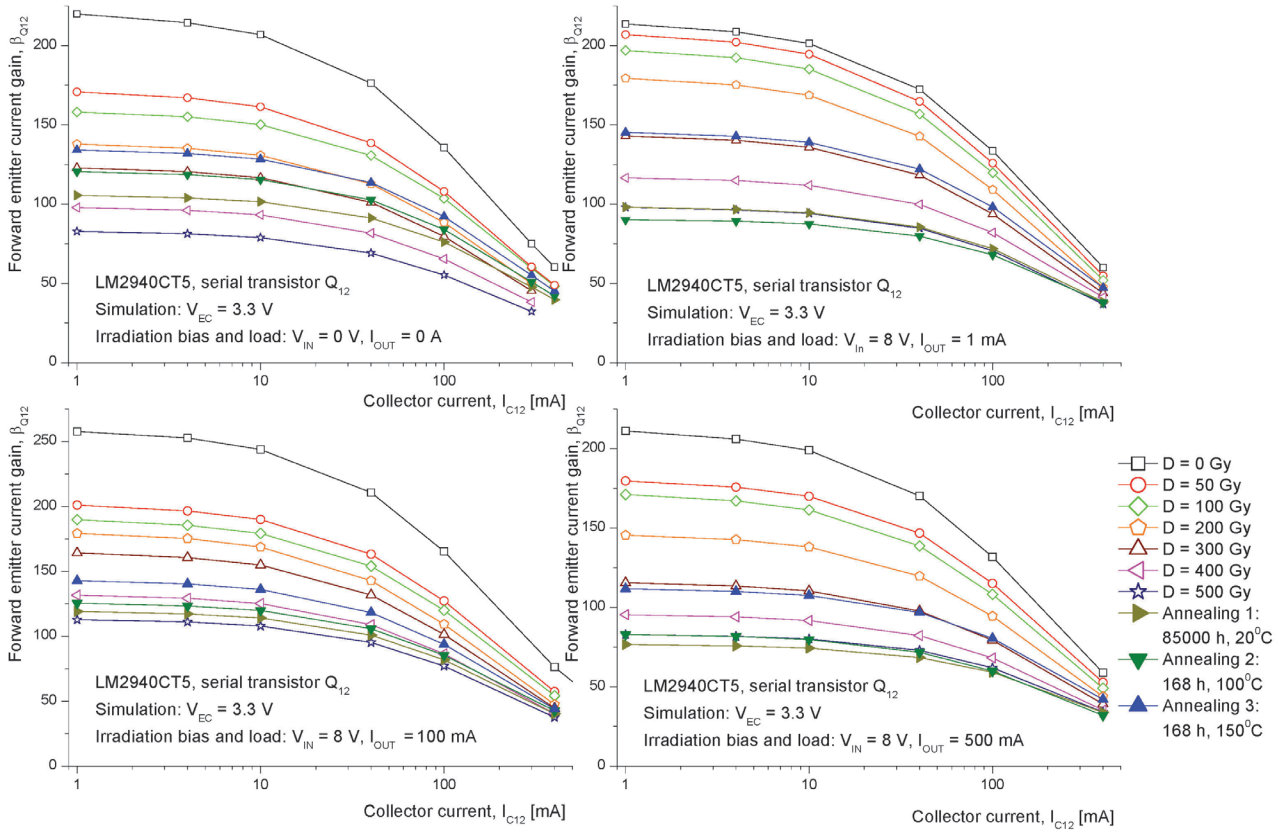

Figure 7: Variations of the current gain of the serial power transistor Q_{12} in the LM2940CT5 voltage regulator, presented as a function of the collector current in: a) unbiased circuits (V_{IN} = 0 V, V_{OUT} = 0 A); b) biased and negligibly loaded (V_{IN} = 8 V, V_{OUT} = 1 mA); c) biased and moderately loaded (V_{IN} = 8 V, V_{OUT} = 100 mA); d) biased and heavily loaded circuits during irradiation (V_{IN} = 8 V, V_{OUT} = 500 mA). Diagrams were created for a constant emitter-collector voltage, V_{EC} = 3.3 V. Data were obtained from computer simulation models of the irradiated and annealed voltage regulators, which demonstrated high agreement with the experimental results presented in Table 1 and figures 3 - 6.

ertheless, this factor is connected with the total power dissipation and, consequently, to the emitter-collector dropout voltage. Since the input voltage was 8 V during irradiation, the dropout voltage was nearly 3 V. Taking into account an output current of 0.5 A, power dissipation was 1.5 W. The total thermal resistivity of the LM2940CT5 voltage regulator is approximately 18 K/W (thermal resistivities of the implemented heatsink and junction-case structure of the TO-220 package were, respectively, 14 K/W [14] and 4 K/W [23]), as well as an ambient temperature of 20°C, there could be a theoretical chip temperature rise of up to 47°C. Nevertheless, this value is low for any expressed annealing of the oxide-trapped charge, since the oxide-trapped charge significantly anneals only when temperatures exceed 75–100°C [34], and interface traps at even higher temperatures, up to 250°C [7].

In previous research, a detailed discussion was dedicated to analysis of the influence of the trapped charge type on the LM2940CT5 voltage regulator radiation response [16]. Taking into account that, above the base and emitter areas of the lateral power PNP transistor was highly contaminated isolation oxide, with an approximate thickness d_{ox} = 500 nm [12], it was assumed that the oxide trapped charge would primarily affect this integrated circuit radiation response, while the interface trap concentrations would have secondary importance [16]. The primary reason for this supposition was the expectation that the concentration of the charge trapped in the oxide would be very high, with a proportion of $N_{ot} \sim d_{ox}^{\ 2}$ [34, 35] or even $N_{ot} \sim d_{ox}^{\ 3}$ [34]. Nevertheless, a more recent publication revealed that in thick oxides, at room temperature and at low electric fields, charge yield would be relatively low, since most of the oxide bulk would not influence the total concentration of the oxide trapped charge [36]. Accordingly, in most real applications, in thick isolation oxides of bipolar integrated circuits, the concentration of the oxide trapped charge would not be proportional to the square of the oxide thickness, but rather much weaker dependence than $N_{ot} \sim d_{ox}^{\ 2}$, primarily observed in thin

gate oxides of metal-oxide-semiconductor (MOS) devices [35]. Thus, in most practical cases, the influence of the interface trap concentrations (N_{it}) would be of primary importance to bipolar integrated circuit radiation response.

Therefore, it may be assumed that high current flow in the LM2940CT5 voltage regulator primarily passivated switching states, i.e., traps at the interface silicon–oxide and at the accompanying border oxide region, which lead to voltage regulator recovery from gamma-radiation influence. This proposition is much more plausible than the influence of high current on the oxide-trapped charge itself, either due to chip temperature increase or the high-current-density effect on the oxide below the wide emitter's metal contacts [16]. Large emitter resistivity variations in virgin, unirradiated devices indicate a defect build-up even in the fabrication phase of integrated circuits that would consequently decrease the voltage regulator's maximum output current (as have been seen in [12]).

The developed *LTspice* simulation model and obtained electrical characteristics $\beta(I_{C12})$, as well as the previously presented line regulation characteristics [16], mutually show the primary cause of the LM2940CT5 voltage regulator low radiation tolerance was primarily related with high emitter resistance of the serial PNP power transistor Q_{12}.

5.3 Post-irradiation effects

As mentioned earlier, three annealing sequences were selected to analyse the dominant influence of various kinds of trapped charge on the radiation response of the LM2940CT5 voltage regulator. It would be expected that long-term, room temperature annealing should allow partial recovery of the oxide-trapped charge with further build-up of interface traps [25, 37]. Then, one-week 100°C annealing should allow recovery of most of the remaining oxide-trapped charge without seriously affecting the interface traps [17, 23]. Finally, 168-hour, 150°C annealing should remove most residual interface traps while simultaneously eliminating all remaining oxide trapped charge [17, 22]. Thus, such an approach enables a rough estimation of the influence of bias and load conditions on charge trapping in the LM2940CT5 voltage regulator.

Data from Table 1 and Fig. 7 indicate great variation in the post-irradiation response of the various voltage regulator samples. Current-gain characteristics of the serial power transistor, $\beta(I_{C12})$, are good foundations for analysis of these circuit responses. The first conclusion is that post-irradiation effects related to the serial transistor's forward emitter current gain and knee current, on the one hand, and the emitter resistance, on the other, showed no correlation; both demonstrated variations in separate ways. Heavily loaded voltage regulators demonstrated slight degradation of the serial transistor current gain during the ten-year room-temperature annealing, while moderately loaded circuits showed slight recovery. However, in both mentioned cases emitter resistance increased (sevenfold for the heavily loaded circuits). At the same time, negligibly loaded circuits (I_{OUT} = 1 mA) seemingly remained unaffected by the room-temperature annealing sequence, both from the perspective of current gain and emitter resistance. Finally, unbiased samples demonstrated great recovery of the serial transistor's current gain, followed by significant reduction in emitter resistance. Thus, a conclusion may be drawn that during radiation exposure the unloaded circuits were heavily affected by the oxide-trapped charge. Biased and negligibly loaded samples were seemingly unaffected by the oxide trapped charge, and, consequently, ten-year build-up of the interface traps. Room-temperature annealing apparently caused more substantial degradation to the voltage regulator operated with higher load current during radiation exposure. In this case, it may be assumed that the interface states buildup resulted in the marked emitter resistance increase.

The next step was one-week, 100°C annealing. Except in the case of unloaded voltage regulators, this test marginally affected the serial transistor's forward emitter current gain, while, for all biased samples, emitter resistance increased (most prominently in the heavily loaded devices). This test was intended primarily to remove the oxide-trapped charge. Thus, the obtained results (Table 1 and Fig. 7) supported the previous conclusion that, in all the voltage regulators, biased during irradiation, serial transistors were, in comparison with the influence of interface traps, marginally affected by the influence of the oxide trapped charge.

Finally, the third annealing procedure was 168-hour, 150°C exposure of irradiated samples in a thermal chamber. Such an annealing procedure, designed for the removal of most interface traps, led to the recovery of the serial transistor current gain in all of the examined circuits. The most prominent was the forward emitter current gain recovery in biased, negligibly loaded voltage regulators. Further, emitter resistance declined or remained the same in all cases. Nevertheless, all the examined circuits were far from complete recovery from the ionising radiation influence, since the serial transistor current gain remained approximately 60 % of its pre-irradiation value. Yet, there was a very interesting result regarding the serial transistor emitter resistance, R_{E12}. Despite great initial variations obtained by simulations from the experimental results (see Table 1), at the end

of the third annealing sequence, emitter resistances for all serial transistors, regardless of the bias conditions of irradiated voltage regulators, were nearly the same! The maximum values of the output voltage, obtained during the examination of the minimum dropout voltage (with a constant output current of 400 mA) were also nearly the same (V_{OUT} = 4.724 – 4.765 V; Table 1). Thus, at the end of the high-temperature annealing process, it may be assumed that only interface traps remained in the LM2940CT5 voltage regulator, and they heavily affected the serial transistor emitter resistance and forward emitter current gain.

6 Conclusion

The COTS LM2940CT5 voltage regulator was examined in a gamma-radiation environment, where it was exposed to up to 500 Gy radiation, followed by analysis of its performance in various annealing procedures. In order to analyse these radiation and post-irradiation effects, a detailed *LTspice* simulation model of this integrated circuit was developed.

Implementation of the simulation model clearly identified the serial power transistor, comprised of 350 elementary lateral PNP transistors, as the weakest part of the entire integrated circuit. Radiation effects in small signal transistors, as well as in the driver PNP power transistor, did not significantly affect the LM2940CT5 voltage regulator's radiation tolerance. On the other hand, primarily the increase of the serial transistor emitter resistance, followed by the decrease of its forward emitter current gain, disqualifies this circuit for use in a radiation environment.

This integrated circuit demonstrated great influence from bias and load conditions on its radiation tolerance. With the exception of samples that operated with a high load current during irradiation, all the other circuits demonstrated a significantly increased serial PNP power transistor emitter resistance even after initial irradiation (50 Gy total dose). On the other hand, operation with high load current during irradiation led to a multifold reduction in emitter resistance concomitant with an increase in the voltage regulator's maximum output current, regardless of the simultaneous significant reduction of the forward emitter current gain. As expected, serial transistors of unbiased and unloaded voltage regulators exhibited the greatest degradation in the ionising radiation environment; both forward emitter current gain and emitter resistance were affected.

In most of the examined cases, three annealing sequences further degraded emitter resistance. There was significant recovery of forward emitter current gain observed in all the irradiated LM2940CT5 voltage regulators. Serial transistors of unbiased and unloaded circuits demonstrated the most prominent recovery during the 10-year room-temperature annealing. One-week, 100°C annealing led to significant recovery only of the unbiased circuits. Finally, one week, 150°C annealing sequence led to significant recovery of the forward emitter current gain of serial lateral PNP power transistors in all the examined integrated circuits. This final annealing procedure unified emitter resistance in all of the analysed circuits, regardless of their initial values or bias conditions during operation in a gamma-radiation environment.

7 Acknowledgement

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