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Simulation on the Interfacial Singular Stress-strain Induced Cracking of Microelectronic Chip Under Power On-off Cycles

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Abstract: Thermal fatigue failure of a microelectronic chip usually initiates from the interface between the solder joint and substrate due to the mismatch in coefficients of thermal expansion (CTE). Because of the viscoelastic creep properties of the solders, the stress and strain at the solder/substrate interfaces are strongly dependent on temperature and time. Based on the established creep constitutive models of the solder materials, a three-dimensional thermomechanical analysis of the microelectronic chip undergoing power on-off cycles is conducted based on the finite element method (FEM). The singular interfacial stress-strain fields are obtained and the singular field parameters are quantitatively evaluated. Furthermore, the crack nucleation in power on-off fatigue test of the microelectronic chip is observed, to verify the conclusion that the singular stress-strain induces thermal fatigue failure from the solder/substrate interface.

Keywords: Thermal fatigue; microelectronic chip; creep; singular field; crack nucleation

Simulacija razpok mikroelektronskega čipa zaradi posameznih mejnih stresov pri ciklih vklapljanja napajanja

Izvleček: Različni termični koeficienti materialov so večinoma vzrok za odpvedi zaradi termične utrujenosti in pri čipu izhajano iz stične površine med lotom in substratom. Zaradi viskoelastičnosti lota je stress na mejni površini močno odvisen od časa in temperature. Uporabljena je tridimenzionalna termo-mehanična analiza vplivov ciklanja vklapljanja napajalne napetosti z uprabo metode končnih elementov. Kvantitativno so ocenjeni posamezni parametri in opažen je bil pojav nastajanja razpok zaradi stresa na stiku lot/substrat.

Ključne besede: termična utrujenost; mikoelektronski čip; polzenje; nastanek razpok

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1 Introduction

The flip flat package technology is currently widely used in electronic engineering to meet the demands of high-speed functions and system miniaturization [1]. The high density and cost-effective requirements of the package structure have led to the emergence of small size and multiple input/output (IO) points in chip design. Solder joints, as the mechanical, electrical and heat-dissipating components, require excellent reliabilities during soldering and service [2-3]. In the soldering process, the formation of intermetallic compounds (IMCs) is a necessary condition for the formation of solder joints, and the reliability of solder joints is highly dependent on the formation and growth of IMC at the interface [4]. With the growth of intermetallic compounds, stress concentration easily appears at the interface of solder joint due to the mismatch of coefficients of thermal expansion of the materials, which causes the cracking and reduces the service life of solder joints [5-6]. Due to the increase of packaging density, both the size and shape of solder joints appear in various combinations, a quantitative evaluation method of the strength and life for solder joints is strongly expected.

Under thermal cyclic loading, failure or fatigue crack generally initiates from the interface edge or near to the interface between the solder joint and substrate, and its mechanism is strongly affected by the stress singularity at the interface edge or stress concentration induced by the interface [7-9]. Therefore, it is of practical importance to determine the stress state at the interface, so that the susceptibility to thermomechanical failure can be predicted for new geometry-to-material combinations. The traditional strength-based methods are not suitable since the stresses are singular even at the idealized interface edges or corners [10-12]. To overcome this concern, Hattori et al. [13] have suggested a singularity parameter approach for the interface reliability of plastic IC packages using two stress intensity parameters that characterize the stress distribution near a bonded edge along with the interface. Other authors [14-16] argued that the two parameters: singular order λ and stress intensity factor *K*, can be used in a criterion for crack initiation or delamination for certain structure configurations. Generally, FEM is a valuable tool for determining the constants λ and *K*. At the same time, finite element modeling enables the design to be evaluated before it is physically produced thus minimizing time and cost. The results obtained from the FEM modeling will be useful in suggesting design changes in terms of package geometry and choice of packaging materials.

The purpose of this study is to develop an objective method to analyze the thermal cyclic behavior and to evaluate the failure of solder joints in a microelectronic chip. According to the creep results of solder materials, the nonlinear creep constitutive models are established. The three-dimensional thermomechanical analysis of the microelectronic chip under power on-off cycles is conducted, and the time-dependent stress and strain at the solder/substrate interfaces are obtained. Finally, the details that the singular stress-strain promotes the thermal fatigue failures from these interfaces are discussed when compared with the results from fatigue tests.

2 Package description

The structure of the microelectronic chipset is presented in Fig. 1. It has nineteen pieces of chips, including two pieces of chip Q1, one piece of chip Q2, six pieces of chip Q3, four pieces of chip Q4 and six pieces of chip Q5, respectively. Their working powers are 35.7, 33.3, 25.8, 20.0 and 14.5 w, respectively. The schematic cross-sections of chip Q1-5 in layered structure are similar, i.e., substrate, insulate layer, Cu, SnAg3Cu0.5, Cu, Pb-5Sn, wafer and silica gel from bottom to top, as shown in Fig. 2. The main dimensions of chips Q1-5 are listed in Table1.

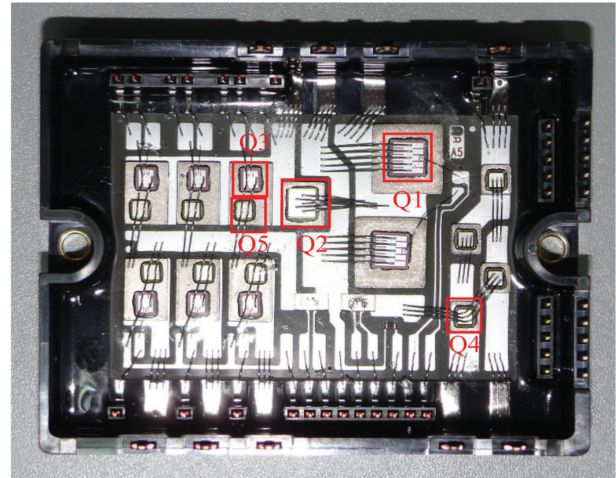

Figure 1: Structure of the microelectronic chipset

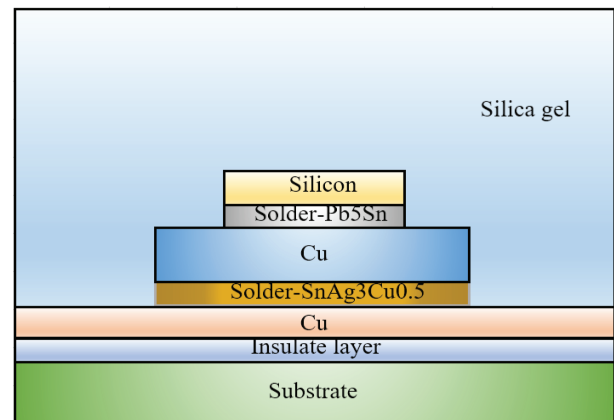

Figure 2: Schematic cross-section of the single chip

Table 1: Dimension of five different types of chips (unit: mm)

Chip type	Wafer $A_0 \times B_0 \times C_0$	Solder Pb-5Sn $A_1 \times B_1 \times C_1$	Solder $SnAg_3Cu_{0.5}$ $A_2 \times B_2 \times C_2$
Q1	6.6×6.6×0.38	6.6×6.6×0.08	13×13×0.12
Q2	5.4×5.4×0.46	5.4×5.4×0.08	8×8×0.12
Q3	3.6×4.2×0.38	3.6×4.2×0.08	8×11.5×0.12
Q4	3.3×3.3×0.25	3.3×3.3×0.08	5.5×5.5×0.12
Q5	3.2×3.2×0.46	3.2×3.2×0.08	8×11.5×0.15

3 Numerical simulation process

3.1 Constitutive model of solder materials

According to the theory of viscoelasticity, the typical strain rate-stress relationship of the solder is linear at

low stress, and power law creep at middle and high stresses. On the basis of the previous literature [17-18], a hyperbolic sine power constitutive model is adopted, in which the relationship of strain rate with stress is linear at low stress and is hyperbolic sine power at middle and high stresses, as shown in Eq. (1). At each temperature *T*, there exists a critical stress σ_v (*T*), which is used to separate the linear and power law creep stages. According to the creep results of two solder materials Sn3Ag0.5Cu and Pb5Sn, the strain rates under various stress levels and temperature-dependent σ_v are determined, as shown in Table 2 [19].

Sn3Ag0.5Cu: $$\dot{\varepsilon}=\begin{cases}A(\sinh B\sigma)^n\exp(-H/RT) & \text{if } \sigma>\sigma_V\\ A_0\exp(A_1/T)\sigma\exp(-H/RT) & \text{if } \sigma\le\sigma_V\end{cases}$$

Pb5Sn: $$\dot{\varepsilon}=\begin{cases}A(\sinh B\sigma)^n\exp(-H/RT) & \text{if } \sigma>\sigma_V\\ (A_0-A_2(T-T_R))\sigma\exp(-H/RT) & \text{if } \sigma\le\sigma_V\end{cases} \quad (1)$$

$$\sigma_V=C_0-C_1(T-T_R)+C_2(T-T_R)^2 \quad (2)$$

where σ is the equivalent stress, σ_v is the linear viscous creep limit, *H* is the activation energy, *R* is the universal gas constant, *T* is the absolute temperature value, and T_R is 273 Kelvin (K).

3.2 FEM analysis and results

The FEM model of the whole chipset is shown in Fig. 3, and the related material constants are shown in Table 3.

Before the power-driven transient thermal analysis, the coefficients of heat transfer are determined by comparison of the temperatures obtained from numerical analysis and measured results in tests. The chipset maintains power on at the first 30 s, then power off. The measured temperature at the center of the bottom surface increases linearly from 21.2 °C to 70 °C within the first 19 s, keeps at 70 °C till 25 s, and decreases linearly from 70 °C to 35.2 °C within 25-44 s, finally maintains at 35.2 °C in the remained times. By adjusting the coefficients of heat transfer in the FEM model until the temperature at the center of the bottom and upper surfaces agree with the measured ones, the actual values of coefficients of heat transfer at the bottom and upper surfaces are finally determined.

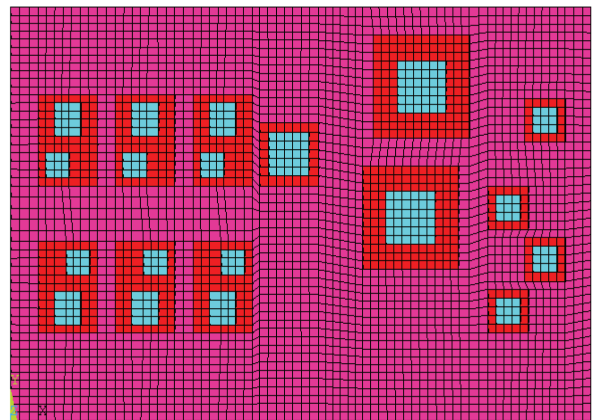

Figure 3: FEM model of the chipset

Table 2: Material parameters and coefficients in Equations (1)-(2)

Eq. (1)	*A* (s^{-1})	*B* (MPa^{-1})	*n*	*H/R* (K)	A_0 (MPa-1.s^{-1})	A_1 (MPa)	A_2 (MPa)
Sn3Ag0.5Cu	2.08×106	0.145	5.85	12993	2.039×10-4	8484	__
Pb5Sn	3.16	0.18	4.2	6535	8.168	__	0.0524
Eq. (2)	C_0 (MPa)			C_1 (MPa.K^{-1})		C_2 (MPa.K^{-2})	
Sn3Ag0.5Cu	17.357			0.1219		2.457×10^{-4}	
Pb5Sn	8.0667			0.0017		1.1364×10^{-4}	

Table 3: Material constants in the analysis

Material	Elastic modulus GPa	Poisson's ratio	Coefficient of thermal expansion 10^{-6}/K	Coefficient of heat transfer W/(m.K)	Density kg/m^3	Specific Heat J/(kg.m)
Silicon	187.0	0.25	5.05	150.0	2330	678.262
Pb5Sn	16.1	0.44	29.4	35.2	11160	129.791
Cu	110.0	0.35	16.5	398.0	8960	385.186
SnAg3Cu0.5	41.6	0.36	21.7	64.2	7400	234.461
Cu	110.0	0.35	16.5	398.0	8960	385.186
Insulate layer	5.4	0.34	67.0	4.0	3100	962.964
Al	73.0	0.33	23.6	237.0	2700	900.162
Substrate	0.1	0.36	50.0	0.17	980	1507.25

In the actual power-driven transient thermal analysis, the chipset is repeatedly powered on and off, and both the dwell times are 3 minutes. The transient thermal conduction analysis of the whole chipset is carried out at first, then followed by thermal stress submodel analysis of each chip according to the temperature fields obtained from the thermal conduction analysis of the whole chipset, to get the stress and strain distributions at the solder/substrate interfaces. The boundary conditions in the submodel of each chip are obtained by automatic interpolation of the ANSYS software, as shown in Fig. 4.

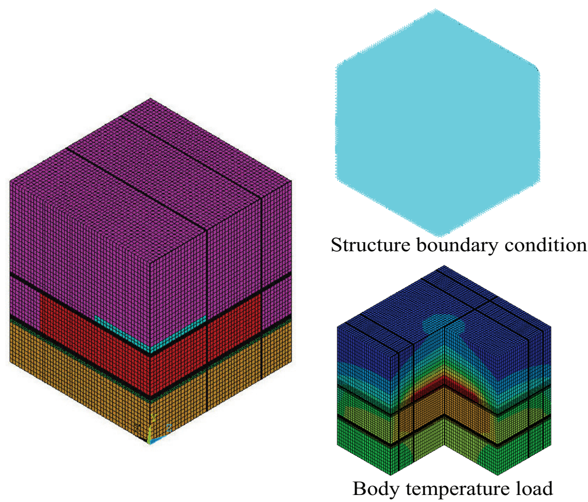

Figure 4: The detailed mesh and boundary conditions of chip Q1

Fig. 5 shows the temperature and strain rate at the center of material 2 (solder Pb5Sn) and 4 (solder Sn3Ag0.5Cu). Due to the shock of power on, high temperature gradient and stress appear in solder Pb5Sn since it is just beneath the power layer. The high stress is presently relaxed because the strain rate reaches a balanced state. After the temperature gets to a saturated state, the strain rate decreases. Because the heat flux is difficult to pass through the thermal insulate layer (material 6) beneath it, the temperature gradient and stress in Sn3Ag0.5Cu solder are very small at the beginning of power on. Therefore, the strain rate at the initial state is very small and gradually increases with the rise of temperature. At the edges around the interface, the heat flux comes from the directions that are not blocked by the thermal insulate layer, as a result, the thermal shock appears. The instant thermal stress and strain distribution in the symmetry plane of chip Q1 at 30 s are shown in Fig. 6, it can be seen obvious stress and strain concentration at the interfacial edge between wafer and Pb5Sn (denoted by E12 in follows), and SnAg3Cu0.5 and Cu (denoted by E45 in follows).

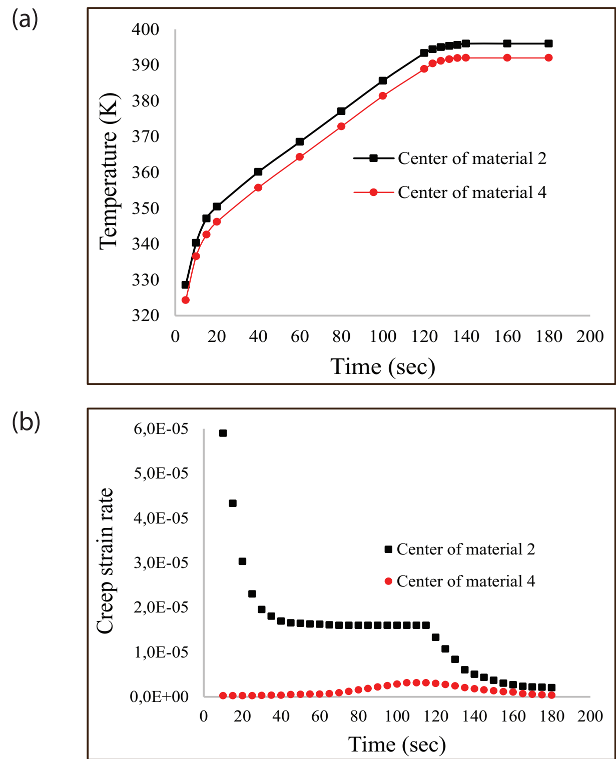

Figure 5: Variations of temperatures and creep strain rates of the solders: (a) temperature, (b) creep strain rate (material 2: Pb5Sn, material 4: Sn3Ag0.5Cu)

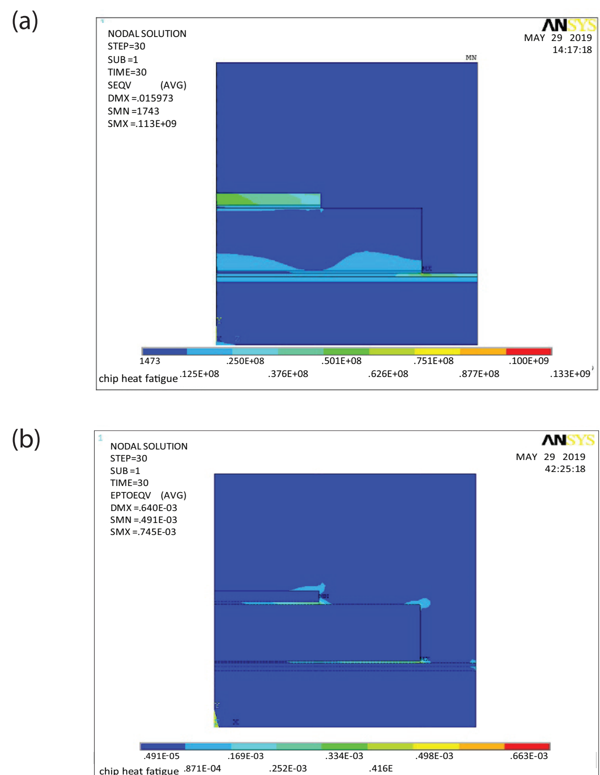

Figure 6: Equivalent stress and strain distribution in the symmetry plane at 30 s: a) stress; b) strain

Fig. 7 shows the equivalent stress distribution in materials 1, 2 and 3 near the interfacial edges. The stress concentration is found at the interfacial edge between materials 1 and 2. Fig. 8 depicts the equivalent strain distribution in materials 3, 4 and 5, and we can also see a severe strain concentration appearing at the interfacial edge between materials 4 and 5. Here the failures of solder joints are mainly concerned, it can be understood from the stress and strain distributions that the failures may occur at the interfacial edges of either E12 or E45. Therefore, the singular stress and strain near these interfacial edges need to be investigated carefully. For this purpose, two data points A and B at E12 and E45 are selected, respectively, as shown in Fig. 9.

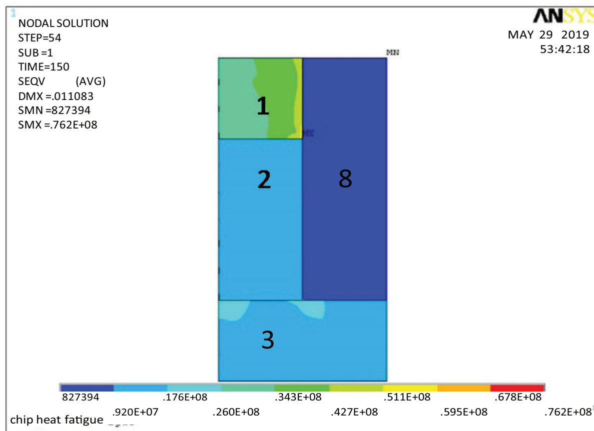

Figure 7: Equivalent stress at 30 s

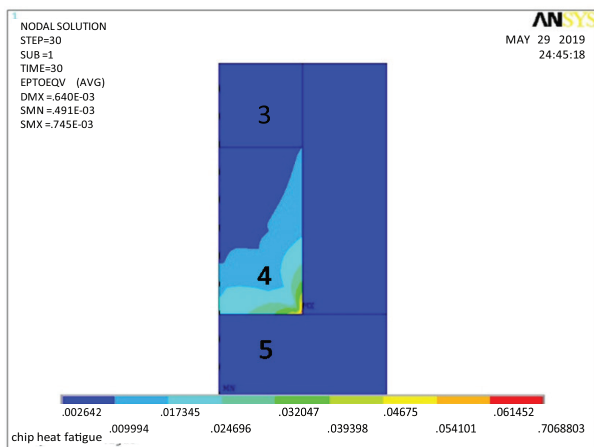

Figure 8: Equivalent creep strain at 30 s

Figs.10 and 11 show the cyclic stress variations of points A and B with power on-off cycles. The severest stress case appears just after power on and finally tends to be steady. Since the normal stress at interface E12 is always compressive, we use the maximum shear stress to define the maximum stress state. Similarly, the maximum traction stress $\sigma_t=(\sigma^2+\tau^2)^{1/2}$ is adopted to define the maximum stress state because the normal stress at E45 is tensile. Fig.12 presents the cyclic strain variations of points A and B with power on-off cycles, and the maximum strain state appears just at the moment of power off. The maximum creep strain increase with cycle since the creep strain can accumulate.

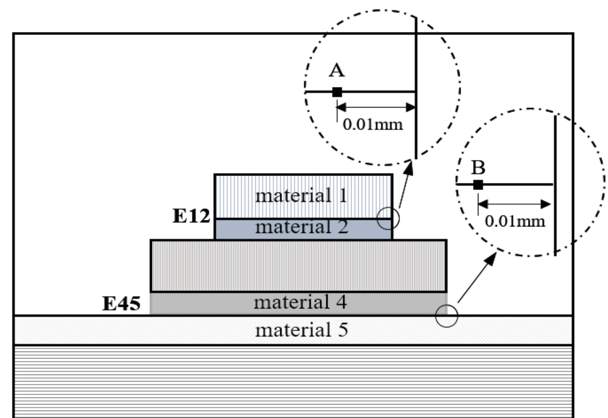

Figure 9: Selected data points A and B

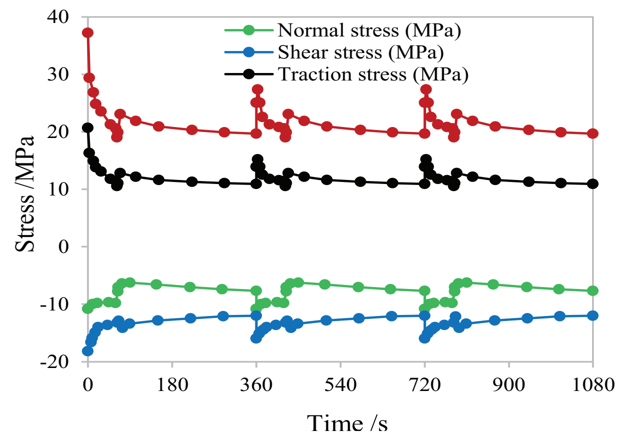

Figure 10: Stress distribution vs time at point A

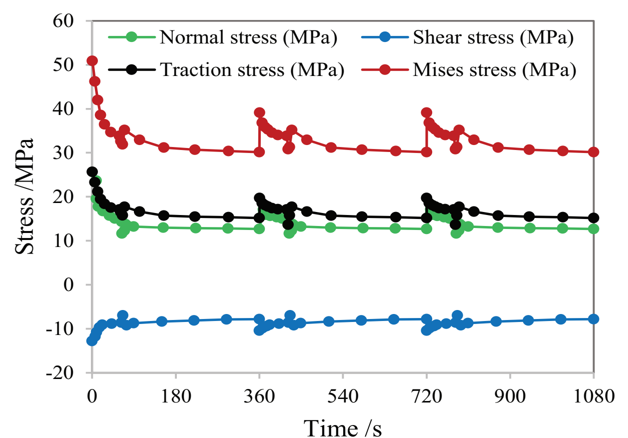

Figure 11: Stress distribution vs time at point B

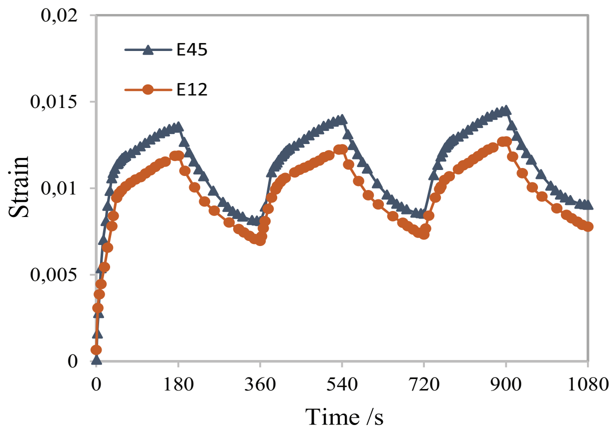

Figure 12: Strain distribution at points A and B

4 Stress-strain singularity and thermal fatigue failure

4.1 Singularity analysis

High stress-strain singularity weakens the connection strength and promotes the crack nucleation from the solder/substrate interface. Therefore, the interfacial singular characteristics, as the key factor affecting the fatigue life, should be discussed in detail. According to the singular field theory, the instant singular stress and strain fields can be expressed as [20]

$$\sigma_i = \frac{K_i(t)}{r^{\delta_i(t)}}, \quad \varepsilon = \frac{K_\varepsilon(t)}{r^{\zeta(t)}} \tag{3}$$

where $K_i(t)$ and $K_\varepsilon(t)$ denote stress and strain intensity factors, $\delta_i(t)$ and $\zeta(t)$ are the stress and strain singular orders, r denotes the distance from the interfacial corner, and i=1, 2 denotes the normal and shear stress, respectively.

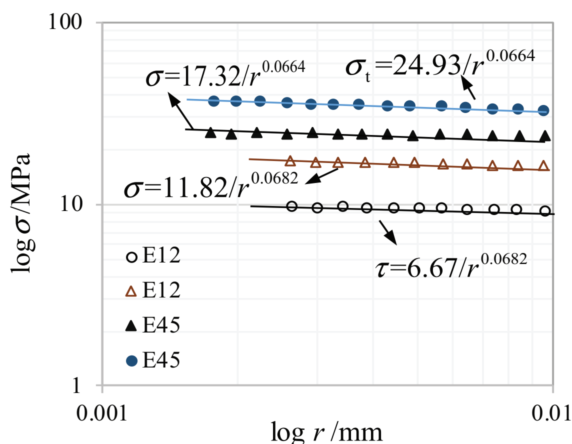

Figure 13: Logarithmic stress distribution

Fig. 13 shows the logarithmic stress distributions along with the distance from the corner at the interfaces E12 and E45. According to the fitting results, the stress intensity factors and singular orders of E12 and E45 are different. Fig. 14 shows the strain distributions at the interfaces E12 and E45, we can see that the singularity of strain is far stronger than that of stress. This fact indicates the strain field may be the dominant factor of failure. The singular orders of stress and strain are different due to the nonlinear constitutive relationships adopted in this analysis.

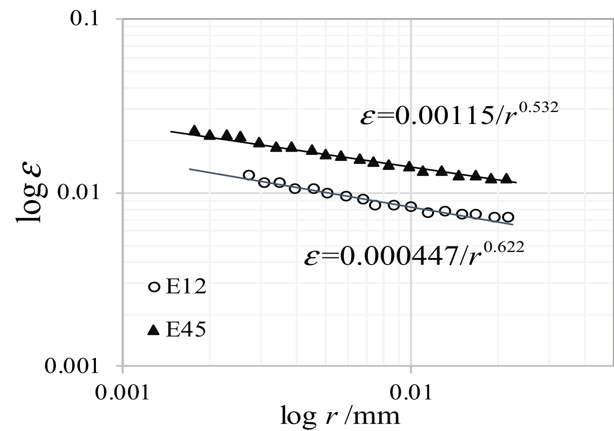

Figure 14: Logarithm strain distribution

The stress and strain singularities of the five types of chips are analyzed by the above method. The stress intensity factors and singular orders at the maximum stress state are shown in Table 4, where K_t is the intensity factor of tensile traction, i.e., $\sigma_t = K_t/r^\delta$. The strain intensity factors and singular orders at the maximum strain state are listed in Table 5. It is noted that the normal stress at E12 is always compressive, so the stress intensity factor $K_{\sigma'}$ in this case, has no physical meaning. Since the traction stress combined by the tensile normal stress and shear stress at E45 is the dominant factor for the failure from the interface, it is not necessary to give K_τ separately in this case. Regarding the state before power on as the zero stress-strain states, the stress and strain intensity factors listed in Tables 4 and 5 represent the variation ranges dominating the fatigue failure.

Table 4: Analysis results of the maximum stress field (* CS denotes normal compressive)

Chip Type		Maximum stress state			
		δ	K_t	K_σ	K_τ
			(MPa mm$^\delta$)		
Q1	E12	0.068	11.8	CS	-6.76
	E45	0.067	17.3	24.9	--

Q2	E12	0.112	9.11	CS	-5.21
	E45	0.078	13.3	19.6	--
Q3	E12	0.098	9.93	CS	-5.64
	E45	0.087	12.9	19.2	--
Q4	E12	0.048	13.8	CS	-7.54
	E45	0.098	13.4	18.9	--
Q5	E12	0.120	6.53	CS	-3.64
	E45	0.112	9.94	14.8	--

Table 5: Analysis results of the maximum strain field

Chip Type		Maximum strain state	
		ζ	K_ζ (mm$^\zeta$)
Q1	E12	0.622	0.000447
	E45	0.532	0.001150
Q2	E12	0.789	0.000151
	E45	0.687	0.000238
Q3	E12	0.762	0.000138
	E45	0.705	0.000176
Q4	E12	0.745	0.000157
	E45	0.678	0.000163
Q5	E12	0.658	0.000221
	E45	0.784	0.000067

4.2 Power on-off fatigue failure test

Based on the three-dimensional thermomechanical analysis, the interfaces E12 and E45 both undergo a cyclic creep strain during power on-off cycles. To observe the fatigue failure of the microelectronic chip, the cyclic power on-off tests of the chipset are carried out to observe the failure situation. The dwell times of power on-off at the fatigue tests are set as same as that in the FEM analysis. It is found the fatigue failure of the microelectronic chip causes the increase in electronic resistance, so the in-situ resistance measurement is adopted to determine the fatigue failure when the resistance increase exceeds a specific threshold value that followed by 10 % resistance increase [21]. The cutting sections and crack morphologies of the chips are observed by the JSM-6301F scanning electron microscope (SEM) (JEOL, Tokyo, Japan). The samples are covered by carbon before and the analysis is conducted under 20 KeV in the SEI mode. The selected images of chip Q1 and Q5 are shown in Fig. 15. It can be found that there exists a main crack both at the interface E45 (SnAg3Cu0.5/Cu) of chip Q1 and Q5. Many micro cracks are also seen around the main crack, while no crack is observed at E12 (Pb5Sn/wafer). The results from FEM analysis are in good agreement with the test results. Considering the crack nucleation of the failed chips and the results obtained from finite element analysis, it can be drawn that the fatigue failure of the microelectronic chip is attributed to the interaction of singular stress and strain at the interface E45.

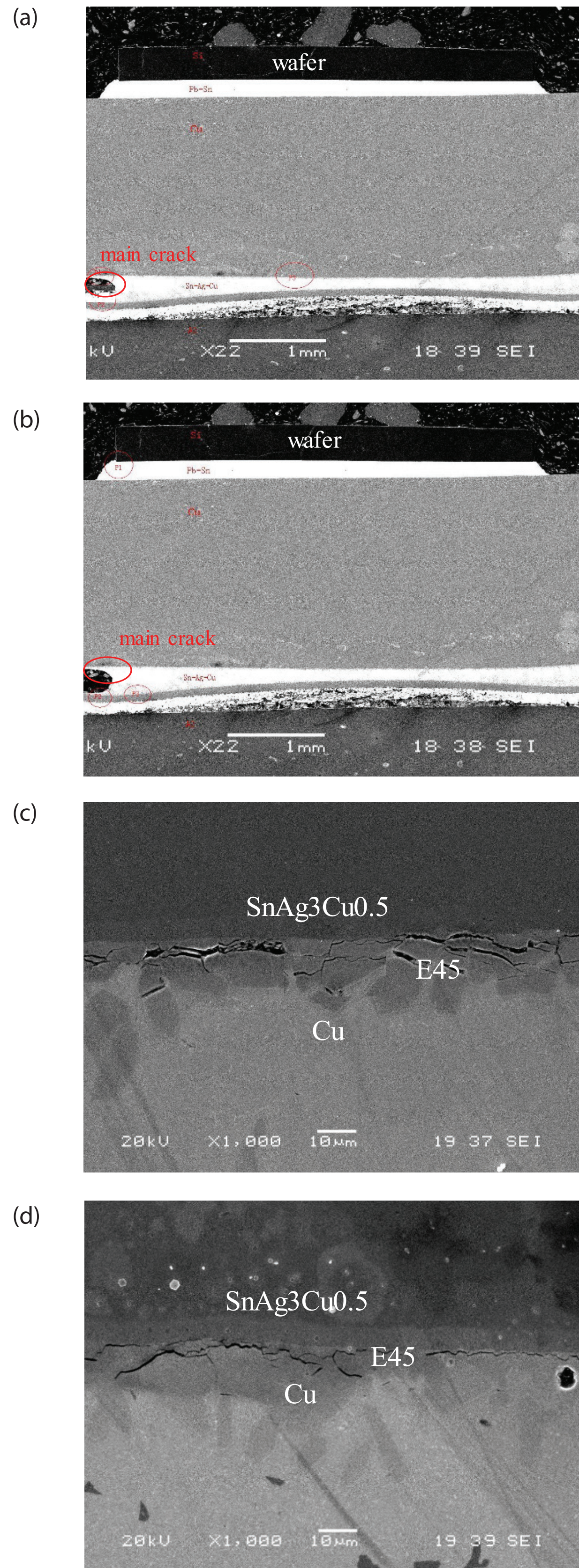

Figure 15: Crack morphology of selected fatigued chip: (a)(c) chip Q1, (b)(d) chip Q5

5 Conclusions

In this paper, we have demonstrated a three-dimensional finite element model that can provide a unique insight into the localized stress and strain concentrations at the solder/substrate interfaces in a microelectronic chip that undergoes power on-off cycles. Based on the calculated stress-strain distributions and singularity parameters, the conclusions are summarized as follows:

The variations of interfacial stress-strain fields are time dependent. The maximum stress appears just after the moment of power on and finally tends to be steady. The creep strain continues to increase after power on and reaches the peak value until power off. The singular order of strain is larger than that of stress, owing to the adopted nonlinear stress-strain relationships of the solders. The stress and strain intensity factors and singular orders at E45 are higher than that at E12, indicating that E45 undergoes a more severe stress-strain fluctuation. From the SEM observation of the fatigued chip, the fatigue crack indeed initiates firstly from E45. The test results are in good agreement with that from the FEM analysis, and the fatigue failure of the microelectronic chip is mutually controlled by the singular stress and strain at the SnAg3Cu0.5/Cu interface.

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