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A New FGMOS FDCCII and Filter Applications

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Abstract: In this work, a new floating gate MOS (FGMOS) fully differential difference current conveyor (FDCCII) is presented. Employing FGMOS transistors two important advantages are introduced compared to conventional CMOS structure; firstly the input stage of the circuit providing the arithmetic calculations gets simpler, secondly the linearity range increases due to the properties of FGMOS differential amplifier. Furthermore, the versatility of the proposed FGMOS FDCCII is demonstrated on a filter circuit example. Both the FGMOS FDCCII circuit and proposed filter circuit are simulated with SPICE simulation program by using 0.35μm technology parameters. Simulation results show that the proposed building block can be used for the design of filters with high linearly properties.

Keywords: FGMOS, FDCCII, Biquad Filter, Analog Integrated Circuits

Nove možnosti uporabe FGMOS FCCII in filtrov

Izvleček: V članku je predstavljen nov diferencialni MOS ojačevalnik s plavajočimi vrati (FGMOS). V primerjavi s klasično CMOS strukturo ima FGMOS dve prednosti: enostavnejša vhodna stopnja aritmetičnih izračunov in izboljšana linearnost zaradi lastnosti FGMOS ojačevalnika. Vsestranskost predlaganega FGMOS FDCCII vezja je predstavljena na primeru filtra. FGMOS FDCCII in vezje filtra sta simulirana v SPICE okolju v 0.35μm tehnologijo. Simulacije nakazujejo, da je predlagana struktura uporabna za načrtovanje filtrov z visoko linearnostjo.

Ključne besede: FGMOS, FDCCII, biquad filter, analogna integrirana vezja

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1 Introduction

Designing circuits suitable for differential signals leads to have more versatile applications. There are lots of filter topologies in electronics literature employing the extensions of second generation current conveyor like differential difference current conveyor (DDCC) [1-2], differential voltage current conveyor (DVCC) [3-4], inverting current conveyor (ICCII) [5], current controlled conveyor (CCCII) [6-7] and dual-X current conveyor (DXCCII) [8].

Current conveyors are one of the most useful building blocks in analog design. Many efficient applications can be designed with success using CCII as basic component. Anyway, second generation current conveyors, as they have been proposed, show some drawbacks. For example, only one of the input terminals presents a high impedance level. This can be a problem if differential signals have to be handled. To overcome this, a solution using more CCIIs has been proposed [9].

A different approach can be that to implement more complicated basic blocks, one of which will be presented in this paper.

Fully differential difference current conveyor (FDCCII) may be considered as the most versatile building block that can be designed starting from the basic CCII. In fact, its topology can be thought as the "natural differential evolution" of the CCII idea. FDCCII circuit block combines the advantages and versatility of DDCC and DXCCII together. It has arithmetic signal processing capability of DDCC and gives opportunity to design filters with electronically tunable characteristics by utilizing two X terminals that is similar to DXCCII.

FGMOS structures are also known as multi-input MOS and their multi input advantages make it simpler to realize an arithmetic signal processing circuit. The FGMOS drain current is proportional to the square of the weighted sum of the input signals. In the last few years,

FGMOS transistors have found many applications in electronic programming [10], Op-amp offset compensation [11], D/A and A/D converters [12], inverters and amplifiers [13], voltage attenuators [14], current mirrors [15] and low voltage analog circuits [15]. Recently, an increased number of publications on the use of the FGMOS in analog computational circuits have been reported voltage squarers and multipliers [16-19].

In this paper, a new FGMOS FDCCII is proposed to obtain flexibility in analog IC design. By using FGMOS transistors the input stage of the circuit providing the arithmetic calculations gets simpler, also the linearity range increases due to the properties of FGMOS differential amplifier. The proposed FGMOS FDCCII is used in a filter circuit to demonstrate the versatility of the FDCCII block. Both the FGMOS FDCCII circuit and proposed filter circuit are simulated with SPICE simulation program by using 0.35um technology parameters. Simulation results show that the proposed circuit building block can be used to design filters with linearly tunable characteristics.

Rest of the paper is organized as follows. In Section II, the basic structure of the FGMOS transistor is described. The principle of operation of the FGMOS FDCCII and simulation results of the proposed circuit are presented in Section III and Section IV, respectively. Proposed filter circuit, as an application example, is shown in section V followed by conclusion in section VI.

2 The FGMOS transistor

Floating gate (FG) MOSFETs are being utilized in a number of new and exciting analog applications [17-20]. These devices are available in standard CMOS technology because they are being widely used in digital circuits. Thus floating gate devices are now finding wider applications by analog researchers. As a result, the floating gate devices are not only used for memories but are also being used as circuit elements. FGMOS transistors are used as analog memory elements, as part of capacitive biased circuits, and as adaptive circuit elements [20].

An FGMOS can be fabricated by electrically isolating the gate of a standard MOS transistor, so that there are no resistive connections to its gate. A number of secondary gates or inputs are then deposited above the floating gate (FG) and electrically isolated from it. These inputs are only capacitively connected to the FG, since the FG is completely surrounded by highly resistive material. So, in terms of its DC operating point, the FG is a floating node [20]. The equivalent schematic for an n-input n-channel FGMOS transistor is given in Figure 1.

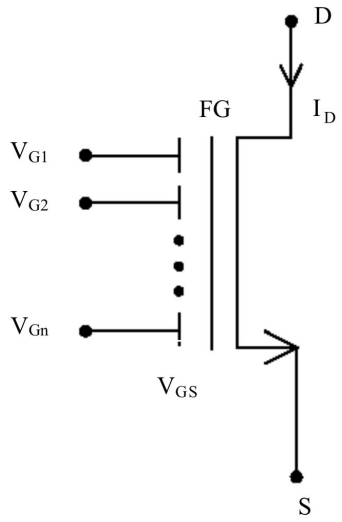


Figure 1: n-input n-channel FGMOS transistor

3 FGMOS FDCCII

Starting from the first and second generation current conveyors, many types of new topologies have been designed during the past years. FDCCII is one of the most versatile circuit blocks which presents flexibility in analog circuit design with its arithmetic signal processing capability and gives opportunity to electronically tunable characteristics in application examples.

3.1 FDCCII Circuit Building Block

FDCCII is characterized by four high-impedance input terminals (Y_1, Y_2, Y_3 and Y_4), two low-impedance node (X_1 and X_2) and four high-impedance output nodes (Z_1, Z_2, $Z_{1'}$ and $Z_{2'}$). Its block scheme and matrix characteristics are summarized below.

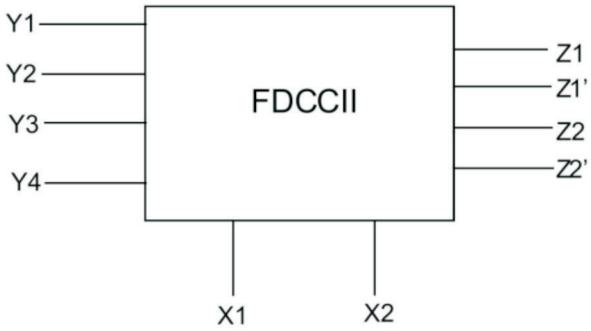


Figure 2: FDCCII block representation

$$\begin{bmatrix} V_{X1} \\ V_{X2} \\ I_{Y1,2,3,4} \\ I_{Z1,Z1'} \\ I_{Z2,Z2'} \end{bmatrix} = \begin{bmatrix} 1 & -1 & 1 & 0 & 0 & 0 \\ -1 & 1 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & \pm 1 & 0 \\ 0 & 0 & 0 & 0 & 0 & \pm 1 \end{bmatrix} \begin{bmatrix} V_{Y1} \\ V_{Y2} \\ V_{Y3} \\ V_{Y4} \\ I_{X1} \\ I_{X2} \end{bmatrix} \quad (1)$$

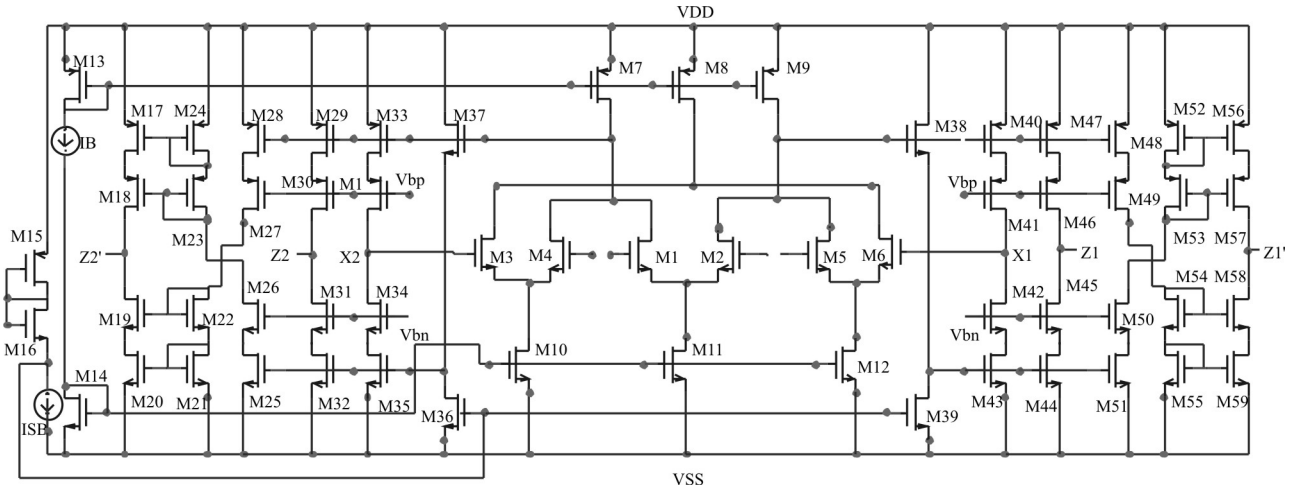
3.2 FGMOS FDCCII

Fig. 3a shows the CMOS FDCCII circuit while Fig. 3b shows the proposed floating gate fully differential difference current conveyor circuit employing FGMOS differential pairs instead of conventional MOS pairs to improve the circuit behavior. CMOS FDCCII circuit given in [21] employs three differential pairs in order to get the relationship of $V_{X1} = V_{Y1} - V_{Y2} + V_{Y3}$ and $V_{X2} = - V_{Y1} + V_{Y2} - V_{Y4}$. In FGMOS FDCCII circuit given in Fig. 3 only two FGMOS differential pairs are used to get both $V_{X1} = V_{Y1} - V_{Y2} + V_{Y3}$ and $V_{X2} = - V_{Y1} + V_{Y2} - V_{Y4}$. It is clearly seen that by using FGMOS transistors both the input stage of the circuit providing the arithmetic calculations gets simpler also the linearity range increases due to the properties of FGMOS differential amplifier [20]. In addition to these, new Y nodes can be added to FGMOS FDCCII circuit without any new transistors by only increasing the inputs of FGMOS transistors already used in differential pairs. This also reveals the flexibility of using FGMOS transistors in circuit blocks employing arithmetic calculations.

FGMOS transistors in differential pairs have three inputs which are applied through equal sized capacitors, Ci. The input signals of V_{Y1}, V_{Y2}, V_{Y3} and the control voltage V_C are applied to one of the floating gates in the differential pairs. Since the voltage at the gate is less than the input voltage the differential pair transistors can work in saturation even when large signals are applied. This leads to increase the input dynamic swing.

Determining parameters of voltage and current conveying properties are the slopes of related transistors and it is achieved easily by choosing matched transistors.

Impedance values of X, Y, Z nodes of the FGMOS FDCCII circuit can be seen as small at X node because of feedback and high at Z nodes because of the drain nodes of related transistors.



Figre 3a: CMOS FDCCII circuit

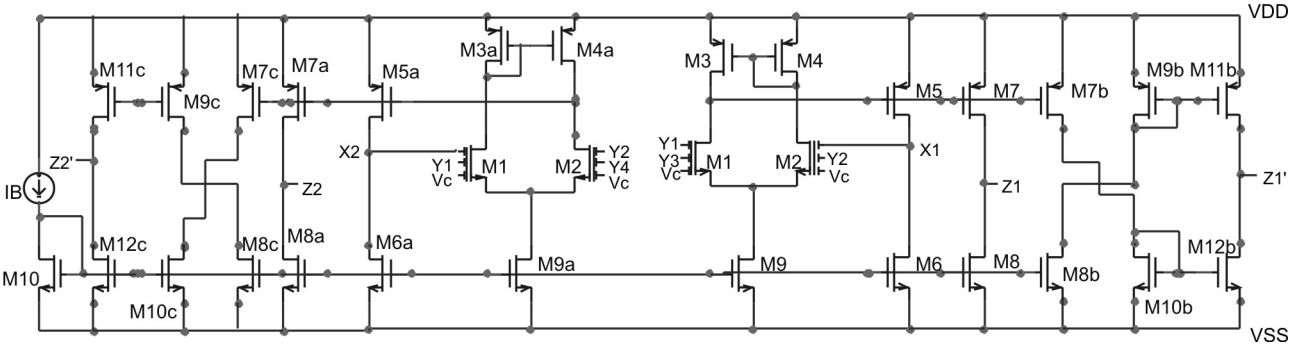


Figure 3b: FGMOS FDCCII circuit

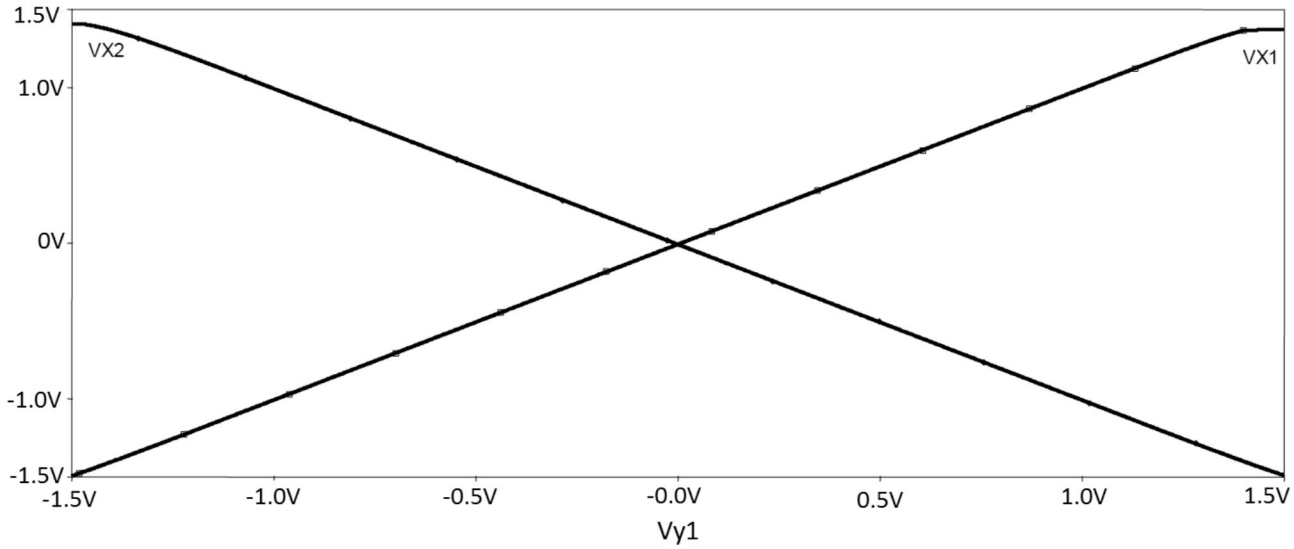


Figure 4: FGMOS FDCCII DC voltage transfer characteristics (V_{X1}-V_{Y1} and V_{X2}-V_{Y1})

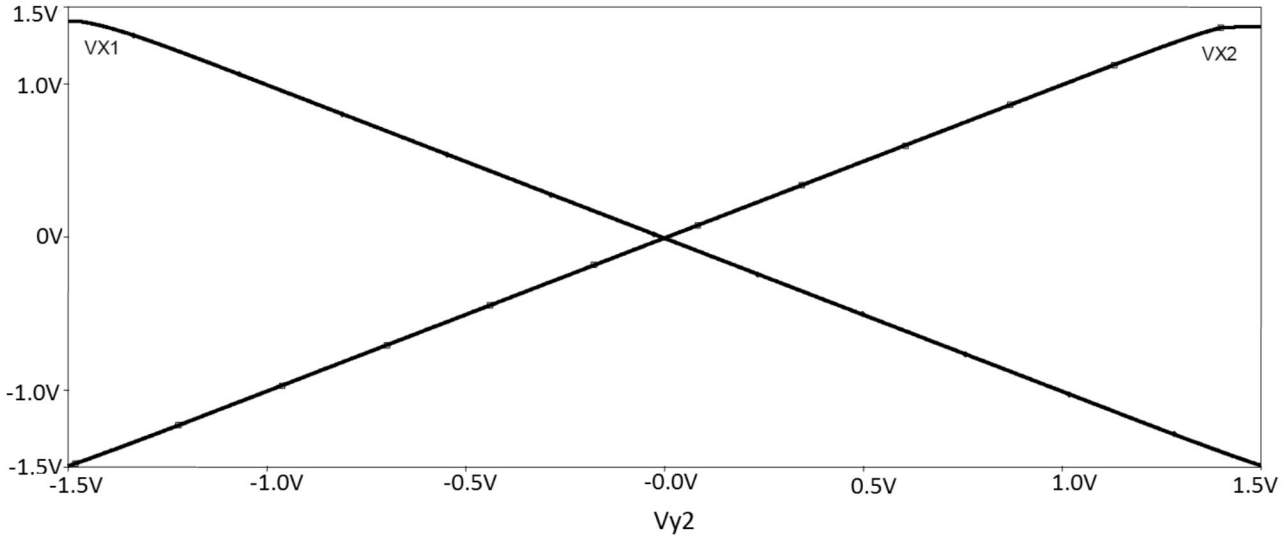


Figure 5: FGMOS FDCCII DC voltage transfer characteristics (V_{X1}-V_{Y2} and V_{X2}-V_{Y2})

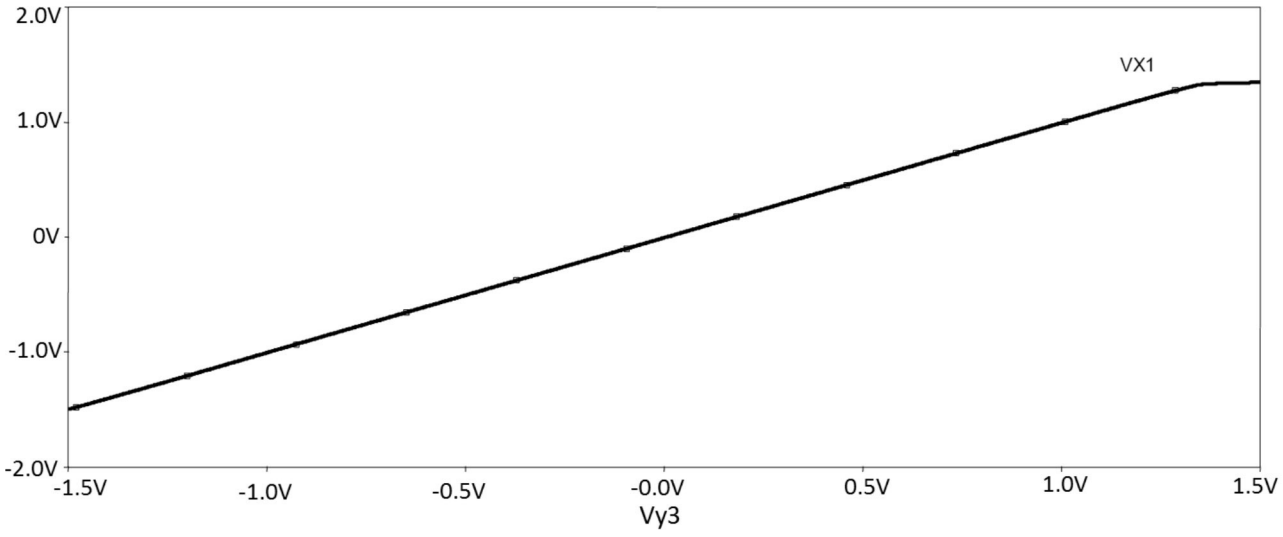


Figure 6: FGMOS FDCCII DC voltage transfer characteristics (V_{X1}-V_{Y3})

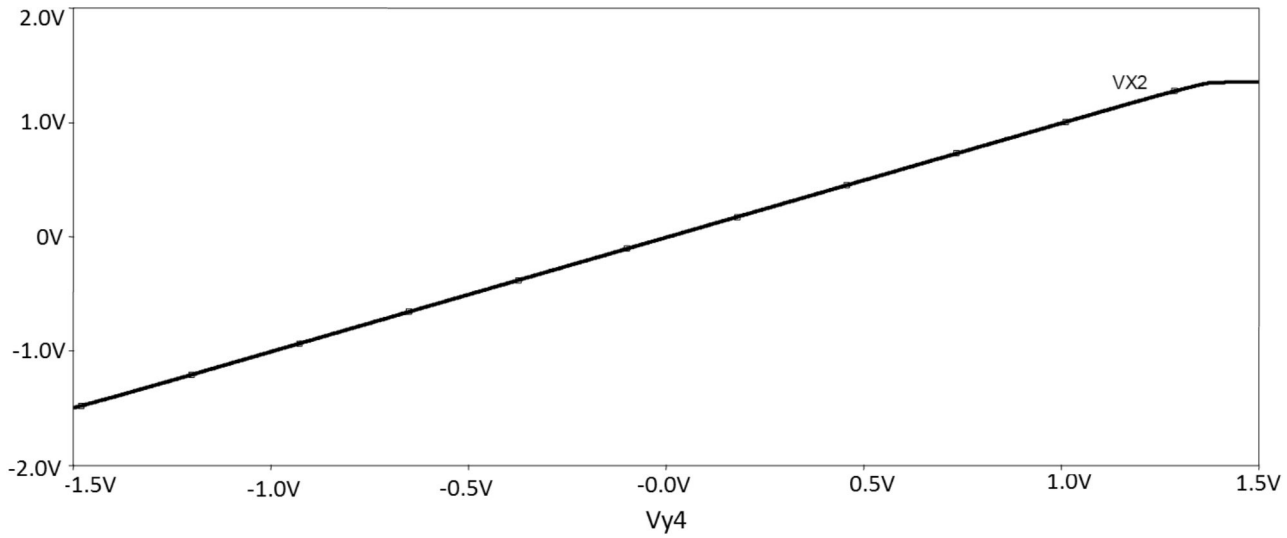


Figure 7: FGMOS FDCCII DC voltage transfer characteristics (V_{X2}-V_{Y4})

4 Simulation results

The proposed circuit of Fig. 3 is simulated with SPICE by using 0.35µm TSMC technology parameters. The supply voltages are ±1.5V, V_C is set to V_{DD} and bias current I_B = 10µA. The input capacitor values are taken C_i= 16,25fF while the C_{FGD} and C_{FGS} values are calculated as 0.2fF and 1.63fF, respectively. The dimension for n-type transistors is W / L = 0.7µm / 0.7µm and for p-type transistors is W / L = 1.4µm / 0.7µm.

Fig. 4, Fig. 5, Fig. 6 and Fig. 7 show the DC voltage transfer characteristics of the proposed circuit with respect to $V_{Y1, Y2, Y3, Y4}$ input DC voltages. DC voltage $V_{Y1, Y2, Y3, Y4}$ is swept between -1.5V and 1.5V while the DC voltage $V_{X1, X2}$ is plotted.

In Fig. 5, Fig. 6 and Fig. 7 while V_{Yi} is -1.5V, VX1 and VX2 take -1.49V and 1.4V, respectively. While V_{Yi} is 1.5V, V_{X1} and V_{X2} take 1.4V and -1.49V, respectively. As it is seen from these values, input swing is almost equal to the supply voltages.

Fig. 8 shows the DC voltage transfer characteristics of the proposed FGMOS circuit and the CMOS circuit [21] together. V_{X1} is plotted for both circuits. As it is seen from the figure, input swing is increased by using FGMOS transistors.

Fig. 9 and Fig. 10 show the DC current transfer characteristics of the proposed circuit with respect to I_B bias current. DC bias current I_B is swept between -10µA and 10µA while the DC output currents $I_{Z1,Z1',Z2,Z2'}$ are plotted.

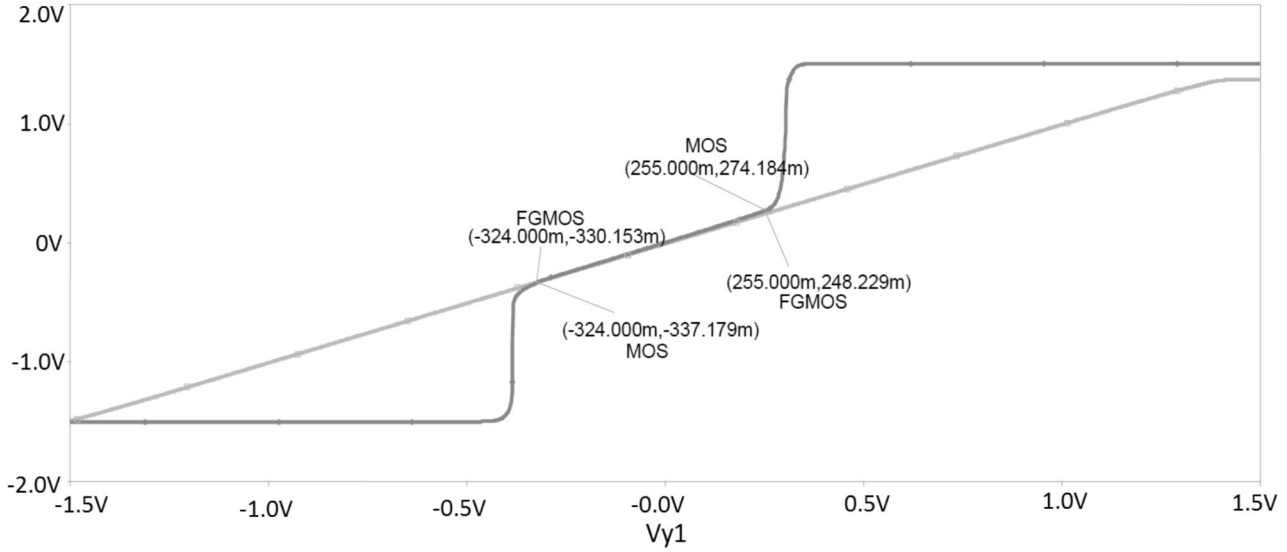


Figure 8: DC voltage transfer characteristics of the proposed FGMOS circuit and CMOS circuit

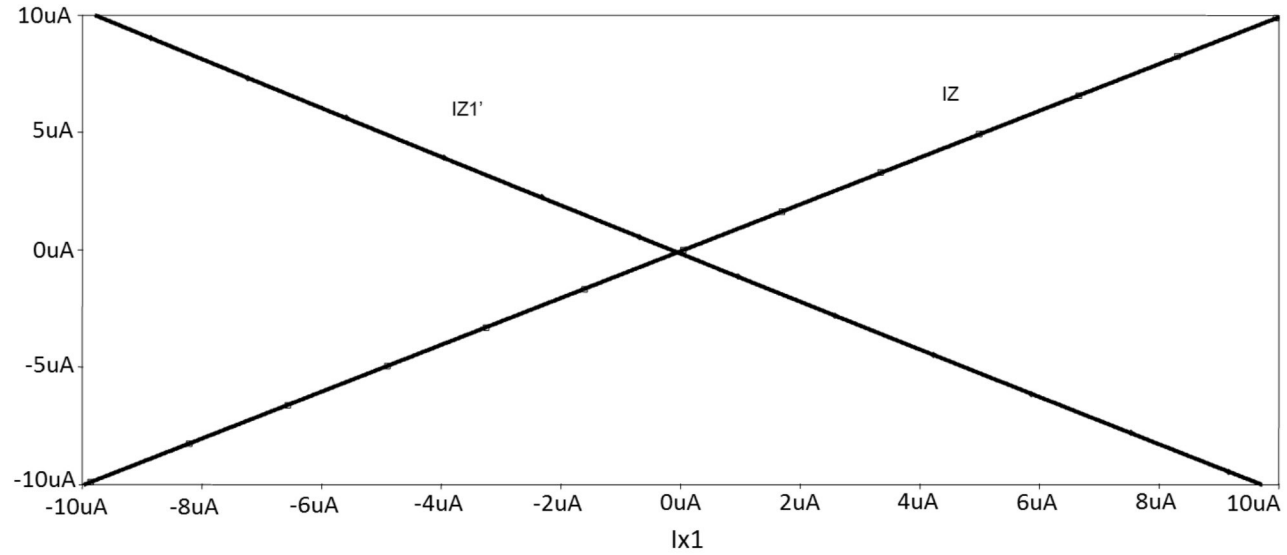


Figure 9: FGMOS FDCCII DC current transfer characteristics

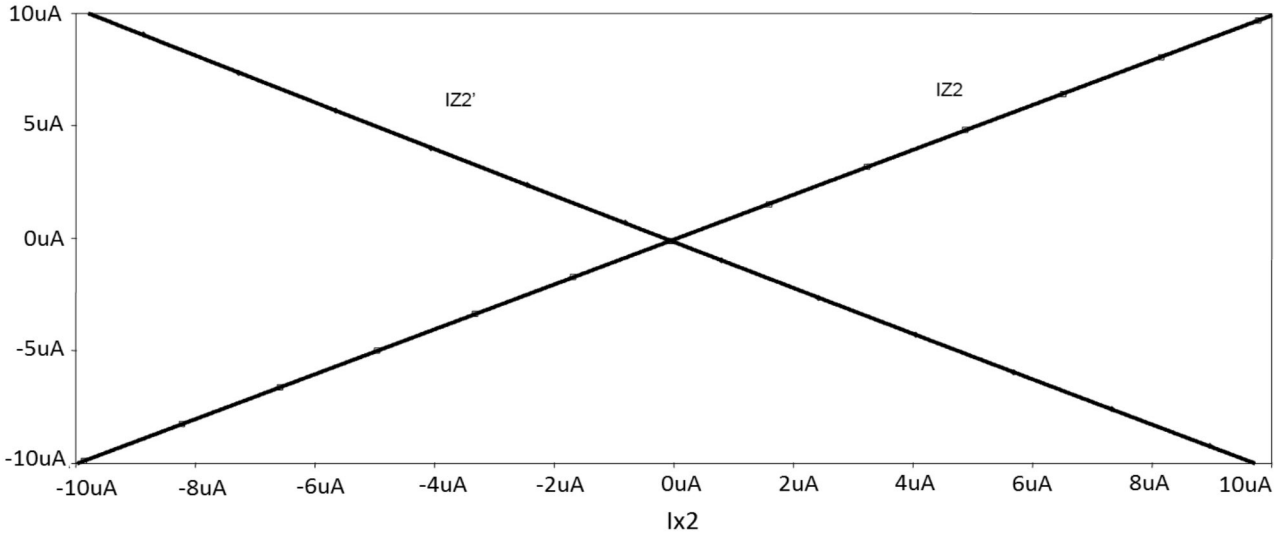


Figure 10: FGMOS FDCCII DC current transfer characteristic

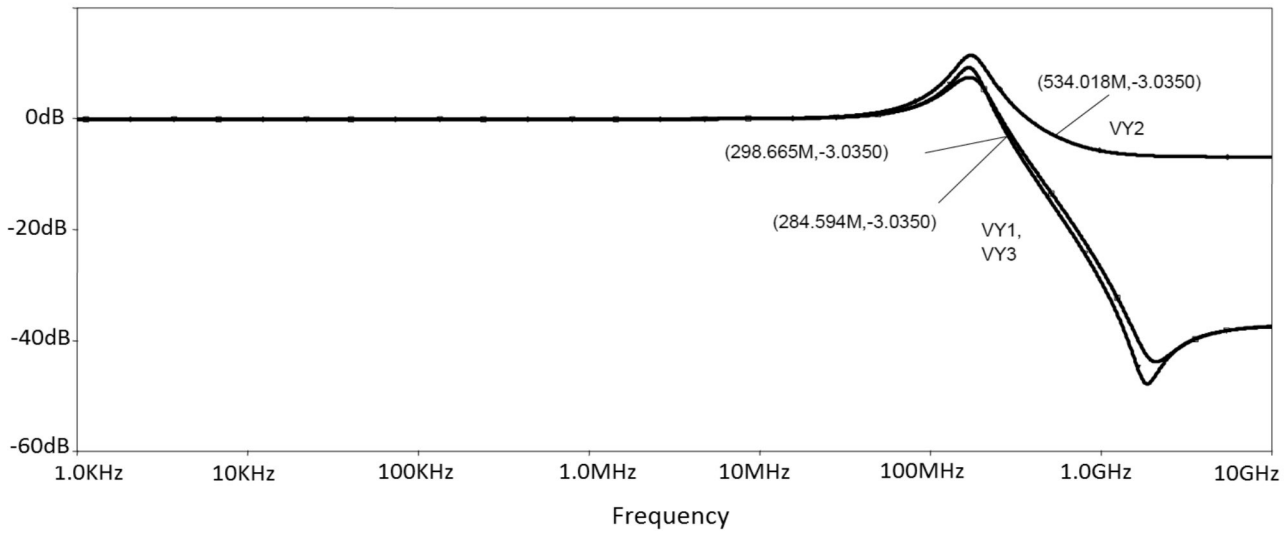


Figure 11: FGMOS FDCCII AC voltage transfer characteristics (V_{X1}-$V_{Y1, Y2, Y3}$)

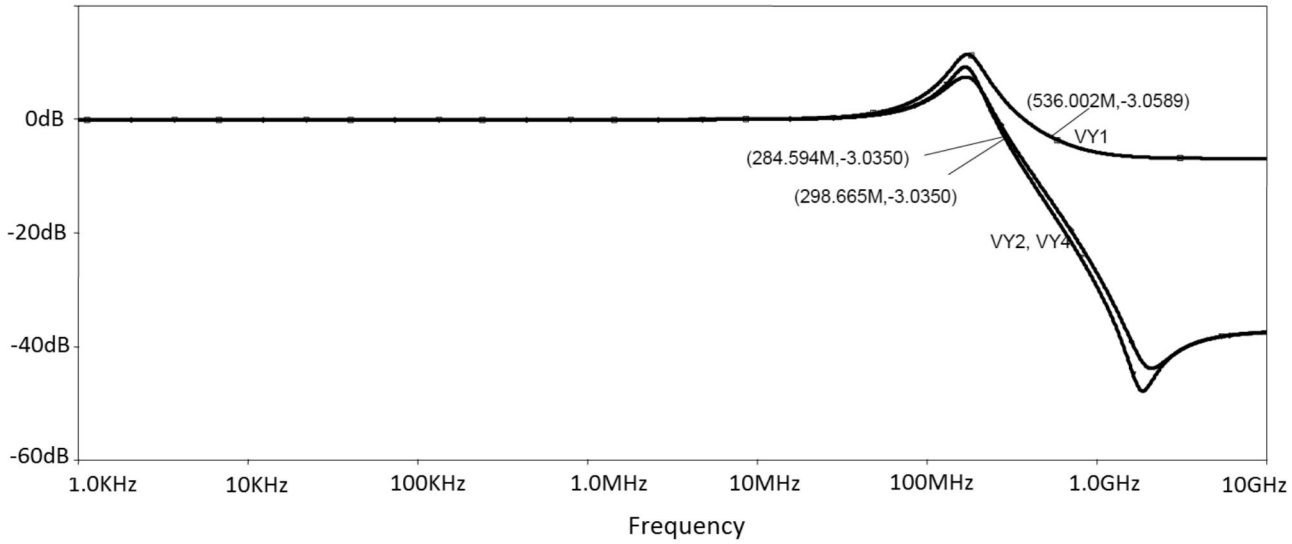


Figure 12: FGMOS FDCCII AC voltage transfer characteristics (V_{X2}-$V_{Y1, Y2, Y4}$)

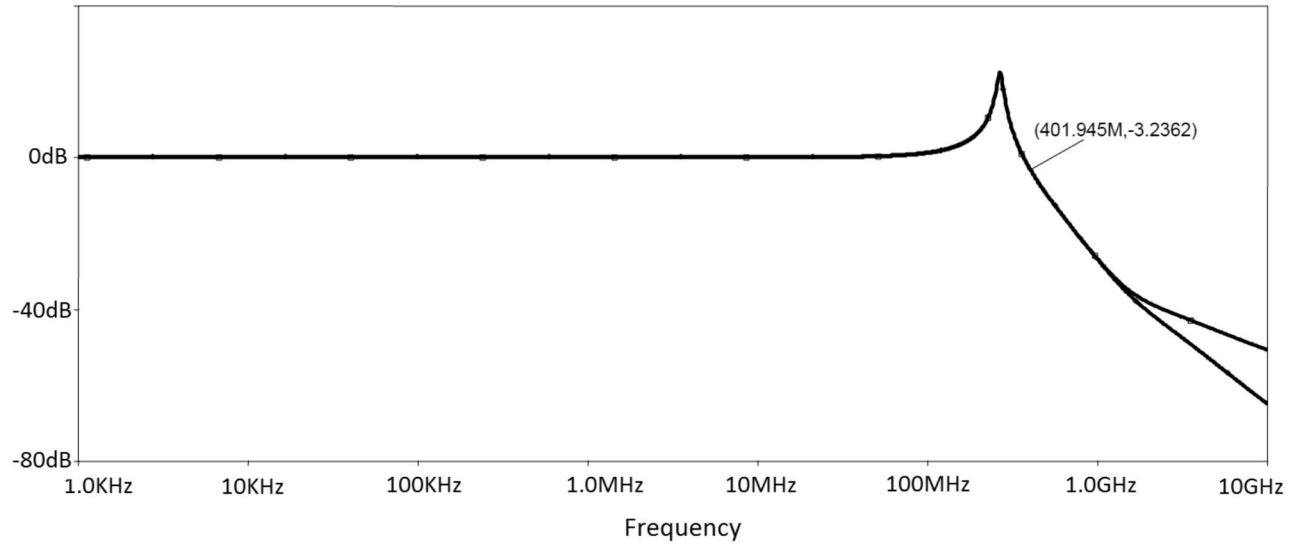


Figure 13: FGMOS FDCCII AC current transfer characteristics

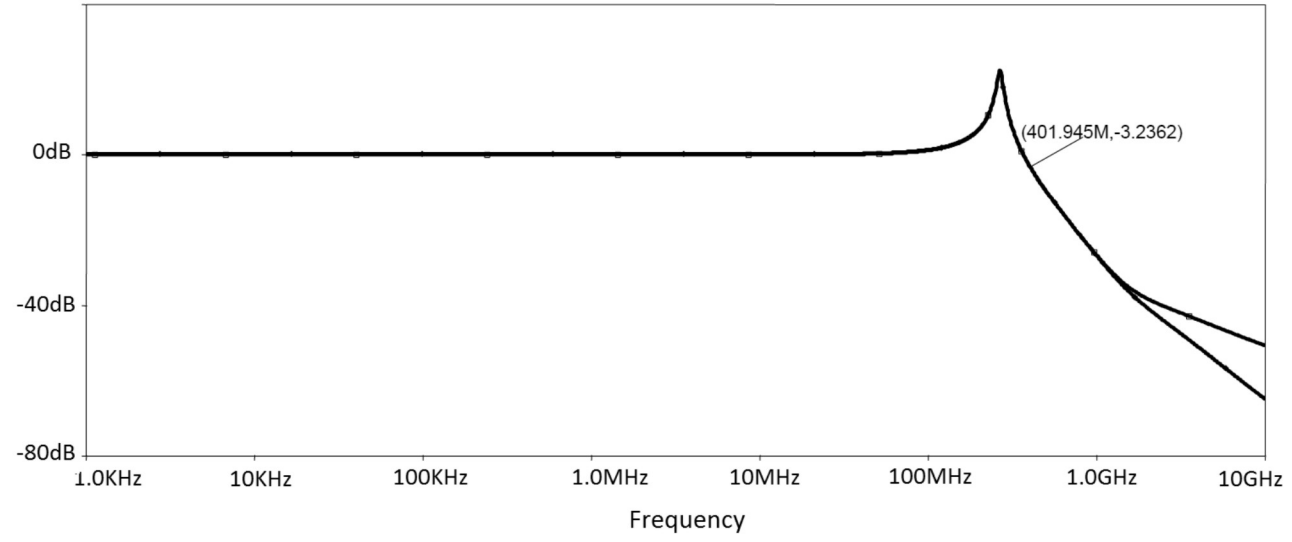


Figure 14: FGMOS FDCCII AC current transfer characteristics

Fig. 11 and Fig. 12 show the AC voltage transfer characteristics of the proposed circuit with respect to $V_{X1, X2}$ and $V_{Y1, Y2, Y3, Y4}$.

Fig. 13 and Fig. 14 show the AC current transfer characteristics of the proposed circuit with respect to $I_{X1, X2}$ and $I_{Z1, Z2, Z1', Z2'}$.

Impedance values of X1, X2, Y1, Y2, Y3 and Z nodes have been also determined as 1.46kΩ, 1.78kΩ, 1.43TΩ, 1.36TΩ, 1.43TΩ and 1.57MΩ, respectively. We considered V_{X1} (output) against V_{Y1}(input) at 10 MHz for THD (Total Harmonic Distortions) analysis. Fig.15 shows the THD variation of the proposed FGMOS circuit and the conventional CMOS circuit together during the input voltage swing of V_{Y1} change between 1mV and 400mV which is common input voltage gap for FGMOS and CMOS circuits.

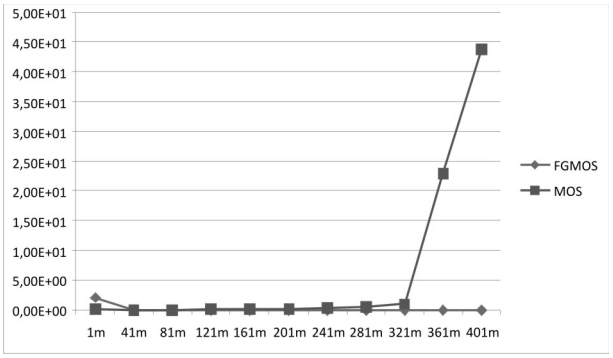


Figure 15: Total harmonic distortion (THD) values of the proposed FGMOS FDCCII and MOS FDCCII

5 Proposed filter as application example

In this section, current-mode and voltage mode two biquad filters have been presented. First proposed circuit is current-mode a biquad filter with single-input and three-outputs, which can simultaneously realize current mode low-pass, band-pass and high-pass filter responses employing all grounded passive components. The second proposed is voltag- mode biquad filter with three-inputs single-output, which can realize current mode low-pass, band-pass, high-pass, band-stop and all-pass filter responses employing single FDCCII.

The proposed current-mode filter is shown in Fig.16. Routine analysis of these circuits, which single-input three-output yields the following current-mode filter transfer functions:

$$\frac{I_{BP1}}{I_{IN}} = \frac{C_2 G_1 s}{G_1 G_2 + C_2 G_1 s + C_1 C_2 s^2} \quad (2)$$

$$\frac{I_{BP2}}{I_{IN}} = \frac{C_2 G_1 s}{G_1 G_2 + C_2 G_1 s + C_1 C_2 s^2} \quad (3)$$

$$\frac{I_{HP}}{I_{IN}} = \frac{C_1 C_2 s^2}{G_1 G_2 + C_2 G_1 s + C_1 C_2 s^2} \quad (4)$$

$$\frac{I_{LP}}{I_{IN}} = \frac{G_1 G_2}{G_1 G_2 + C_2 G_1 s + C_1 C_2 s^2} \quad (5)$$

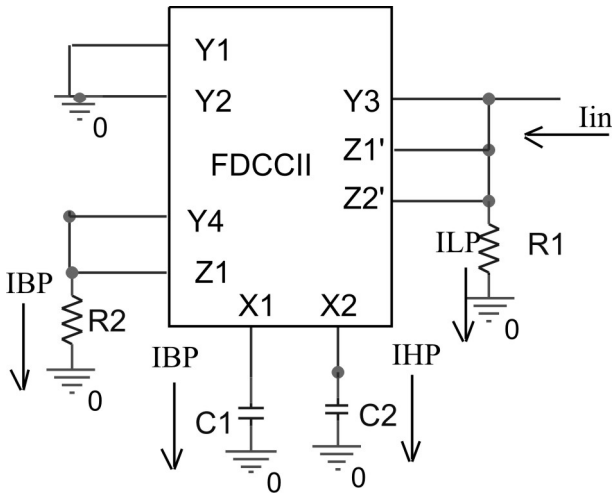


Figure 16: The proposed current-mode biquad filter employing FDCCII.

The resonance angular frequency ω_0 and the quality factor Q are given by

$$\omega_0 = \sqrt{\frac{G_1 G_2}{C_1 C_2}} \quad (6)$$

$$Q = \sqrt{\frac{G_1 C_1}{G_2 C_2}} \quad (7)$$

The passive sensitivities of Q and ω_0 are given as follows,

$$S_{G_1}^{Q} = -S_{G_2}^{Q} = S_{C_1}^{Q} = -S_{C_2}^{Q} = \frac{1}{2} \quad (8)$$

$$S_{G_1}^{\omega_0} = S_{G_2}^{\omega_0} = -S_{C_1}^{\omega_0} = -S_{C_2}^{\omega_0} = \frac{1}{2} \quad (9)$$

The second filter circuit can be used three-input single-output voltage-mode filter is shown in Fig. 17. Circuit analysis yields the following for the output voltage can be expressed as

$$V_O = \frac{G_1 G_2 V_1 - C_2 G_2 s V_2 + C_1 C_2 s^2 V_3}{G_1 G_2 + C_2 G_2 s + C_1 C_2 s^2} \quad (10)$$

Depending on the status of the input voltages V_1, V_2, and V_3, numerous filter functions are obtained. Special-

ization of the numerator yields the following voltage-mode filter transfer functions for the circuits.

(i) LP: $V_1 = V_{in}$ and $V_2 = V_3 = 0$,
(ii) BP: $V_2 = V_{in}$ and $V_1 = V_3 = 0$,
(iii) HP: $V_3 = V_{in}$ and $V_1 = V_2 = 0$,
(iv) BS: $V_1 = V_3 = V_{in}$, and $V_2 = 0$,
(v) AP: $V_1 = V_2 = V_3 = V_{in}$,

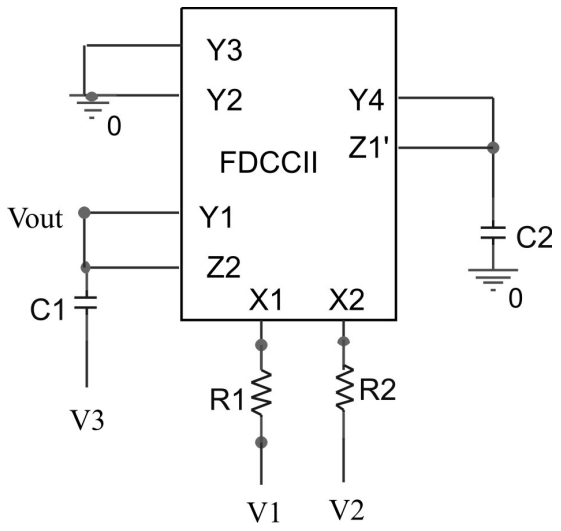


Figure 17: The proposed current-mode biquad filter employing FDCCII.

The resonance angular frequency ω_0 and the quality factor Q are given by

$$\omega_0 = \sqrt{\frac{G_1 G_2}{C_1 C_2}} \quad (11)$$

$$Q = \sqrt{\frac{G_1 C_1}{G_2 C_2}} \quad (12)$$

The passive sensitivities of Q and ω_0 are given as follows,

$$S_{G_1}^{Q} = -S_{G_2}^{Q} = S_{C_1}^{Q} = -S_{C_2}^{Q} = \frac{1}{2} \quad (13)$$

$$S_{G_1}^{\omega_0} = S_{G_2}^{\omega_0} = -S_{C_1}^{\omega_0} = -S_{C_2}^{\omega_0} = \frac{1}{2} \quad (14)$$

The current-mode biquad in Fig. 16 was designed for f_0 = 10 MHz by choosing $R_1 = R_2$ = 75kΩ, C_1 =0.3pF and C_2=0.15pF. Simulated response of high-pass, band-pass and low-pass filters topology shown in Fig. 18. For voltage mode filter in Fig. 17 has been design to provide high-pass, band-bass, low-pass, band-stop and all-pass responses with f_0 = 9.73 MHz. The passive component values are chosen as $R_1 = R_2$ = 75kΩ, C_1 =0.3pF and C_2=0.15pF. In Fig. 19 shows the simulated frequency responses for the high-pass, band-pass, low-pass, all-pass and band-stop configurations. As can be seen, there are a good agreement between theory and simulations.

Time domain analysis result is given in Fig. 20 for peak-to-peak 20 μA, 10 MHz sine wave input for current

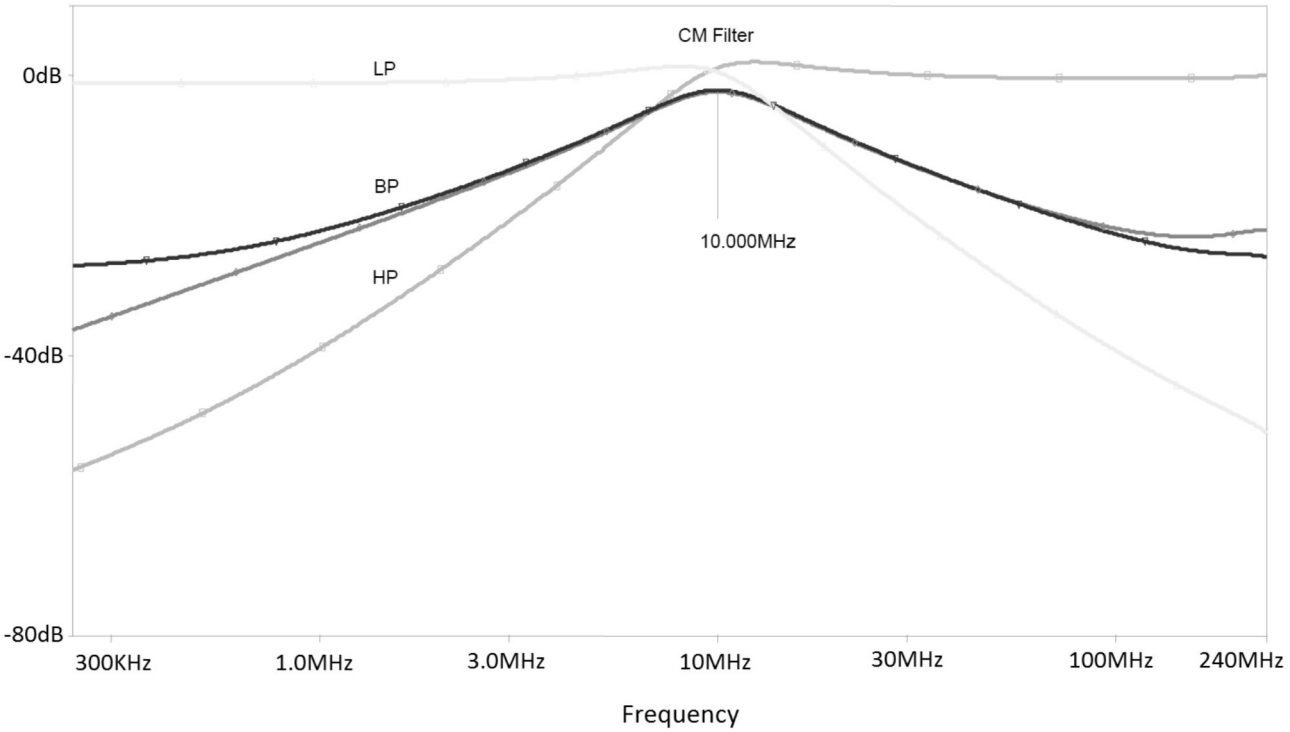


Figure 18: The simulated results of the gain–frequency responses of proposed curret-mode biquad filter

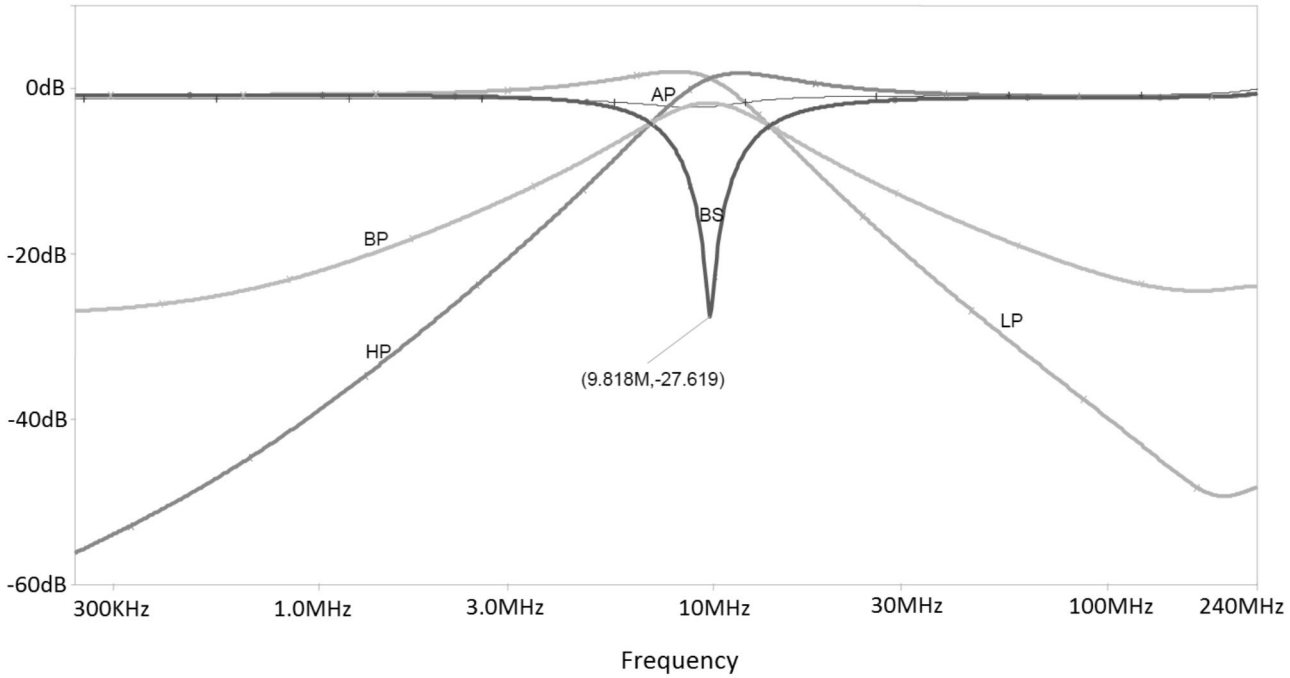


Figure 19: The simulated results of the gain–frequency responses of proposed voltage-mode biquad filter

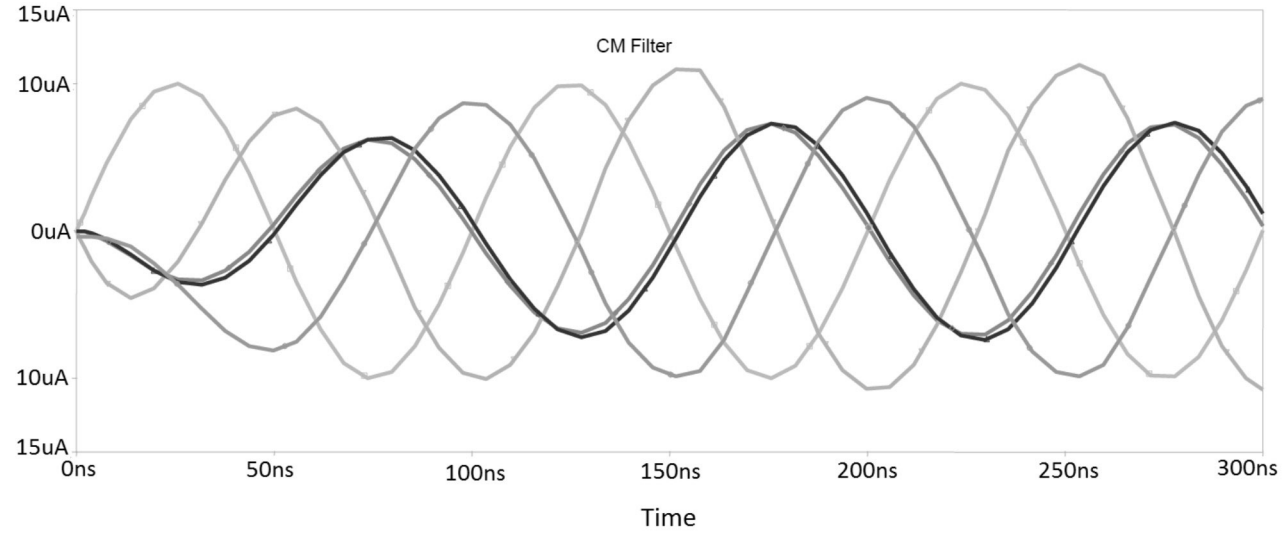


Figure 20: Time domain response of curret-mode filter

mode low-pass, band-pass and high-pass filters configuration for the circuit in Fig. 16. Time domain analysis result is given in Fig.21 for peak-to-peak 2V, sine wave at 9.73MHz input for voltage-mode low-pass filter. The large signal behavior of the circuit was tested by investigating the low-pass response on the input signal amplitude.

Fig. 22 shows the frequency response of curent-mode band-pass filter at 0°C, 25°C, 50°C and 100°C. As it is seen from the graphic frequency response of the filter almost does not change with respect to the temperature.

6 Conclusion

A new FGMOS FDCCII has been designed and simulated. By using FGMOS transistors both the input stage of the circuit providing the arithmetic calculations gets simpler also the linearity range increases due to the properties of FGMOS differential amplifier. The proposed FGMOS FDCCII is used in a tunable filter circuit in order to show the versatility of the FDCCII block. We can conclude that proposed FGMOS FDCCII structure provides the circuit designer further possibilites of realizing active circuits by reducing the number of transistors and extending the linearity range.

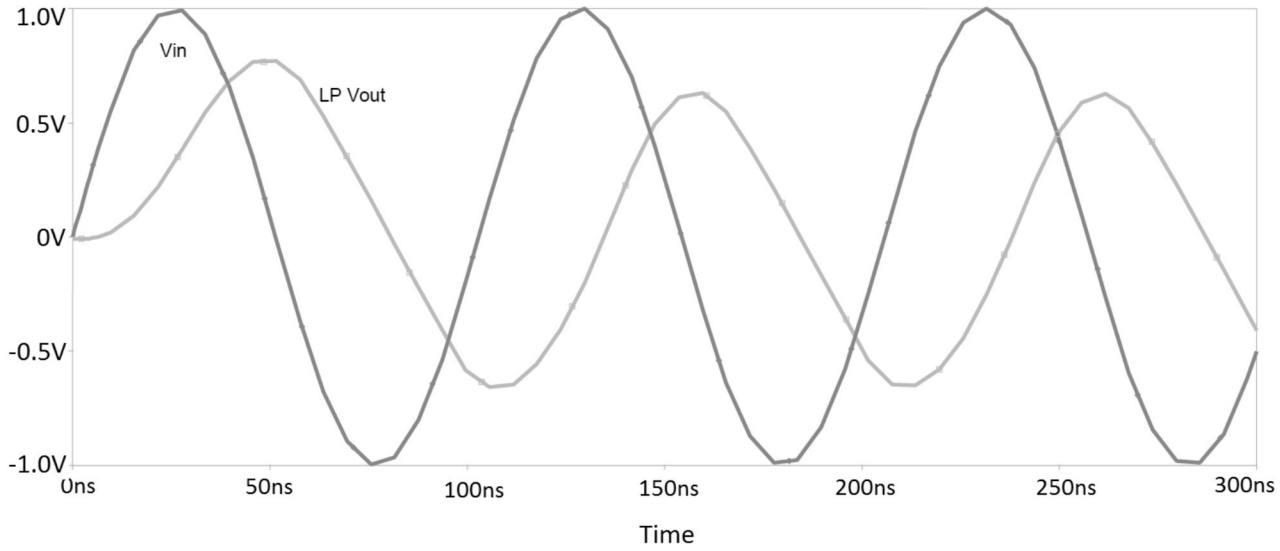


Figure 21: Time domain response of voltage-mode low-pass filter

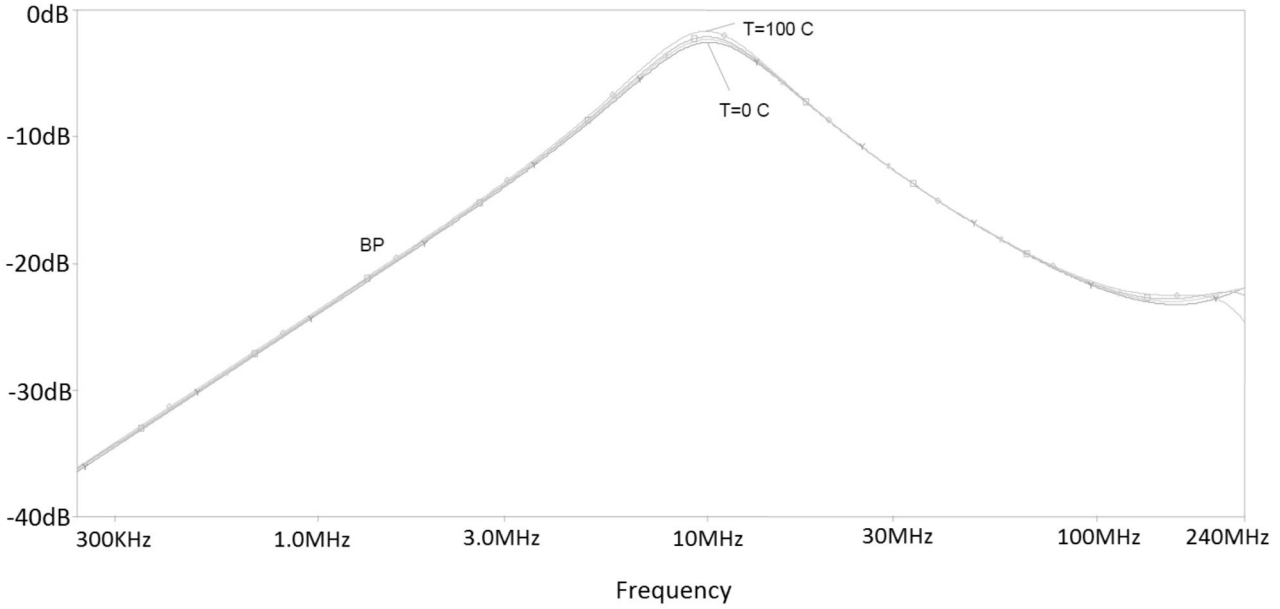


Figure 22: Frequency response of curent-mode band-pass filter at 0°C, 25°C, 50°C and 100°C

7 References

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