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Back Propagation Neural Network in Predicting the Thermal Fatigue Life of Microelectronic Chips

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Abstract: The present study gives an efficient approach to predict the thermal fatigue lives of microelectronic chips under cyclic thermal load using back propagation (BP) artificial neural network method. Strain based and stress-strain based thermal fatigue life models are established, respectively, according to the experimental results of thermal fatigue tests and the singularity parameters at the failure interface calculated by finite element method (FEM). According to the existing FEM results, the BP approach is configured to predict the singularity parameters at the failure interface in the new chips once the dimensions and thermal-mechanical properties of solders are obtained. By comparison, the predicted thermal fatigue lives according to the established thermal fatigue life models are in good agreement with the experimental results. The thermal fatigue life prediction of microelectronic chips based on the BP network approach is feasible.

Keywords: thermal fatigue, microelectronic chips, BP, singularity parameters, life prediction

Nevronske mreže z vzvratnim širjenjem pri napovedovanju temičnega utrujenosti mikroelektronskega čipa

Izvleček: Članek predstavlja učinkovit način napovedovanja življenjske dobe mikroelektronskega čipa zaradi termičnega staranja pri cikličnih termičnih obremenitvah z uporabo nevronskih mrež z vzvratnim širjenjem. Vzpostavljeni so modeli termične utrujenosti glede na rezultate poskusov in izračunov parametrov singularnosti po metodi FEM. Primerjava novih in obstoječih modelov je pokazala dobro ujemanje z rezultati meritev. Napovedovanje termične utrujenosti čipov na osnovi BP mrež je mogoče.

Ključne besede: termična utrujenost; mikorelektronski čip; BP; singularnost; napovedovanje življenjske dobe

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1. Introduction

The electronics industry is mainly driven by the demand for smaller size with lower power consumption while having increased functionality and lower cost. Because of high-density and cost-effective performance, microelectronic chip has been widely used as the core component of automatic control and power converters in various industrial field [1, 2]. Exposed to the switching on-off and random fluctuations of power in the actual operation, the microelectronic chipset is often subjected to cyclic temperature loads. At the same time, the multi-layer package structure inherent in power electronics has an interface layer of a plurality of different materials inside. When the interface layer is under the action of cyclic temperature load, the irreversible plastic deformation accumulates from the interface, due to the mismatch of the coefficients of thermal expansion in different layers. When the cumulative plastic deformation reaches a critical level, the crack begins to nucleate and grow, and finally the device is permanently ineffective [3-6]. The solder layer plays an important role in the mechanical and electric connections, therefore, its performance, especially, thermo-mechanical properties, has become an important factor affecting the whole reliability of the microelectronic chips. Generally, the strength and failure properties joints are dominated by the properties of both the solder material itself and the interface bonding [7, 8]. To obtain the

excellent interface bonding, usually the solder material needs to satisfy the following requirements: 1) proper melt temperature; 2) excellent wettability or adhesive properties; 3) enough strength for bonding. Besides, adaptation to surroundings becomes much more important from the social requirements [9, 10]. However, such requirements for the solder materials cannot give a quantitative evaluation of strength and thermal fatigue life for older joints. To give a proper estimation of strength and thermal fatigue life, numerical analysis and failure criterion (including thermal fatigue law) are necessary to obtain the parameters describing the stress or strain state and the evaluation criteria [11-13]. Since Hattori et al. [14] suggested a singularity parameter approach for the interface reliability of plastic IC packages using two stress intensity parameters that characterize the stress distribution near a bonded edge along the interface, similar methods had been widely adopted to predict the crack initiation or delamination of the microelectronic chip [15, 16]. However, such a method, strictly, is based on the concept of point failure, which may difficultly be observed by the physical experiment, and is valid only for the cases that the geometric shape of the solder joints and the loading conditions are the same with that used to build up the fatigue law [17, 18]. Meanwhile, the stress intensity factor at the edge of the interface is always dependent on the test condition, assembly geometry, mechanical property of materials and their interactions, as well as the impact of process parameters [19, 20], which leads to the result that the precise models and a large amount of calculation are necessary to obtain the stress intensity factors at the failure interfaces of different chips. Soft-computing is doubtless a good alternative for handling this complex problem as it is tolerant of imprecision and uncertainty. Up to date, various soft-computing methods, e.g. artificial neural network [21-23], and genetic programming (GP) [24, 25] have been used in the field of thermal fatigue.

In the present work, the thermal fatigue life models of microelectronic chips based on interfacial singular stress-strain fields are established. Thermal fatigue tests are carried out to obtain the thermal fatigue lives of the chips, and the three dimensional finite element thermal mechanical analysis is also conducted to get the singularity parameters at the failure interface. Therefore, the parameters in the established model are determined. Also, to save the workload of calculating singularity parameters of new chips, an attempt has been made to predict these parameters by applying the BP neural network approach and accordingly, the thermal fatigue lives of these chips can be calculated.

2. Thermal fatigue prediction model

2.1 Thermal fatigue test

Five types of chips, denoting as I-V chips, are packaged in one chipset. The working powers of I-V chips are 35.7, 33.3, 25.8, 20.0 and 14.5 w, respectively. Each chip has the same layered stacking structure, and the materials from top to bottom are, in order, silica gel, wafer (silicon), solder Pb-5Sn, Cu, solder SnAg3Cu0.5, Cu, insulate layer, and the substrate, as shown in Fig. 1. Before the thermal fatigue tests, the silica gel protector is cleaned and the chips are cut out from the chipset by a wire cutter. The cyclic temperature varies from -40 to 90 °C in the thermal fatigue test, as shown in Fig. 2. It is accomplished by the specially designed heating box inserted in a bigger low temperature container which is always kept -40 °C by the liquid nitrogen. When the chips are heated, the sliding door of the heating box is close, the embedded heating tubes work. When cooled, and the sliding door is open and the heating tubes are powered off. All the chips are put into a same heating box to undergo the cyclic temperature load.

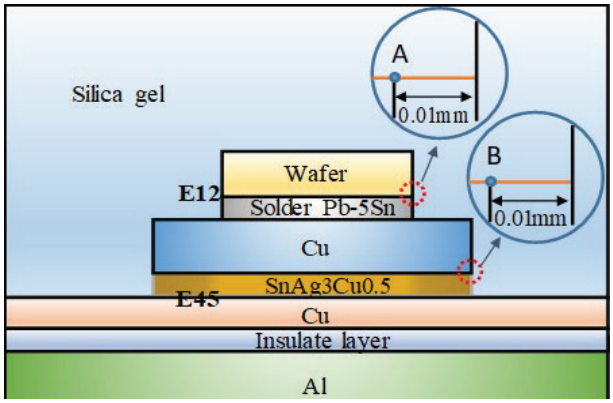

Figure 1: Structure of the chip

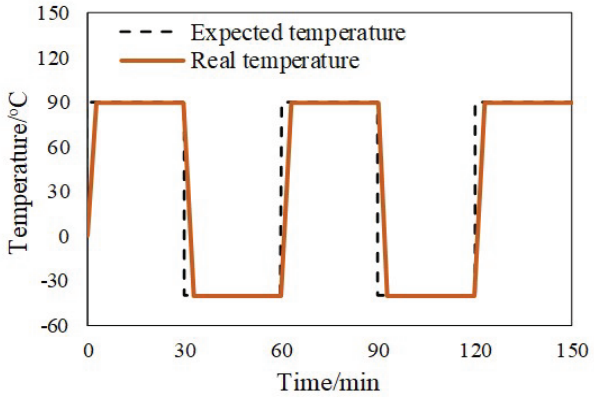

Figure 2: Ambient temperature cycles

To detect the fatigue failure, the electric resistance of the chips measured by a digital resistance meter for certain

intervals. According to the sketch of electronic resistance variation during the thermal cycles, the crack morphology of chip IV when the electronic resistance increasing (RI) reaches 10 % and 15 % are respectively observed by the JSM-6301F scanning electron microscope (SEM) (JEOL, Tokyo, Japan). The samples are covered by carbon before and the analysis is conducted under 20 kV in the SEI mode, the observed SEM images are shown in Fig. 3. It can be seen that many micro-cracks appear at the interface between the wafer and solder Sn-5Pb (E12) at 10 % RI, and the micro cracks have gradually merged into a main crack when RI reaches 15 %. While at this time micro cracks start to appear at the interface between solder SnAg3Cu0.5 and Cu (E45). The locations of the E12 and E45 have been demonstrated in Fig. 1, and the representative data points at the E12 and E45 are also selected to analyze the connection between cyclic stress-strain variations from FEM analysis to the experimental thermal fatigue cracking. It is interesting that the main crack also comes into being firstly from the E12 in the other four chips. For the convenience, we define the fatigue life limit Nf when the electronic resistance increasing reaches 15 % [26]. Fig. 4 shows the measured electronic resistance variations of each chip, and the tested fatigue life Nf is listed in Table 1.

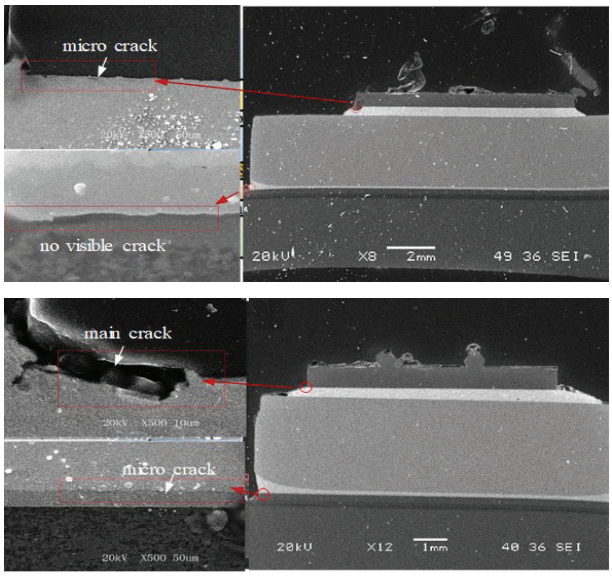

Figure 3: SEM observations of fatigue crack morphology of IV chip: (a-c) 10% RI, (d-f) 15% RI

Table 1: Fatigue life limit N_f for the tested I-V chips

Chip type	I chip	II chip	III chip	IV chip	V chip
N_f/cycles	910	830	1030	980	1040

2.2 FEM analysis

Three dimensional thermal conduction and thermal stress analysis have been carried out to obtain inter-

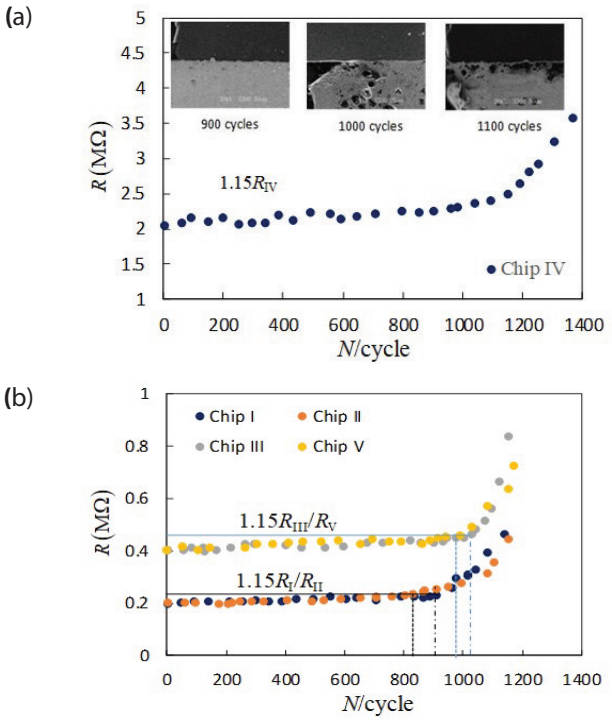

Figure 4: (a)Electronic RI with thermal cycles and (b) the corresponding thermal fatigue lives

facial stress-strain fields of the chips undergoing the cyclic thermal load. The load condition is the same as what applied in the thermal fatigue tests. Here IV chip is taken as an example to depict the general features. To obtain the accurate stress and strain distribution at the interface, FEM submodel analysis is carried out, and the boundary condition of the submodel is obtained from the former thermal conduction and stress analysis of the whole chipset by automatic interpolation, as shown in Fig. 5.

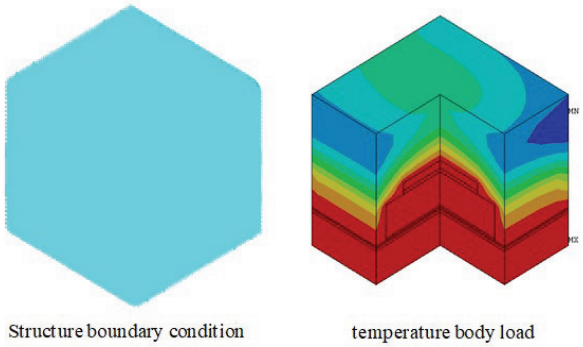

Figure 5: Boundary condition interpolation

Fig. 6 shows the stress variation at the E12 and E45 with thermal cycles, where $\sigma t=(\sigma^2+\tau^2)^{1/2}$ donates the maximum traction when the normal stress is tensile at the interface. It can be found that the E12 is under compress, while the E45 is under tension at the heating

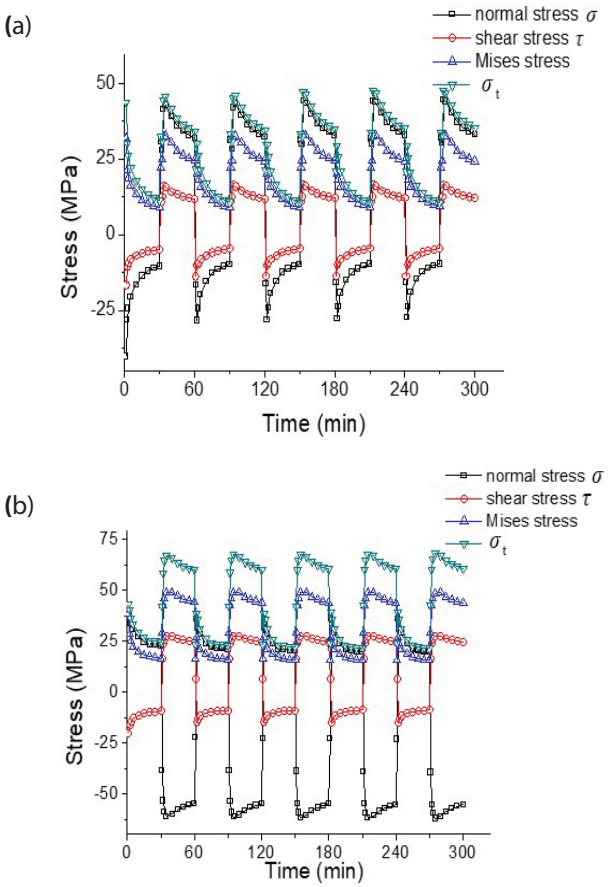

Figure 6: Stress variation near the interface edge: (a) E12; (b) E45

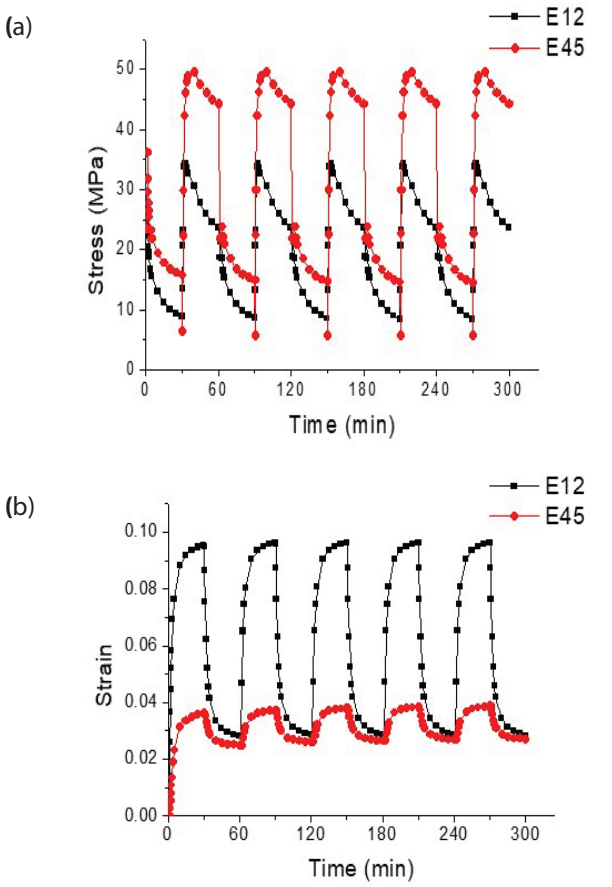

Figure 7: Comparison of E12 and E45: (a) Mises stress (b) Equivalent strain.

step. However, the opposite is true at the cooling step. There are two stress shocks, one is in the heating process and the other in the cooling process. The second shock is much stronger than the first one. The stress near the edge varies in the first several cycles, but it is saturated after 3 cycles. Fig. 7 shows the variations of Mises stress and equivalent strain at the E12 and E45. It can be seen that the stress range is severe at the E45, but the strain range is severe at the E12 since Pb5Sn is softer. Therefore, it follows that the actual fatigue failure mode is determined by the coupling stress and strain controlled mechanism.

According to the instant singular field theory [27-29],

$$\sigma_i = \frac{K_i(t)}{r^{\delta_i(t)}}, \quad \varepsilon_e = \frac{K_\varepsilon(t)}{r^{\varsigma(t)}} \tag{1}$$

where $K_i(t)$ and $K_s(t)$ denote the stress and strain intensity factors, $\delta i(t)$ and $\varsigma(t)$ are the stress and strain singular orders, i = σ, τ denotes the normal and shear stress, respectively, and r denotes the distance from the singular edge.

Picking up the stress and strain distributions at the corresponding steady states along the interface edge, the

Table 2: Singular stress field parameters at the E12 interface edge

Chip No.	Maximum stress state in the heating step				Maximum stress state in the cooling step			
	Normal Stress		Shear Stress		Normal Stress		Shear Stress	
	δ_σ	K_σ /MPa.mm$^\delta$	δ_τ	K_τ /MPa.mm$^\delta$	δ_σ	K_σ /MPa.mm$^\delta$	δ_τ	K_τ /MPa.mm$^\delta$
I	0.04119	-20.53	0.03882	-9.382	0.1551	13.59	0.04223	14.00
II	0.04305	-19.98	0.04005	-9.202	0.1524	12.99	0.04350	13.59
III	0.05363	-18.12	0.03861	-9.241	0.1627	12.55	0.04298	13.75
IV	0.04186	-19.55	0.04144	-8.939	0.1559	12.63	0.04431	13.45
V	0.05254	-17.77	0.03867	-9.134	0.1758	11.30	0.04137	13.66

Table 3: Singular stress field parameters at the E45 interface edge

Chip No.	Maximum stress state in the heating step				Maximum stress state in the cooling step			
	Normal Stress		Shear Stress		Normal Stress		Shear Stress	
	δ_σ	K_σ /MPa.mm$^\delta$	δ_τ	K_τ /MPa.mm$^\delta$	δ_σ	K_σ /MPa.mm$^\delta$	δ_τ	K_τ /MPa.mm$^\delta$
I	0.04012	27.18	0.03184	-12.87	0.01688	-53.85	0.04195	19.78
II	0.03348	28.71	0.03523	-12.14	0.01957	-52.44	0.04322	19.18
III	0.07525	21.58	0.02823	-13.35	0.07769	-35.02	0.03464	21.57
IV	0.07966	21.23	0.02806	-13.40	0.11488	-27.59	0.03080	22.52
V	0.1171	16.42	0.02805	-13.36	0.1629	-19.83	0.03049	22.53

If a unit length is taken, Eq. (3) can be simplified as

Table 4: Singular strain field parameters at the E12 and E45 interface edges

Chip No.	E12				E45			
	Maximum state		Minimum state		Maximum state		Minimum state	
	ς	K_ε / mm$^\varsigma$	ς	K_ε / mm$^\varsigma$	ς	K_ε / mm$^\varsigma$	ς	K_ε / mm$^\varsigma$
I	0.5855	2.166E-03	0.5660	9.871E-04	0.5482	1.156E-03	0.6585	1.297E-04
II	0.5829	1.853E-03	0.5768	7.819E-04	0.5647	8.242E-04	0.7642	2.398E-05
III	0.5745	1.661E-3	0.5588	7.514E-04	0.4760	2.433E-03	0.6023	2.093E-04
IV	0.5883	1.322E-03	0.5854	5.773E-04	0.4654	2.823E-03	0.6011	2.429E-04
V	0.5775	1.312E-03	0.5599	6.341E-04	0.4384	3.728E-03	0.5710	2.785E-04

stress and strain intensity factors and singular orders can be determined numerically. Applying the FEM submodel analysis to each chip, the singularity parameters as described above are summarized and listed in Tables 2-4, respectively.

2.3 Thermal fatigue models based on interfacial singularity

Thermal cycles lead to the coupled stress and strain cycles, though their peaks do not appear simultaneously, which attributes to the visco-properties of solder materials. This fact means that both stress and strain cycles contribute to thermal fatigue failures. Instead of using stress or strain as the parameters for thermal fatigue life evaluation, here the stress and strain intensity factor ranges and their corresponding singular orders are adopted to formulate the thermal fatigue law. At the interface edge, the ranges of stress and strain are written as

$$\Delta\sigma_j = \frac{K_{j\max}}{r^{\delta_{\max}}} - \frac{K_{j\min}}{r^{\delta_{\min}}}, \Delta\varepsilon = \frac{K_{\varepsilon\max}}{r^{\varsigma_{\max}}} - \frac{K_{\varepsilon\min}}{r^{\varsigma_{\max}}} \tag{2}$$

For the materials with tiny defects, the fatigue strengths and thresholds of fatigue crack propagation match those without defects. Namely, only several points with large stress in materials generally cannot affect fatigue characteristics. Therefore, using the stress-strain range within a region to describe the thermal fatigue behavior is more accurate than only by one or two points. Here the concept of characteristic length of fatigue failure is introduced, i.e., when the average stress or strain range within a characteristic length l arrives at or exceeds the fatigue limit, the thermal fatigue crack begins to initiate or propagate [30]. The average stress range $\Delta\bar{\sigma}$ within l at the interface edge can be expressed as

$$\Delta\bar{\sigma} = \frac{1}{l}\left[\int_0^l \frac{K_{\max}}{r^{\delta_{\max}}}dr - \int_0^l \frac{K_{\min}}{r^{\delta_{\min}}}dr\right] = \\ = \frac{1}{l^{\delta_{\max}}}\frac{K_{\max}}{1-\delta_{\max}} - \frac{1}{l^{\delta_{\min}}}\frac{K_{\min}}{1-\delta_{\min}} \tag{3}$$

If a unit length is taken, Eq. (3) can be simplified as

$$\Delta\bar{\sigma} = \frac{K_{\max}}{1-\delta_{\max}} - \frac{K_{\min}}{1-\delta_{\min}} \tag{4}$$

Then the range of stress and strain intensity factors can be written as

$$\Delta K_\sigma = \frac{K_{\sigma\max}}{1-\delta_{\sigma\max}} - \frac{K_{\sigma\min}}{1-\delta_{\sigma\min}}, \Delta K_\tau = \\ = \frac{K_{\tau\max}}{1-\delta_{\tau\max}} - \frac{K_{\tau\min}}{1-\delta_{\tau\min}}, \Delta K_\varepsilon = \frac{K_{\varepsilon\max}}{1-\varsigma_{\max}} - \frac{K_{\varepsilon\min}}{1-\varsigma_{\min}} \tag{5}$$

where ΔK_σ and ΔK_τ represent the multi-axes effects when both normal and shear stress are considered.

Therefore, strain-controlled and stress-strain controlled fatigue laws are respectively considered, as shown in Eqs. (6-7).

$$\left(\Delta K_{\varepsilon}\right)^{m_1} N_{\mathrm{f}} = C_{\varepsilon} \tag{6}$$

$$\left(\Delta K_{\varepsilon}\right)^{m_1}\left[\left(\Delta K_{\sigma}\right)^2 + \left(\Delta K_{\tau}\right)^2\right]^{m_2} N_{\mathrm{f}} = C_{\varepsilon\sigma} \tag{7}$$

where m_1, m_2, C_ε, and $C_{\varepsilon\sigma}$ are constants determined by test results.

By fitting the results of thermal fatigue tests and the singularity parameters at the failure interface obtained from FEM analysis, one obtains

$$\left(\Delta K_{\varepsilon}\right)^{0.4} N_{\mathrm{f}} = 87.9 \tag{8}$$

$$\left(\Delta K_{\varepsilon}\right)^{0.4}\left[\left(\Delta K_{\sigma}\right)^2 + \left(\Delta K_{\tau}\right)^2\right]^{1.74} N_{\mathrm{f}} = 3.93\times10^{7} \tag{9}$$

Theoretically, once the stress-strain intensity factors and their singular orders at the failure interfaces of new chips are obtained, their thermal fatigue lives can be predicted. However, the calculation of thermal mechanical analysis to get the singularity parameters at the failure interface is not easy and time-consuming for the engineers. Therefore, a BP neural network based method is necessary to be established for the singularity parameters to predict the thermal fatigue life.

3. BP model for thermal fatigue life prediction

3.1 Principle of BP neural network

The classic BP artificial neural network is a three or more than three layers hierarchical forward neural networks (i.e. including an input layer, an output layer, and one or more hidden layers). The algorithm consists of two parts: the forward transmission of information and the back propagation of errors. In the forward transfer process, the input information passes to the output layer through the hidden layer. If the desired output is not obtained at the output layer, the error change value of the output layer is calculated, and the network passes the error signal back along the original connection path and modifies the weight of neurons in each layer until the desired goal is reached [31]. Therefore, it is user-kind to clear these mathematical difficulties by a black box. Since the singular orders and intensity factors can be expressed in following form,

$$K, \varsigma = f\left(\text{load condition, geometry, material properties, } \cdots\right) \tag{10}$$

It is possible to estimate the singular orders and intensity factors by a trained neural network instead of FEM analysis. However, to train an efficient neural network, a huge amounts of FEM analysis results as the samples for training are necessary. That is, the user can obtain the singular orders and intensity factors of new chips simply through the well trained neural networks.

3.2 Variables in BP model

The logical route of the developed method is shown in Fig. 8. To reach the stated goal of BP network predicting the stress-strain intensity factors and their singular orders, four variables, i.e., elasticity of modulus E, thickness t and width w of solder Pb-5Sn, and cyclic temperature range ΔT, are considered and used as the parameters of the input layer of BP network. According to the different values of input variables, 60 sets of samples are prefabricated from FEM simulation, among which 50 sets are selected as training data, and the remaining 10 sets are used as test data.

3.3 Predicted results

The BP model for thermal fatigue life prediction is accomplished by the MATLAB neural network toolbox. The parameters of BP network, including the neuron number in the hidden layer, target error, learning rate are set to 13, 0.0001, and 0.35, respectively. When the testing results meet the accuracy requirement, the

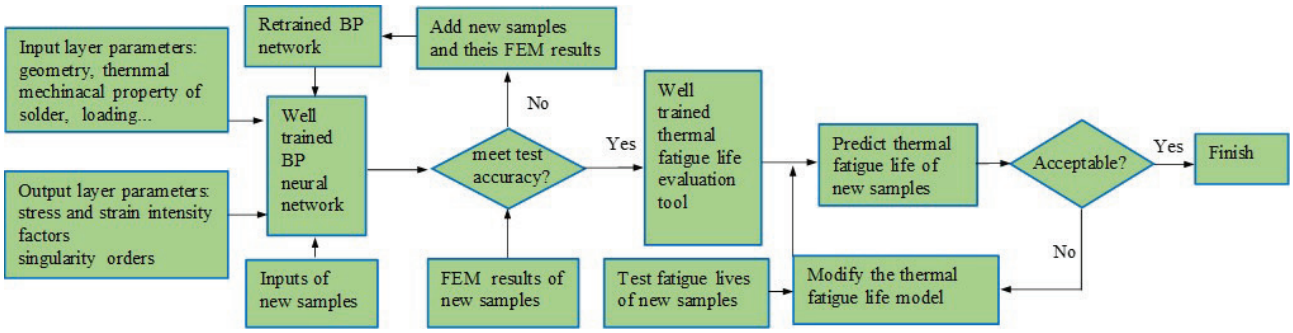

Figure 8: Logical route of developed thermal fatigue life prediction

trained BP network can be used to predict the singular orders and intensity factors in different stages. The detailed input data of the chips to be predicted are listed in Table 5, and the predicted intensity factors (Kσ, Kτ, Kε) and their corresponding singular orders (δσ, δτ, ε) of E12 at steady states are depicted in Figs. 9-11, respectively. The FEM results of these chips are also listed for comparison. The average predicting error of Kσ, Kτ, Kε and δσ, δτ, ε at the heating and cooling stages are 2.13 %, 3.32 %, 5.04 %, 2.04 %, 4.89 %, 3.67 %, 4.78 %, 1.67 %, 1.31 %, 2.87 %, 1.93 %, and 3.90 %, respectively, indicating that the trained BP neural network can predict the stress-strain intensity factors and singular orders at the failure interface with good accuracy.

When the singular parameters at the heating and cooling stage are predicted, the thermal fatigue lives of the chips can be calculated by Eqs. 8-9, as listed in Table 6. When compared with the tested results, the stress-strain controlled fatigue law can get more accurate predicting results than strain controlled one strain-controlled, indicating that the thermal fatigue failure of the chips is not just governed by strain, but by the

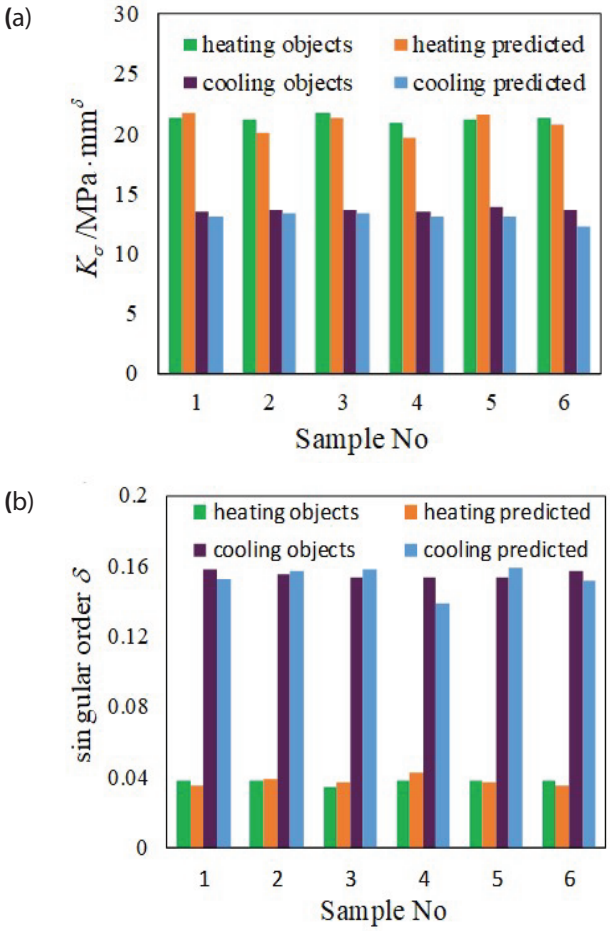

Figure 9: Predicting results of BP network for normal stress field: (a) Intensity factors, (b) Singular orders

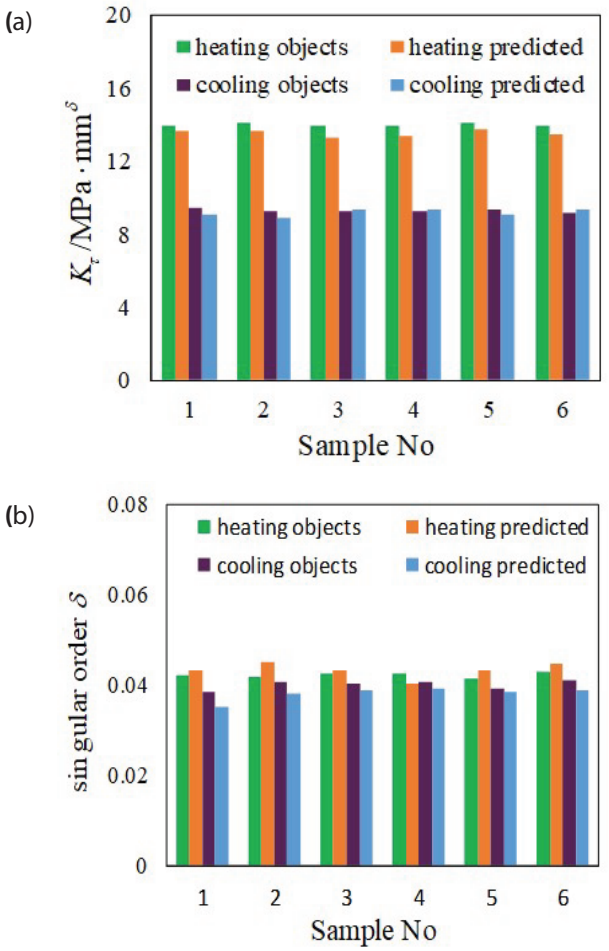

Figure 10: Predicting results of BP network for shear stress field: (a) Intensity factors, (b) Singular orders

mutual effect of interfacial stress and strain. On the whole, the differences between the predicted outputs and experimental results are quite small. The thermal fatigue life prediction method of microelectronic chips based on the BP neural network is feasible.

Table 5: Predicting inputs of BP network

Sample No.	Chip type	t /mm	w /mm	E /GPa	ΔT /°C
1	I	0.24	6.6	16.10	130
2	II	0.22	7.0	16.24	120
3	III	0.22	6.6	16.91	130
4	IV	0.22	6.8	15.62	110
5	V	0.23	6.4	16.12	130
6	II	0.21	6.6	16.58	120

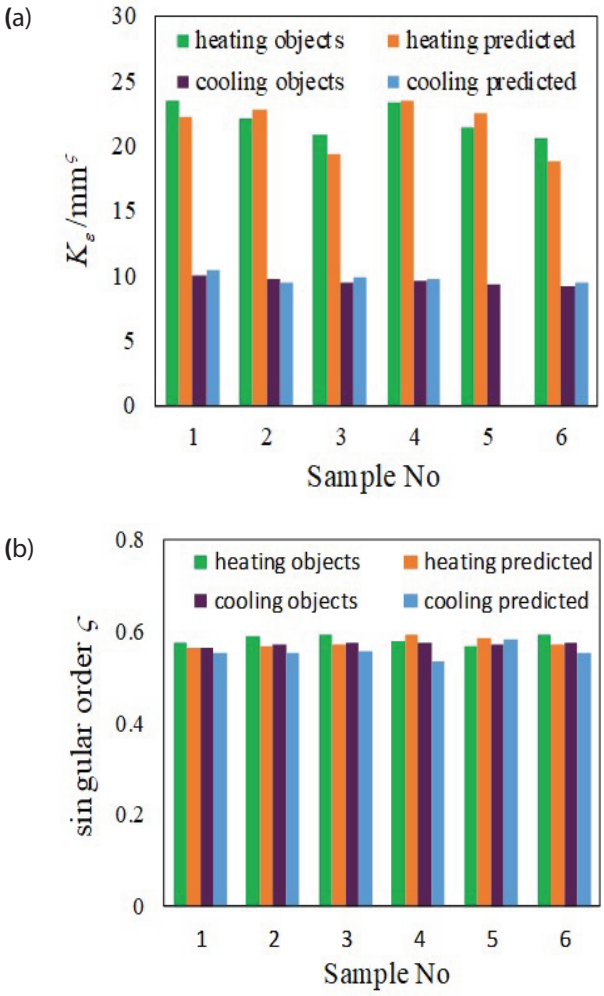

Figure 11: Predicting results of BP network for strain field: (a) Intensity factors, (b) singular orders

Table 6: Comparison of predicted and tested thermal fatigue lives of the selected chips: (a) Intensity factors, (b) singular orders

Sample No.	Chip type	Tested life / cycles	Predicted life/cycles			
			Eq. (8)	Error /%	Eq. (9)	Error /%
1	I	970	1008	3.92	983	1.65
2	II	890	951	6.85	857	3.71
3	III	1070	1014	-5.23	1090	1.87
4	IV	1060	1110	4.50	1108	1.87
5	V	1010	942	6.73	1053	4.26
6	II	950	1014	6.31	986	3.79

4 Conclusions

The present study gives an efficient approach for the thermal fatigue lives prediction of microelectronic chips under thermal cycles using the BP method. Thermal fatigue tests and FEM stress–strain singularity analysis at the failure interfaces are conducted to establish the interfacial singularity based thermal fatigue life prediction model. To save the calculation, a BP neural network model is established to predict the interfacial singularity parameters of new chips. The results show that the established BP method can effectively predict the necessary singularity parameters for thermal fatigue life evaluation. Strain-controlled and stress-strain controlled thermal fatigue models can both give reasonable prediction. The application of the thermal fatigue models demonstrates a fact that the thermal fatigue of chips can be evaluated uniformly no matter what the shapes, dimensions and the thermo-mechanical properties of the solders are, as long as the relevant stress–strain intensity factor and singular parameters at the failure interface can be obtained.

However, as the outcome of numerical analysis and experimental results, the thermal fatigue model involves several factors such as the local interfacial singularity, the diversification of singular field parameters in the FEM analysis, and the measurement of thermal fatigue life during physical experiments throughout the modeling process. Further research based on other computational intelligence approaches, like computational intelligence aided design, can be employed to predict thermal fatigue lives under different loading conditions.

5 Acknowledgements

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6 Conflict of interest statement

The authors declare no conflicts of interest.

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