

# CMOS High-Performance 5-2 and 6-2 Compressors for High-Speed Parallel Multipliers

Ali Rahnamaei

Islamic Azad University, Ardabil Branch, Department of Electrical Engineering, Ardabil, Iran

**Abstract:** In this article, the design procedure for high-speed 5-2 and 6-2 compressors, along with their analysis, has been discussed. With the help of the combinational logic consisting of the 4-2 compressor and 3-2 counter blocks, a high-performance structure for 6-2 compressor has been achieved, which shows significant speed improvement over previous architectures. The optimization has been carried out by reducing the carry rippling issue between the adjacent compressor structures. Also, the help of some modifications, the proposed 6-2 compressor will turn into a 5-2 compressor where the latency of the critical path has considerably been reduced, illustrating the superiority of designed circuits. The corresponding latencies of the proposed 5-2 and 6-2 structures are equal to 3.5 and 4 XOR logic gates, respectively, demonstrating speed boosting of 15% and 20% compared to the best-reported architectures. In addition, the power consumption and the transistor count of proposed circuits are have remained at a moderate level. Therefore, by considering the Power-Delay Product (PDP), our work will be a good choice for high-speed parallel multiplier design. Post-layout simulation results based on TSMC 90nm standard CMOS process and 0.9V power supply have been presented to confirm the correct functionality of the implemented compressors. These results have also been used as a fair comparison infrastructure between the proposed works and redesignated architectures of the previously reported schemes.

**Keywords:** 6-2 compressor; 5-2 compressor; multiplier; CMOS; high-speed

## Visoko učinkovit CMOS 5-2 in 6-2 kodirnik za vzporedne množilnike velikih hitrosti

**Izveček:** V članku je predstavljen postopek načrtovanja in analiza hitrega 5-2 in 6-2 kodirnika. S pomočjo kombinatorne logike 4-2 kodirnika in 3-2 števca je bil izveden visoko učinkovit 6-2 kodirnik. Z dodatnimi poenostavitvami je bil načrtan 5-2 kodirnik pri katerem so bile močno zmanjšane latence kritičnih poti. Latence predlaganih 5-2 in 6-2 kodirnikov so enake 3.5 oziroma 4 XOR logičnim vratom, pri čemer je bila hitrost izboljšana za 15% oziroma 20%. Pri upoštevanju porabe se je izkazalo, da je predlagan kodirnik dober za hitre paralelne množilnike. Simulacije v standardnem CMOS okolju so potrdile rezultate raziskav. Rezultati pa so uporabljeni tudi za verno primerjavo nove arhitekture s prejšnjimi.

**Ključne besede:** 6-2 kodirniki; 5-2 kodirnik; množilnik; CMOS; visoka hitrost

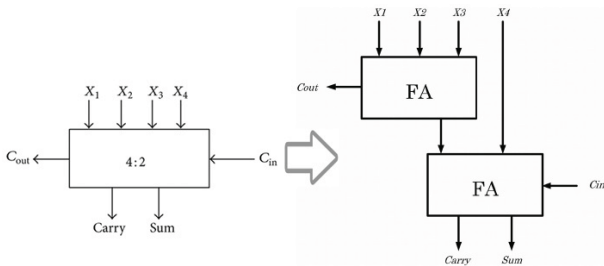
\*Corresponding Author's e-mail: [a\\_rahnamaei@iauardabil.ac.ir](mailto:a_rahnamaei@iauardabil.ac.ir)

### 1 Introduction

In 1981 a new architecture was introduced by Weinberger, which was based on the cascaded carry-save adders [1]. Getting popular as 4-2 compressor, the structure was composed of two Full Adders (FAs). One of the outputs of such structure (denoted as  $C_{out}$ ) is horizontally sent to the next sitting compressor block with a higher binary bit position value [2]. Figure 1 illustrates the explained structure in which X1 – X4 constitute the main input bits while the fifth input comes from the previous compressor with a lower binary bit value [3].

Along with the development of VLSI circuits, which provided the possibility for hardware-level realization of the parallel multipliers [4], the applications of such systems were greatly increased in Digital Signal Processors (DSPs) and microprocessors. A thorough literature review depicts that the parallel multiplier lies in the critical path for delay measurement of its former system [5]. Also, the most significant part of the propagation latency in a parallel multiplier belongs to the Partial Product Reduction Tree (PPRT) consisting of the compressors [6]. As a consequence, delay reduction for PPRT in state-of-the-art schemes is one of the main concerns for the circuit designers.

One of the effective solutions for this purpose that impressively applies to the large input bit multiplications is the utilization of high compression rate compressors such as 5-2, 6-2, and 7-2 blocks [7].



**Figure 1:** General architecture of the 4-2 compressor consisting of two cascaded FAs.

Following the general concept of the 4-2 compressor, the cascading of three FAs will result in the conventional architecture of 5-2 compressor [7]. At least a latency of 5 XOR logic gates (in gate-level) is expected for this realization where with the help of some optimizations reported in [8], the delay has been reduced to 4 XOR gates. Although there are many structures reported in the literature [8, 9, 10, 11, 12, 13, 14], none of them have been able to reach latencies less than 4 XOR gates. This partially comes down to the lack of deep consideration and investigation of the original truth table for the 5-2 compressor block.

The structure of a 6-2 compressor consists of three horizontal paths which transfer their corresponding bits to the adjacent block. Although several works have been introduced over recent years for hardware implementation of this structure [10, 15, 16, 17, 18, 19], none of them could achieve latencies less than 5 XOR logic gates.

A comprehensive study over n-2 compressor design depicts that there are some neutral states in the conventional truth table. These states can be helpful in the simplification of the Karnaugh Map (KM) for the corresponding compressor. The main objective is to obtain better speed performance while the power consumption would not be degraded. This concept is the basis of the idea in this article to design a high-performance 6-2 compressor. Furthermore, after successfully applying the mentioned idea to the 6-2 structure and by using some simplifications, a novel 5-2 compressor will be presented later in this paper. This scheme also outperforms previous works when the Power-Delay Product (PDP) is concerned.

One important issue that needs to be considered in the design of the proposed structures is the reduction of carry rippling problem between the adjacent compres-

or blocks. For instance, in the horizontally cascaded architectures of Figure 2, the conventional design principles will lead to the rippling of input signals to three compressor blocks. The same concept also holds for 6-2 compressor. However, in this paper, careful design considerations have utilized to reduce the carry rippling problem by one level. The effect of such decrement is the key factor for speed enhancement.

The organization of the paper is as follows. Section 2 explains the analysis and design of the proposed high-performance 6-2 compressor. In section 3, the novel 5-2 compressor architecture has been discussed. Post-Layout simulation results, along with the comparison tables, have been presented in section 4. Finally, section 5 contains the conclusions.

## 2 The 6-2 compressor

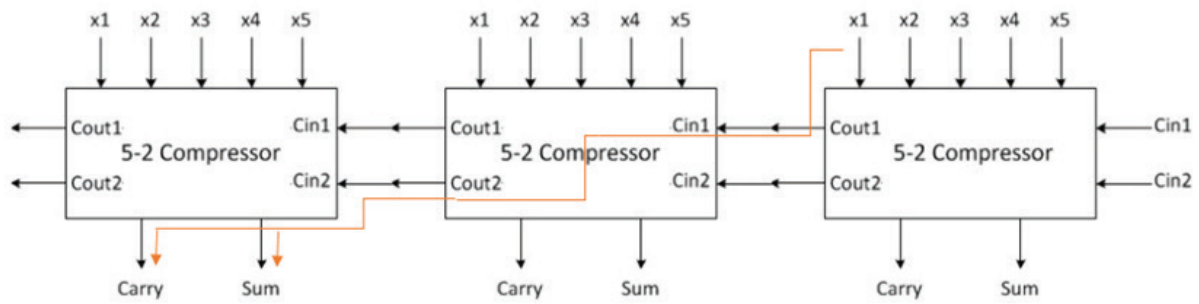
The conventional structure of a 6-2 compressor comprises two FAs along with one 4-2 compressor, as shown in Figure 3. Based on the defined architecture, a 6-2 compressor is composed of nine inputs and five outputs. The following expression describes the relationship between the input and output bits [10]:

$$I_1 + I_2 + I_3 + I_4 + I_5 + I_6 + C_{in1} + C_{in2} + C_{in3} = Sum + 2 \times (Carry + C_{out1} + C_{out2} + C_{out3}) \quad (1)$$

As Eq. (1) shows, all of the input bits along with output have the same weighting while the other four outputs will assume the next higher binary bit value. By considering the proposed architectures for 4-2 compressor reported in [2] and [3], which exhibit 2 XOR logic gate-level delay from inputs to the outputs, the latency of less than 5 XOR logic gates is expected for implementation of the 6-2 compressor in Figure 3.

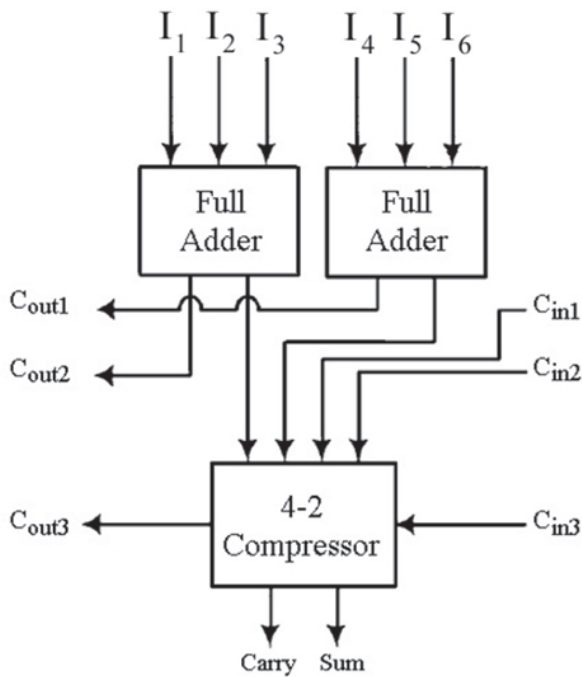
The design introduced in [10], directly uses the conventional structure for hardware realization of a 6-2 compressor. Because the 4-2 compressor of [7] was employed, the latency of the circuit was equal to 5 XOR gates. If the compressor of [3] is going to be used in that structure, again, a slight amount of gate-level reduction can be achieved for the critical path delay.

In [15] and [19], gate-level simplification has been utilized for the design of 6-2 compressor. However, the critical path delay which belongs to output is still 5 XOR gates. The architectures used in [17] and [18] have modified the conventional structure by using two 4-2 compressors and one adder. But they were not able to reduce the latency, and due to the higher transistor count, neither active area nor power consumption has been improved.



**Figure 2:** The carry rippling problem between three cascaded 5-2 compressor blocks.

By considering the aforementioned implementations and their drawbacks, in this paper, a new architecture has been proposed for the 6-2 compressor. In this realization, the gate-level delay has been reduced considerably.



**Figure 3:** Conventional structure of 6-2 compressor.

The proposed circuit is shown in Figure 4, in which the pins labeled  $I_1, I_2, I_3, I_4, I_5,$  and  $I_6,$  along with  $C_{in1}, C_{in2},$  and  $C_{in3},$  constitute the input bits. Also,  $C_{out1}, C_{out2},$  and  $C_{out3},$  along with  $Carry_{6-2}$  and  $Sum_{6-2}$  form the output bits. The operating principle of the proposed structure can be seen as a 4-2 compressor that is fed by  $I_1, I_2, I_3, I_4,$  and  $I_5$  inputs. These inputs are then utilized to generate  $C_{out1}$  and  $C_{out2}$  outputs of the 6-2 compressor. If at least two of five inputs have high-level logic value, then one of  $C_{out1}$  and  $C_{out2}$  outputs will rise to high-level voltage. If at least four input bits have the logic value of one, then both of the outputs will get the high logic value as well. By considering the conventional architecture of the 4-2

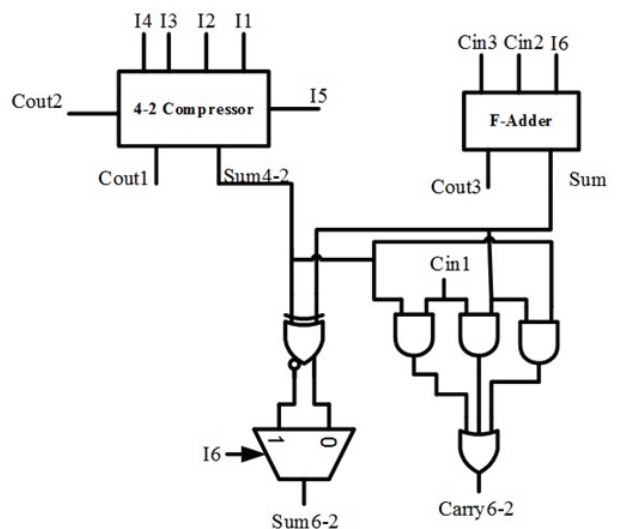
compressor described in [7], the Boolean expressions pertaining to the functions of  $C_{out1}$  and  $C_{out2}$  will be as follows:

$$C_{out1} = (I_1 \oplus I_2 \oplus I_3 \oplus I_4) \cdot I_5 + \overline{(I_1 \oplus I_2 \oplus I_3 \oplus I_4)} \cdot I_4 \quad (2)$$

$$C_{out2} = (I_1 \oplus I_2) \cdot I_3 + \overline{(I_1 \oplus I_2)} \cdot I_1 \quad (3)$$

The odd number of ones at the input pins will result in the corresponding sum output signal (denoted as  $Sum_{4-2}$ ) to get the high logic value.

For the comparison of three horizontal inputs (represented as  $C_{in1}, C_{in2},$  and  $I_6$ ), an FA has been utilized where the corresponding carry output of this stage will establish the  $C_{out3}$  output of the proposed 6-2 compressor. In order to increase the speed performance, the three gates model of FA from [12] has been employed to implement such block. This output abides by the following relation:



**Figure 4:** Proposed 6-2 compressor.

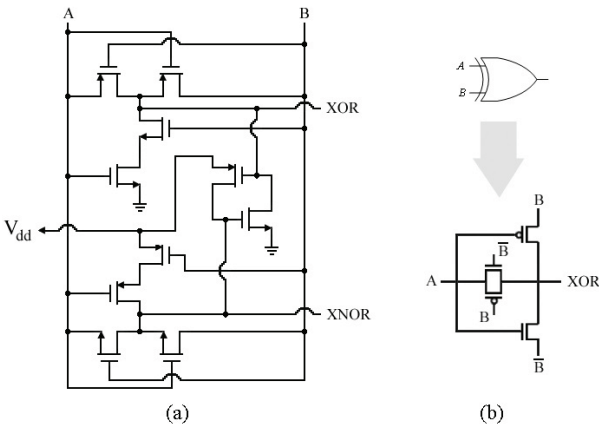
$$C_{out3} = (C_{in2} + C_{in3}) \cdot I_6 + C_{in2} \cdot C_{in3} \quad (4)$$

The combination of two sum outputs coming from 4-2 compressor and the FA block will construct the Sum output of the 6-2 compressor, which is noted as *Sum*<sub>6-2</sub>. Finally, for *Carry* output will have:

$$Carry = ((I_1 \oplus I_2 \oplus I_3 \oplus I_4 \oplus I_5) + (C_{in2} \oplus C_{in3} \oplus I_6)) \cdot C_{in1} + ((I_1 \oplus I_2 \oplus I_3 \oplus I_4 \oplus I_5) \cdot (I_6 \oplus C_{in2} \oplus C_{in3})) \quad (5)$$

The calculated Boolean expressions clearly demonstrate that the carry rippling issue has been reduced by one, which is a notable advantage of the proposed 6-2 compressor.

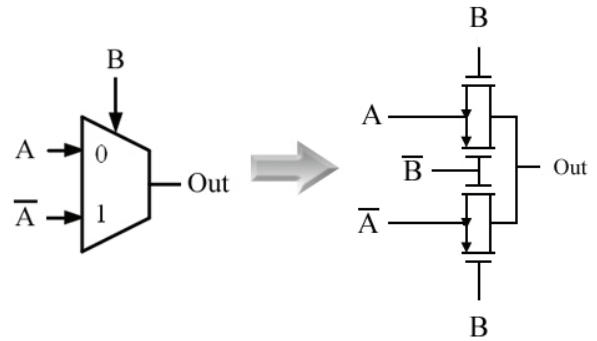
To calculate the gate-level latency, we refer to the calculations provided in [7]. As shown in Figure 5(a) and discussed in [7], the latency of two output XOR/XNOR gate is considered  $\Delta$ . As a consequence, the propagation delay of the single output XOR gate in Figure 5(b) will be equal to  $0.75 \Delta$ , considering the fact that the Transmission Gate (TG) transistors are channel-ready transistors. For a channel-ready transistor, the corresponding latency is half of a transistor where the bias signal of the gate didn't put the transistor in ON state.



**Figure 5:** The XOR gates used in the compressor circuits (a) Two output XOR-XNOR gate proposed in [7] (b) Single output XOR gate introduced in [2].

The same hypothesis also holds for the Multiplexer (MUX) gate of Figure 6, which is composed of two paralleled TGs. In the normal mode, the normalized latency of this gate will be equal to  $0.5 \Delta$ , while for the channel-ready case, the corresponding delay will be reduced to  $0.25 \Delta$ .

Furthermore, the three input OR gate can be treated almost the same as two output XOR-XNOR gate con-



**Figure 6:** Utilized MUX gate and its circuitry.

cerning the propagation latency. Also, a single pass transistor-like device will have a delay value of  $0.25 \Delta$  of the unit gate [2]. The NAND/NOR gates will also be treated the same as the MUX circuit, which is operating in the normal mode.

Therefore, according to the circuit structure in Figure 4, the critical path of the proposed 6-2 compressor will belong to *Carry* output. The start point for this path is at  $C_{out2}$  output coming from the adjacent compressor, which then enters the FA block inside the proposed present 6-2 compressor. Such a gate-level delay ( $T_d$ ) will abide by:

$$T_d = t_{Cout2} + t_{FA} + t_{AND} + t_{3OR} \quad (6)$$

in which  $t_{Cout2}$  defines the corresponding delay for the generation of  $C_{out2}$  from the previous level compressor block. Moreover,  $t_{FA}$  illustrates the time interval for the generation of output in Figure 4. The terms  $t_{AND}$  and  $t_{3OR}$  represent the latencies for AND, and three input OR gates, respectively. By considering the optimizations pertaining to the conversion of AND to NOR and OR to NAND,  $t_{AND}$  and  $t_{3OR}$  can be replaced by  $t_{NOR}$  and  $t_{3NAND}$  to reduce the gate-level latency.

Because the 4-2 compressor block reported in [3] has been utilized to achieve higher speed performance,  $t_{Cout2}$  will be equal to  $\Delta$ . On the other hand, in an FA block, two single output XOR gates are needed to produce *Sum*. Therefore,  $t_{FA}$  will be equal to  $1.5 \Delta$ . Substitution of the obtained values in Eq. (6), will result in:

$$T_d = \Delta + 1.5\Delta + 0.5\Delta + \Delta = 4\Delta \quad (7)$$

As Eq. (7) expresses, the gate-level delay of the proposed compressor is almost equal to 4 XOR logic gates, which is a substantial improvement for the delay performance of the proposed 6-2 compressor compared with the previously reported works.

### 3 The 5-2 compressor

By applying some modifications, the designed 6-2 compressor can be used as a high-speed 5-2 compressor. In order to achieve this configuration,  $Sum$ . Therefore,  $t_{FA}$  will be equal to  $1.5 \Delta$ . output should be connected to the ground. The proposed architecture has been illustrated in Figure 7.

Because one of the inputs to the FA cell has been eliminated, therefore, this block can be replaced with a Half Adder (HA), which is denoted in Figure 7 as H-Adder. Equations (8), (9), (10), and (11) present the corresponding expressions for the four output signals of this system:

$$Sum = I_1 \oplus I_2 \oplus I_3 \oplus I_4 \oplus I_5 \oplus C_{in1} \oplus C_{in2} \quad (8)$$

$$Carry = (I_1 \oplus I_2 \oplus I_3 \oplus I_4 \oplus I_5) \cdot (C_{in1} \oplus C_{in2}) + C_{in1} \cdot C_{in2} \quad (9)$$

$$C_{out1} = (I_1 \oplus I_2 \oplus I_3 \oplus I_4) \cdot I_5 + \overline{(I_1 \oplus I_2 \oplus I_3 \oplus I_4)} \cdot I_4 \quad (10)$$

$$C_{out2} = (I_1 \oplus I_2) \cdot I_3 + \overline{(I_1 \oplus I_2)} \cdot I_1 \quad (11)$$

With the help of the same definitions for propagation latency, it can easily be concluded that the delay of the critical path for the proposed 5-2 compressor will belong to the  $Carry$  signal. By starting from the  $C_{out1}$  node of the adjacent compressor, the path will end in the HA block. This can be expressed in terms of gate-level delay ( $T_d$ ), by means of the following expression:

$$T_d = t_{Cout1} + t_{HA} + t_{AND} + t'_{MUX} \quad (12)$$

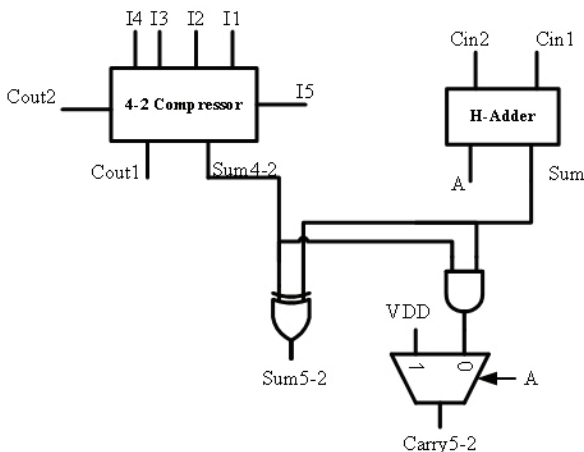


Figure 7: Proposed 5-2 compressor.

In this equation,  $t_{Cout1}$  represents the delay associated with the generation of  $C_{out1}$  from the previous compressor block, which is equal to the summation of two different terms.

Again, by considering the 4-2 compressor architecture of [3], the first term will belong to a two output XOR-XNOR gate. The second term will pertain to the latency of two cascaded MUX gates with channel-ready transistors. As a consequence,  $t_{Cout1}$  will be equal to  $1.5\Delta$ .

For a HA block, the propagation latency denoted by  $t_{HA}$  will be equal to that of a single output XOR gate ( $0.75\Delta$ ). But for the AND gate, the combination of a NAND and inverter gate is needed, which makes the corresponding delay of this gate ( $t_{AND}$ ) be equal to  $\Delta$ . Finally,  $t'_{MUX}$  represents the propagation latency of a channel-ready MUX, which is equal to  $0.25\Delta$ . The sum of these latencies will result in the following value:

$$T_d = 1.5\Delta + 0.75\Delta + \Delta + 0.25\Delta = 3.25\Delta \quad (13)$$

As Eq. (13) expresses, the gate-level delay of the designed compressor is almost 3.5 XOR logic gates, which is a notable improvement for the speed performance of this block.

### 4 Simulation results

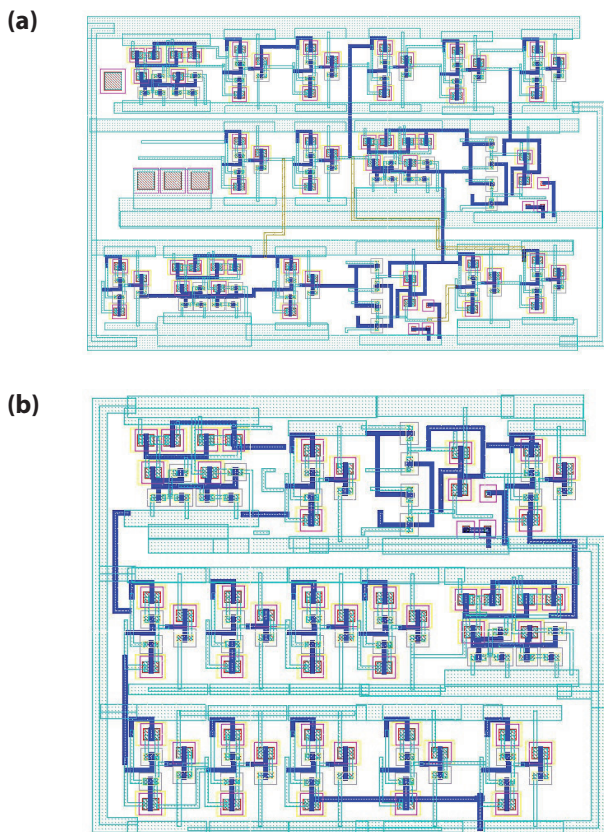
In order to perform a thorough analysis and comparison for the simulation results of the works, which are discussed in this paper, at the first step, the layouts of the designed circuits have been drawn, and their parasitics have been extracted. After that, some of the recently reported structures in the literature for 6-2 and 5-2 compressors with remarkable results and improvements have been selected and redesigned here using the similar gates employed for this work.

Figure 8 illustrates the layout schemes for the proposed architectures. In Figure 8(a), the layout of the 6-2 compressor has been shown, which occupies an active area of  $55 \times 35 \text{mm}^2$ . For the implemented 5-2 compressor, as demonstrated in Figure 8(b), an active area of  $35 \times 30 \text{mm}^2$  is needed.

In order to resemble the practical situation in the simulation setup, each of the inputs is driven by a buffer circuit. Every output has been passed through a buffer block as well to be able to drive the next stage without loading effect on the compressor circuit. In addition, the compressor blocks are used in a parallel fashion to cover the critical path, as shown in Figure 9.



It must be mentioned that the configuration of Figure 9 is used for the case in which the propagation delay between two adjacent compressor structures finishes in the second compressor block. If the propagation delay is rippled for three horizontally cascaded compressors, then three compressors must be considered in the simulation environment. This fact has been presumed for the architectures reported in [9], [10], [12], [13], [14], [18] and [19] (similar as Figure 2).

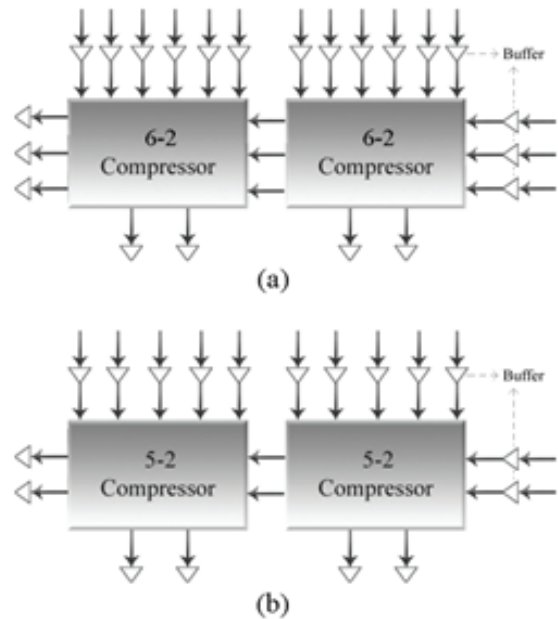


**Figure 8:** Layouts of the proposed architectures (a) 6-2 compressor (b) 5-2 compressor.

Meanwhile, in the simulation environment, the propagation delay has been measured from the point that the earliest input transition reaches 50% of  $V_{dd}$  to the point where the latest output signal rises to 50% of the  $V_{dd}$  voltage. [7]. The worst-case, which demonstrates the longest latency from inputs to the outputs (considering the signal propagation between the adjacent blocks), shows the delay of the critical path.

*4.1 The 6-2 compressor*

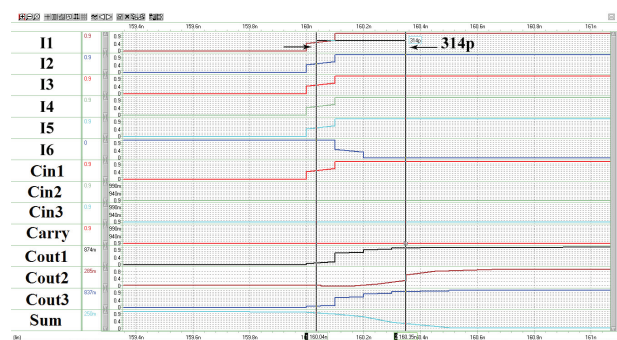
Post-layout simulations using HSPICE for TSMC standard 90nm CMOS technology along with 0.9V power supply have been carried out to measure the delay, and power consumption of the proposed 6-2 compressor and the works reported in [10], [18] and [19] which are



**Figure 9:** Simulation setup for (a) 6-2 compressor (b) 5-2 compressor considering the propagation delay for two stages.

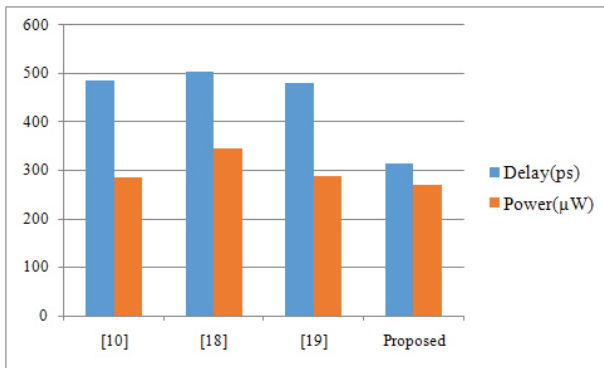
redesigned and optimized here to make a fair comparison.

Figure 10 illustrates the results for the correct functionality of the proposed architecture along with delay measurements. The results demonstrate the delay of 314ps for the critical path of the proposed circuit.



**Figure 10:** Simulation results for correct functionality and delay measurement of the proposed 6-2 compressor.

The result of the comparison for the power-delay measurement of the designed structure and the selected works is shown in Figure 11. The results indicate that the lowest PDP value belongs to the proposed architecture. The design reported in [19], which has a delay value of about 481ps will need 53% more time to produce the output compared to the designed scheme.



**Figure 11:** Power-Delay comparison of the proposed work and redesigned 6-2 compressors based on the TSMC 90nm CMOS process.

Also, the measurement results for the power dissipation at the operating frequency of 100MHz demonstrate that the proposed compressor circuit has the lowest value of power consumption, while the design reported in [10] which shows the lowest power consumption among the competitors, consumes 6% more power compared to the proposed circuit.

Table 1 illustrates the comparison between the redesigned 6-2 configurations based on their circuitry and simulation results obtained by the author.

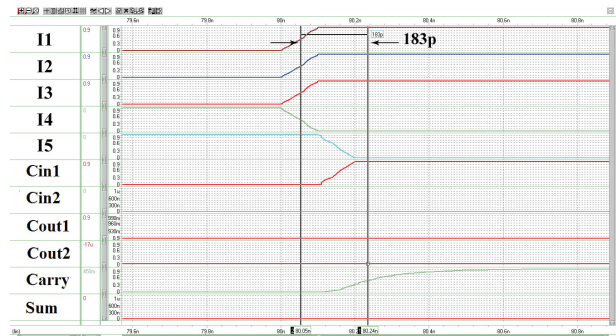
**Table 1:** Comparison of Proposed 6-2 Compressor and Other Structures.

Work	Proposed	[10]	[18]	[19]
Technology (nm)	90	90	90	90
Transistor Count	125	140	152	142
Gate Level Delay (XOR)	4 gates	5 gates	6 gates	5 gates
Power (μW) @100MHz	269	285	345	289
Delay(ps)	314	487	505	481
PDP (pJ)	0.084	0.139	0.174	0.139

#### 4.2 The 5-2 compressor

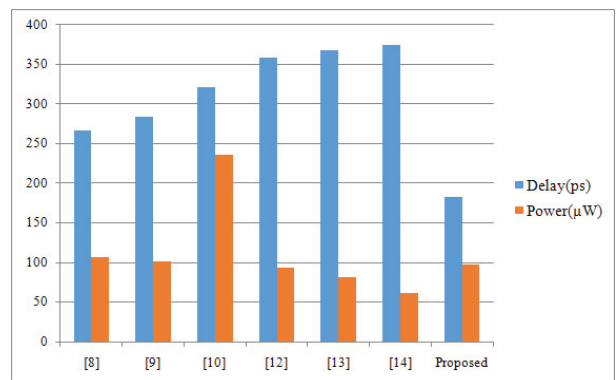
As described for 6-2 compressor, post-layout simulations using HSPICE for TSMC standard 90nm CMOS technology along with 0.9V power supply have been carried out to measure the delay and power consumption of the proposed 5-2 compressor and redesigned architectures reported in [8], [9], [10], [12], [13], and [14].

Figure 12 illustrates the results for the correct functionality of the proposed structure along with the delay measurement, which depicts the value of 183ps for the delay of the critical path.



**Figure 12:** Simulation results for correct functionality and delay measurement of the proposed 5-2 compressor.

The result of the comparison for the power-delay measurement of the proposed design and the redesigned works is shown in Figure 13. The results indicate that the lowest delay value belongs to the designed scheme. Also, the measurement result and comparison for power dissipation at the operating frequency of 100MHz demonstrates that the power consumption of the proposed design is about 97μW, which is not the lowest among the presented works. The designs reported in [13] and [14] have the lowest power consumption. However, the lowest PDP belongs to the proposed scheme.



**Figure 13:** Power-Delay comparison of the proposed work and redesigned 5-2 compressors based on the TSMC 90nm CMOS process.

Finally, Table 2 summarizes the comparison between the redesigned 5-2 structures based on their circuitry and simulation results obtained by the author.

## 5 Conclusions

In this article, a novel 6-2 compressor was introduced, which outperforms the previous designs from the viewpoint of the propagation delay for the critical path. The proposed architecture is based on the combinational

**Table 2:** Comparison of Proposed 5-2 Compressor and Other Structures.

Work	Proposed	[8]	[9]	[10]	[12]	[13]	[14]
Technology (nm)	90	90	90	90	90	90	90
Transistor Count	97	112	112	135	90	82	58
Gate Level Delay (XOR)	3.5 gates	4 gates	5 gates	5.5 gates	6 gates	6 gates	6 gates
Power ( $\mu$ W) @100MHz	97	107	101	236	94	81	61
Delay(ps)	183	247	284	321	359	368	375
PDP (pJ)	0.0177	0.0286	0.0287	0.0757	0.0337	0.0298	0.0229

circuit consisting of a 4-2 compressor and FA, which has resulted in a 20% speed improvement in comparison with the other works reported in this criterion. The design approach for the proposed compressor was able to reduce the number of transistors used in the circuit. This is another advantage of the presented circuit, which will occupy a small area on the chip while the carry rippling problem has been reduced by one level.

With some extra modifications, the proposed 6-2 compressor can be used as a 5-2 compressor. In this case, the latency of the critical path has also been reduced significantly. The gate-level delay of the proposed 5-2 and 6-2 compressors is equal to 3.5 and 4 XOR logic gates, respectively, which demonstrate a 15% speed enhancement for the proposed 5-2 architecture compared with the best-reported works. The aforementioned advantages illustrate the capability of the implemented circuits for utilization in high compression multiplication systems.

Simulation results of the proposed circuits using HSPICE for TSMC 90nm standard CMOS technology and 0.9V power supply represent the delay value of 314ps and 183ps for the proposed 6-2 and 5-2 compressors, respectively. The power dissipation is also 269 $\mu$ W and 97 $\mu$ W for these structures at the operating frequency of 100MHz.

## 6 Conflict of Interest

The author declares no conflict of interest.

The author declares that there is no funding support for this work.

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