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Analog / Radio-Frequency Performance Analysis of Nanometer Negative Capacitance Fully Depleted Silicon-On-Insulator Transistors

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Abstract: The negative capacitance field-effect transistor can break the limitation of the Boltzmann tyranny. In this study, the analog and radio-frequency (RF) performance of a nanometer negative-capacitance fully depleted silicon-on-insulator (NC-FDSOI) transistor is investigated. The analog/RF parameters of the NC-FDSOI device are compared with the conventional FDSOI counterparts for transconductance, output conductance, gate capacitance, cutoff frequency, and maximum oscillation frequency. In addition, the effect of ferroelectric thickness on the analog/RF performance of NC-FDSOI device is analyzed and discussed. The results show that even when operated at low voltages, NC-FDSOI transistors enable analog/RF performance improvement in traditional FDSOI counterparts at low power in the case of a suitable ferroelectric thickness.

Keywords: negative capacitance effect; NC-FDSOI transistor; analog / RF Performance; ferroelectric capacitance

Analogna in radio frekvenčna analiza učinkovitosti nanometrskega polno osiromašenega silicijevega tran-zistorja na izolatorju z negativno kapacitivnostjo

Izvleček: Poljski tranzistor z negativno kapacitivnostjo lahko premaga oviro Boltzmannove tiranije. V članku je raziskan analogna in radio frekvenčna učinkovitost nanometrskega polno osiromašenega silicijevega tranzistorja na izolatorju z negativno kapacitivnostjo (NC-FDSOI). Analogni/RF parametri NC_FDSOI elementa, kot so: transkonduktanca, izhodna konduktanca, kapacitivnost vrat, frekvenca odklopa in največja frekvenca osciliranja, so primerjani s klasičnim FDSOI. Dodatno je analiziran vpliv feroelektrične debeline NC-FDSOI elementa. Rezultati kažejo boljšo učinkovitost NC-FDSOI tranzistorjev tudi pri nizki napajalni napetosti in ustrezni feroelektrični debelini.

Ključne besede: efekt negativne kapacitivnosti; NC-FDSOI tranzistor; analogna / RF učinkovitost; feroelektrična kapacitivnost

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1 Introduction

In the past decade, complementary metal-oxide-semiconductor (CMOS) transistors have experienced unprecedented development, shrinking device sizes, and advances in integrated device design and fabrication, bringing the CMOS technology into the nanometer era. However, continued miniaturization has also brought about various new constraints, such as high-power consumption caused by chip overheating [1]. To solve these problems, steep switching characteristics and lower operating voltage can be achieved by lowering the sub-threshold slope (SS). NCFETs based on ferroelectric on a gate stack have attracted significant attention in the field of advanced CMOS devices due to their lower SS (<60 mV/decade) [2]-[8]. Recently, NCFETs have proven to be suitable for a variety of low-

power applications, such as wearables, bioelectronics, and the Internet of Things [9]-[12]. Furthermore, with the advent of the 5G era in radio-frequency (RF) applications, the analog/RF performance of NCFETs must be tested. FDSOI technology is popular because it better overcomes short channel effects and is significantly less expensive to manufacture than fin field effect transistors (FinFETs). In previous studies, FDSOI transistors showed good analog/RF performance [13, 14]. However, the relationship between the negative capacitance effect and analog/RF performance parameters for FDSOI devices is still not understood. Therefore, in this work, we address this deficiency by simulating analog/RF performance of 20-nm NC-FDSOI transistors with different ferroelectric thicknesses (T_{fe}) utilizing a computer-aided-design (TCAD) tool.

2 Materials and methods

At present, most negative-capacitance transistors are implemented by adding ferroelectric materials [15]-[20]. There are two main types of structures used in the negative capacitance transistors: metal-ferroelectric-metal insulator-semiconductor (MFMIS) and metal-ferroelectric insulator-semiconductor (MFIS). Owing to the better performance of the MFMIS NCFET in terms of it being hysteresis-free [21], a NCFET with MFMIS structure is used in this work. Then, the TCAD tool is used to add a ferroelectric capacitor to the gate on the underlying conventional FDSOI to form an NC-FDSOI transistor. The structure of the FDSOI and NC-FDSOI transistor are shown in Fig. 1.The gate of NC-FDSOI used an HfO2 based ferroelectric with coercive field, Ec = 1 MV/cm and remnant polarization, Pr = 5 μC/cm2. For better compatibility with the CMOS process[22], a smaller ferroelectric thickness is chosen (T_{fe} = 1, 2, 3, and 4 nm).

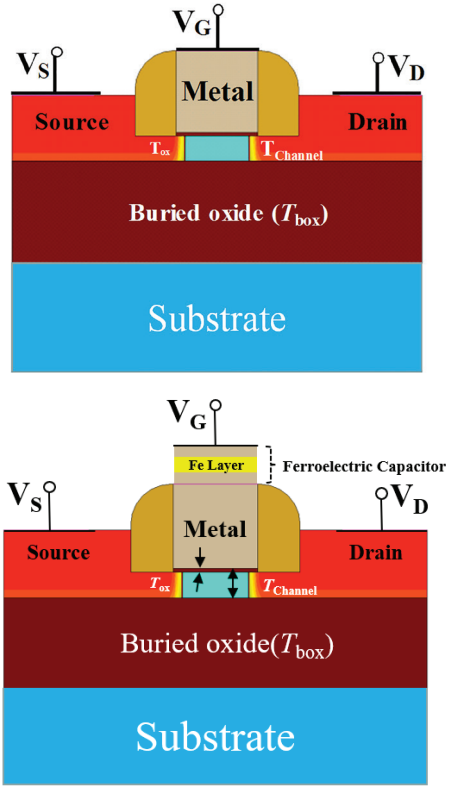


Figure. 1: FDSOI and NC-FDSOI device structure.

The device parameters used for numerical simulation are summarized in Table 1.The TCAD mixed-mode device simulator is used to simulate the NC-FDSOI and FDSOI transistors [23], and the frequency characteristics of the NCFDSOI and FDSOI are discussed by AC small-signal analysis. The simulation uses a variety of physical models, such as Fermi statistics, doping-dependent mobility, high-field saturation, mobility degradation at interfaces, Shockley-Read-Hall recombination, and density-gradient quantization. The Poisson and Landau-Khalatnikov equations are solved self-consistently by the TCAD tool [24, 25]. The LK equation, which relates the polarization (P) and electric field (E), is given in Eq. (1) [26, 27]:

$$E = 2\alpha P + 4\beta P^3 + 6\gamma P^5 + \rho \frac{dP}{dt} \quad (1)$$

where α, β, γ, and ρ are ferroelectric material parameters and P is the polarization strength. In this work, RF performance parameters are extracted from the two-port network.

Table 1: device structural parameters

Parameter	FDSOI	NC-FDSOI
Channel Length(L_g)	20nm	20nm
Spacer Length(L_{sp})	10nm	10nm
Channel Doping(N_d)	$10^{14}cm^3$	$10^{14}cm^3$
Channel Thickness($T_{channel}$)	5nm	5nm
Oxide Thickness(T_{ox})	0.9nm	0.9nm
Work-founction(Φ_m)	4.52	4.52
ferroelectric thickness (T_{fe})	0	1,2,3,4nm
Coercive Field(E_c)	0	$1MV/cm^3$

3 Results and discussion

Fig. 2(a) and (b) shows the transfer characteristics of drain current (I_{ds}) versus gate voltage (V_{gs}) for a conventional FDSOI and NC-FDSOI fixed at drain voltages (V_{ds}) of 0.7 and 0.05 V. It can be seen that the current of the NC-FDSOI is always greater than that of the FDSOI, and the SS is lower, whether it is working in a linear or saturated region. The results show that the current-amplifi-

cation capability of the NC-FDOI is significantly stronger than that of the conventional FDSOI (~60% addition, T_{fe}=3 nm) at V_{ds} =0.7 V. When the thickness of the ferroelectric (T_{fe}) of the NC-FDSOI is set to 6 nm, SS=43 mV/decade breaks the limit of the SS for the transistor at room temperature, where SS is extracted from Eq. (2):

$$SS = \frac{1000}{\frac{d}{dV_{gs}} \log_{10} I_{ds}} \quad (2)$$

As the SS decreases, the ratio of on- and off-state currents (I_{on}/I_{off}) increases compared to the FDSOI, which indicates that the NC-FDSOI is more suitable for high-speed switching applications than the conventional FDSOI. Experiments under actual environmental measurements also show that NC-FDOSI has good current amplification capability and low SS, which the SS is reduced from 78 mV/decade to 73 mV/decade, and the drain current is increased from 4 μA to 7 μA [28]. Fig. 2(c) and (d) shows the output characteristics of I_{ds} versus V_{ds} for their fixed values at V_{gs}=0.7 and 0.4 V. As shown in Fig. 2(c) and (d), the ferroelectric has an enhanced effect on the output characteristics of the device, whether at high or low V_{gs}. However, at low V_{gs}, the internal gate voltage (V_{in}) is lowered due to the influence of the ferroelectric, and the negative differential resistance (NDR) effect is generated [29].

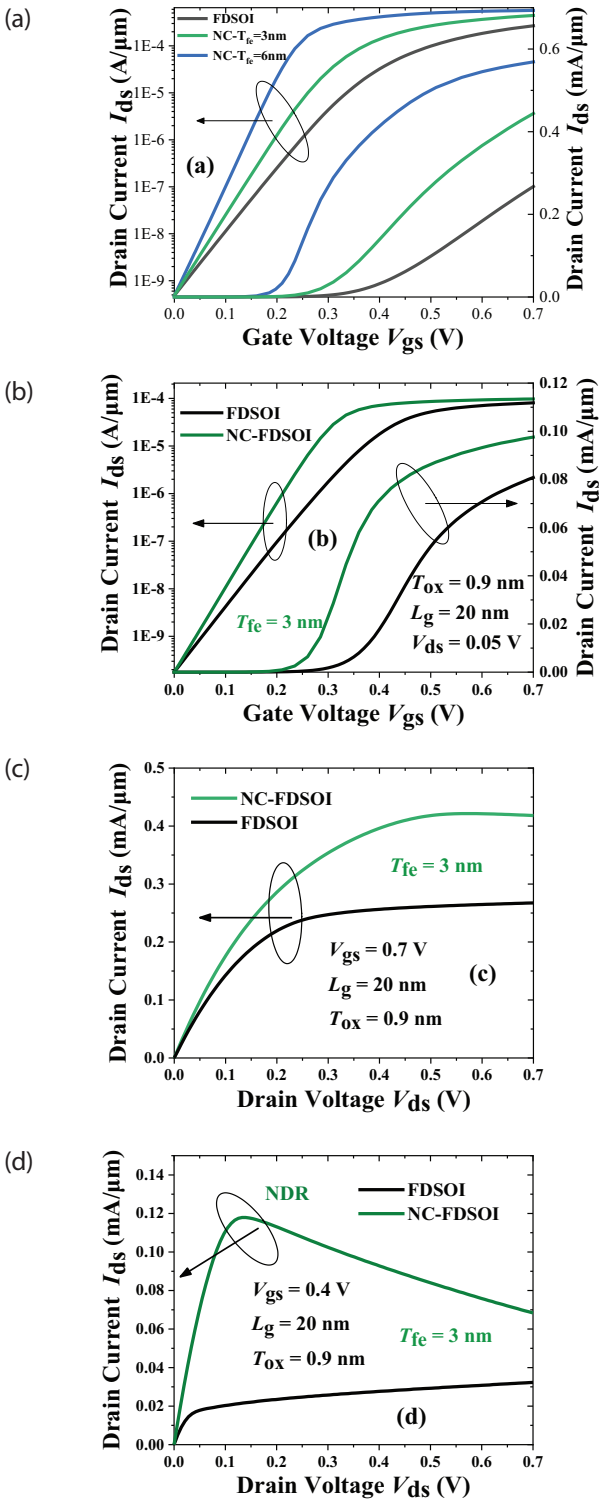


Figure 2: (a) I_{ds} with V_{gs} for FDSOI and NC-FDSOI at V_{ds}=0.7 V. (b) I_{ds} with V_{gs} for FDSOI and NC-FDSOI at V_{ds} =0.05 V. (c) I_{ds} with V_{ds} for FDSOI and NC-FDSOI at V_{gs} =0.7 V. (d) I_{ds} with V_{ds} for FDSOI and NC-FDSOI at V_{gs} =0.4 V.

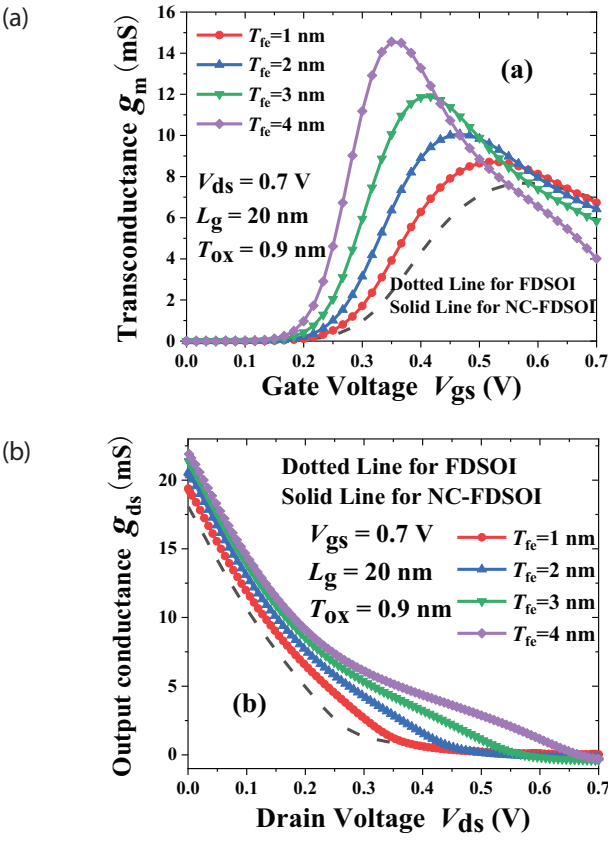
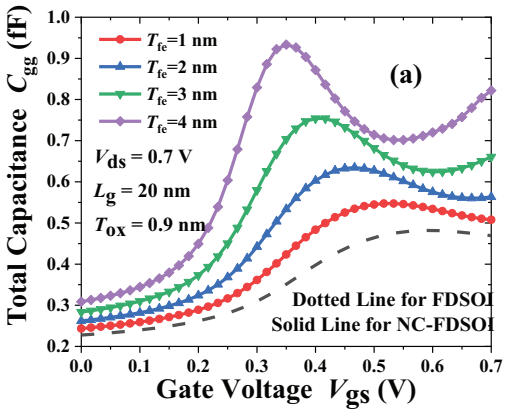


Figure. 3: (a) Transconductance (g_m) with V_{gs} for FDSOI and NC-FDSOI. (b) output conductance (g_{ds}) with V_{ds} for FDSOI and NC-FDSOI.

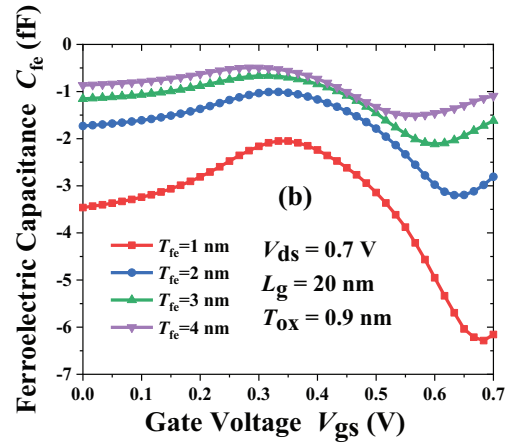
Fig. 3(a) shows transconductance (g_m) with V_{gs} at V_{ds} = 0.7 V and the output conductance (g_{ds}) as a function of V_{ds} fixed at V_{gs} = 0.7 V, where g_m determines the device's gain. The g_m and g_{ds} values for both the devices are obtained by Eqs. (3) and (4), respectively:

$$g_m = \frac{\partial I_{ds}}{\partial V_{gs}} \tag{3}$$

(a)



(b)



(c)

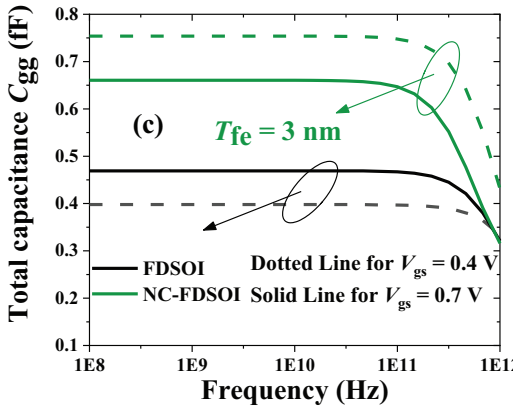


Figure. 4: (a) gate capacitance (C_{gg}) with V_{gs} for FDSOI and NC-FDSOI. (b) ferroelectric capacitance (C_{fe}) with V_{gs} for NC-FDSOI. (c) gate capacitance (C_{gg}) with frequency for FDSOI and NC-FDSOI.

$$g_{ds} = \frac{\partial I_{ds}}{\partial V_{ds}} \tag{4}$$

It can be clearly seen from Fig. 3(a) and (b) that the g_m and g_{ds} values of the NC-FDSOI are much larger than those of the FDSOI device, and the g_m and g_{ds} values of the NC-FDSOI are further increased as the thickness of the ferroelectric increases. As the current gain decreases, g_m will gradually decrease after reaching the peak, but overall it will be larger than that of the FDSOI. This indicates that the NC-FDSOI transistor gain increases as T_{fe} increases within a certain range due to the negative-capacitance effect. The high transconductance makes the NC-FDSOI suitable for high-gain amplifier applications.

Fig. 4(a) and (b) shows the total gate capacitance (C_{gg}) and ferroelectric capacitance (C_{fe}) of the NC-FDSOI with V_{gs} at different ferroelectric thicknesses (T_{fe} = 1, 2, 3, and 4 nm). Simply lowering the threshold voltage (V_{th}) and lowering SS is not enough to improve circuit performance. The important device parameters that affect performance specifications, such as power dissipation and intrinsic delay, are the total gate capacitance [30]. Therefore, it is necessary to analyze the impact of the ferroelectric thickness in the gate stack on C_{gg}. As shown in Fig. 4(a), as the thickness of the ferroelectric increases, the gate capacitance increases compared with the FDSOI total capacitance (C_{mos}). As shown in Fig. 4(b), this is mainly due to the decrease in the absolute value of the ferroelectric capacitance (C_{fe}). Fig. 4(c) shows the variation of C_{gg} with frequency at V_{gs} = 0.4 and 0.7 V. In Fig. 4(c), C_{gg} begins to decrease after approximately100 GHz, and the C_{gg} of NC-FDSOI is larger at V_{gs} =0.4 V. This result is consistent with that shown in Fig. 4(a).

In Fig. 5(a) and (b), the cutoff frequency (f_T) and maximum oscillation frequency (f_{max}) with V_{gs} at V_{ds} = 0.7 V, where f_T is extracted from current gain (h21) through an extrapolation of a 20-dB/decade slope, and f_{max} is extracted from Mason's unilateral gain through an extrapolation of a 20-dB/decade slope. It can be seen from Fig. 5(a) that the maximum f_T of the NC-FDSOI is the same as that of the conventional FDSOI. However, with the increase of V_{gs}, the NC-FDSOI leads to f_T achieving peaks at lower V_{gs} due to the increase of ferroelectric thicknesses compared to the baseline FDSOI (T_{fe} = 0) [26]. As is known from Eq. (5), this is because both g_m and C_{gg} peak at a lower V_{gs}, which is caused by a decrease in V_{th} as Tfe increases [31]. It can be seen from Eq. (6) that f_{max} is mainly affected by f_T and gate resistance (R_g), so f_{max} in Fig. 5(b) is the same as the f_T trend and peaks at a lower gate voltage. Under the influence of g_m reduction, f_T and f_{max} gradually decrease after reaching

the peak value and are lower than that of the FDSOI at high gate voltage, and the RF performance of the circuit will deteriorate at high gate voltage. Therefore, the NC-FDSOI performs better at low bias voltages:

$$f_T = \frac{g_m}{2\pi C_{gg}} \tag{5}$$

$$f_{\max} = \frac{f_T}{\sqrt{4R_g\left(g_{ds} + 2\pi f_T C_{gd}\right)}} \tag{6}$$

(a)

(b)

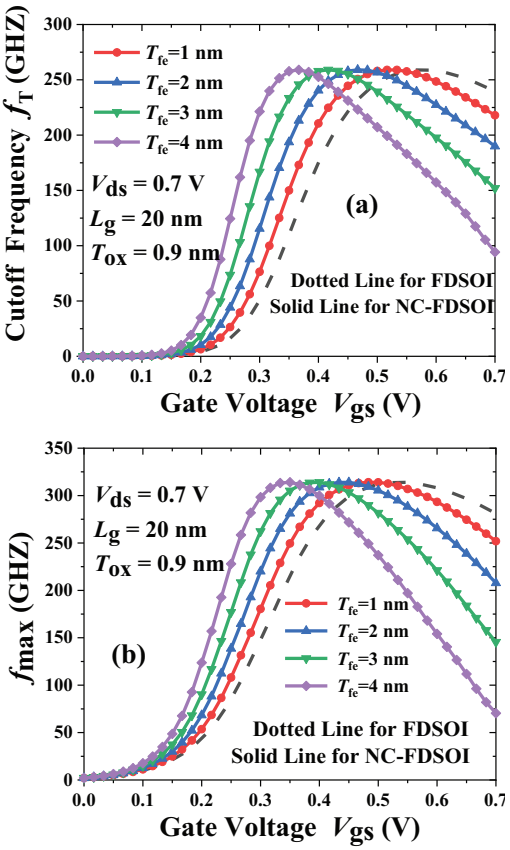


Figure. 5: (a) cutoff frequency (f_T) with V_{gs} for FDSOI and NC-FDSOI.(b) maximum oscillation frequency (f_{max}) with V_{gs} for FDSOI and NC-FDSOI.

4 Conclusions

In this work, a comparison of analog/RF performance between NC-FDSOI and FDSOI transistors is demonstrated, and the effects of ferroelectric thickness on the analog/RF parameters of the NC-FDSOI are analyzed. The f_{max} was measured for the first time, and through a one-to-one comparison with FDSOI, the high frequency dependence of the C_{gg} and the V_{ds} dependence of the g_{ds} were achieved for the first time.The results show that the NC-FDSOI is superior to the conventional FDSOI in terms of SS, g_m, and g_{ds}, and the effect is more significant with the increasing thickness of the ferroelectric. After the addition of the ferroelectric negative capacitance, the f_T and f_{max} values of the NC-FDSOI also peak at a low bias voltage. Therefore, in the case of a suitable T_{fe}, the NC-FDSOI can not only outperform the conventional FDSOI in terms of digital circuits but also achieve better analog/RF performance compared to the FDSOI with reduced power consumption.In the future we will also study the effects of different ferroelectric parameters on analog/RF performance.

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6 Conflict of Interest

The authors declare no conflict of interest. The founding sponsors had no role in the design of the study; in the collection, analyses, or interpretation of data; in the writing of the manuscript, and in the decision to publish the results.

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