

Low-Kickback-Noise Preamplifier-Latched Comparators Designed for High-Speed & Accurate ADCs

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Abstract: High-resolution high-speed comparators are one of the main cores in the implementation of the high-performance systems, such as ADCs. Two comparators are presented in this paper where both of the structures are suitable for high-speed, low-noise and accurate applications. The comparators are designed, based on the positive feedback structure of two back-to-back inverters. An improved rail-to-rail folded cascode amplifier with an active bias circuit is utilized for the first architecture, in which the structure of the comparator is rearranged appropriate to the running comparison phase. Distinguished by its novel data reception style, a new comparator is proposed in the next circuit. In this structure, the hot n-well concept is considered for the PMOS transistors of the positive feedback latch. Applying the inputs to the bulks of the mentioned PMOS devices, isolates the regenerative outputs from the input signals; hence, a sizable attenuation in the kickback noise value is resulted. Merging the reset, evaluation and latch sequences makes it possible to decrease the comparison duration. Both of the proposed comparators of this paper benefits from this excellence, therefore an intensive increase is observed in their comparison speed. In order to confirm the performance accuracy of the circuits in various terms, multiple simulations are performed in all process corners, using HSPICE (level49) with a standard 0.35 μm CMOS process and the power supply of 3.3V. VDD noise of 300mVp-p and alterations in temperature are also included in the simulation conditions. The simulation results confirm recognition of a differential input with 2mV pick-to-pick amplitude at as high a clock frequency as 800MHz with power consumption about 2.6mW for the first circuit and a 1mV differential input with update rate of 1GHz and power consumption about 1.6mW for the low-noise structure of the second comparator. According to the layout pattern, an active area of 55 μm \times 13 μm and 24 μm \times 15 μm is occupied by the improved folded cascode comparator and the proposed novel structure respectively.

Keywords: High Speed Comparator, Kickback Noise, High Speed ADC, High Resolution Comparator.

Visokozmogljiva primerjalnika z nizkim povratnim vplivom na osnovi topologije predojačevalnik-zapah za hitre in natančne analogno-digitalne pretvornike (ADC)

Izveček: Visokoločljivi in hitri primerjalniki so osnova za izvedbo visokozmogljivih sistemov, kot so analogno-digitalni pretvorniki (ADC). V prispevku sta predstavljena dva primerjalnika, katerih struktura je primerna za hitre, nizkošumne in natančne aplikacije. Primerjalnika sta zasnovana na osnovi dveh povratno vezanih negatorjev. Pri prvem primerjalniku je uporabljen kaskodni ojačevalnik, pri katerem je struktura primerjalnika preurejena glede na tekočo fazo primerjanja. Pri drugem primerjalniku so vhodni signali priključeni na substrat tranzistorja prek diferencialnih tranzistorjskih parov. S tem smo zmanjšali vpliv izhoda vezja in vrednost povratnega šuma. Predlagana vezja smo načrtali v 0.35 μm tehnologiji CMOS z napajalno napetostjo 3.3 V in, v postopku simulacije, preverili z uporabo programa HSPICE. Pri tem smo preverili vpliv napetostnih motenj v napajanju in spremembe temperature na delovanje primerjalnikov. Rezultati simulacij potrjujejo zaznavo diferencialne napetosti amplitude 2 mV pri frekvenci ure 800 MHz in porabo moči 2.6 mW za prvi primerjalnik in zaznavo diferencialne napetosti amplitude 1 mV pri frekvenci ure 1 GHz in porabo moči 1.6 mW za drugi primerjalnik. Površina vezja, ki jo zasedata primerjalnika, je 55 μm \times 13 μm in 24 μm \times 15 μm .

Ključne besede: hitri primerjalnik, povratni šum, hitri analogno-digitalni pretvornik, visokoločljivi primerjalnik

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1 Introduction

Although most of the parameters obtained from the nature by different sensors are analog by default, an analog to digital conversion process is required due to the vast improvements in the digital signal processing field. CMOS high-speed analog-to-digital converters (ADCs) are one of the best suited blocks for this purpose where some bottlenecks have to be solved. Precisely comparison of the analog input signal with a reference value and extracting the digital output bit is a great challenge and seems to be the main bottleneck of the process; hence, a high-speed, high-resolution and low-power comparator is needed to keep the overall performance of the system in an acceptable level. The input voltage of the comparators changes continuously which leads to some variations in their outputs at the input clock edges. Based on the comparison, the comparator outputs a High or Low signal.

Depending on their nature, functionality and inputs, comparators are classified into different types such as voltage or current comparators, continuous or discrete time comparators and so on. By another classification, there are two different kinds of comparators: single-stage and multi-stage comparators, [2]. Studying these two kinds, it can be understood that the multi-stage comparators have more power consumption, delay time and die size; however the single-stage ones usually have complicated switches which are required to be controlled accurately via additional controlling signals, [1,2]. Variety of the timing signals might increase the digital coupled noise to the analog section, also generation of these controlling signals requires some extra hardware which again increases the die size and the power consumption of the system. Multi-stage comparators are usually made up of three main stages; pre-amplifier, decision circuit (positive feedback or gain stage) and post-amplifier. The pre-amp stage amplifies the input signal to improve the comparison sensitivity through increasing the minimum detectable input signal by which the comparator can make correct decisions. Meanwhile, it isolates the input of the comparator from the switching noise which is produced by the positive feedback stage like the clock feed through and the kickback noise effect. The gain stage is used to determine which of the input signals is larger and the output buffer amplifies this information and produces a full-range digital data. In the single stage comparators, the three important phases of the comparison, reset, evaluation and latch, are performed via a single block. During the reset phase, the previous data stored in the parasitic capacitors is usually removed using a reset switch that connects the differential output nodes to each other. The second phase is evaluation in which the comparator begins to compare two inputs and de-

termines whether the outputs should be high or low. In the latch phase, the evaluated outputs are separated up to the digital levels. Each of these phases need a certain timeframe, hence it can be concluded that the conversion speed is limited by the decision-making duration of the comparator.

CMOS process variation is the main origin of the offset voltage introduced to the latched comparators, which extremely restricts their comparison accuracy. Coupling a pre-amplifier stage before the output latch attenuates the input-referred offset voltage of the comparator, thus an accurate preamplifier-latch topology is engendered, [6-8], making it possible to utilize the comparator for high-resolution purposes.

Based on the folded cascode structure, a high-speed high-accuracy comparator with preamplifier-latch topology is improved for high-resolution applications. Moreover, another comparator is proposed in which a novel method is utilized for obtaining a high-resolution latched structure. Taking advantage of this circuit, both high speed and high accuracy beside low die size and lessened power consumption is achieved. Rest of the paper is organized in 6 sections. In the next section latched comparators are discussed, the improved folded cascode structure is presented in Section 3, the proposed new comparator circuit is detailed in Section 4, a new readout circuit is presented in Section 5, Section 6 verifies the simulation results, and the final section delivers the conclusion and the comparisons with similar works.

2 Latched Comparators

The threshold voltage of an inverter (V_{th}) is a boundary voltage that determines whether the value of the received signal is High or Low. As depicted in Fig. 1, this voltage is arisen from shorting the input and the output of an inverter. Value of the V_{th} depends on the threshold voltages of NMOS and PMOS transistors (V_{thn} and V_{thp} , respectively).

Threshold voltage for an inverter can be calculated according to (1) and (2).

$$I_{dp} = I_{dn} \quad (1)$$

$$\begin{aligned} \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L} \right)_n (V_{th} - V_{thn})^2 (1 + \lambda V_{th}) &= \\ = \frac{1}{2} \mu_p C_{ox} \left(\frac{W}{L} \right)_p (V_{dd} - V_{th} - V_{thp})^2 (1 + \lambda [V_{dd} - V_{th}]) & \end{aligned} \quad (2)$$

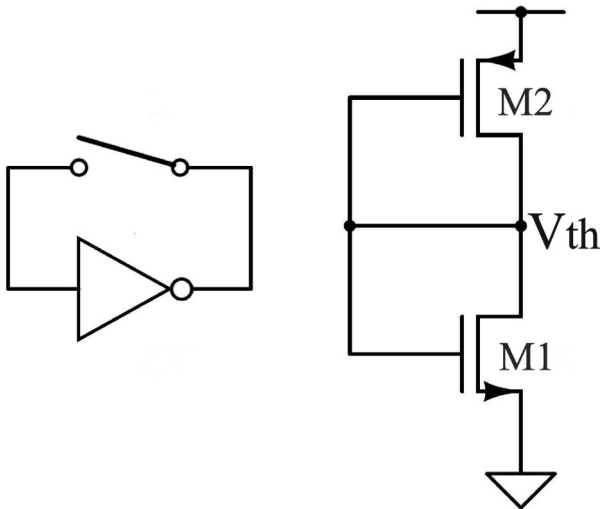


Figure 1: A CMOS Inverter with its Shortened Input and Output.

Ignoring the channel length modulation effect and applying the device sizes as $\mu_n (W/L)_n = \mu_p (W/L)_p$, (3) is obtained:

$$V_{th} = \frac{(V_{dd} + V_{thn} - |V_{thp}|)}{2} \quad (3)$$

As it's clear, the value of V_{th} depends on V_{thn} and V_{thp} so it is affected by the process variations, thus its value varies in different process corners. In TT, SS and FF corners V_{thn} is close to V_{thp} in value, so $V_{th} \approx V_{dd} / 2$ but due to inequality in the conductance of NMOS and PMOS devices, in FS and SF corners V_{th} is respectively a little bit greater or lower than $V_{dd} / 2$.

Fig. 2 illustrates two back-to-back inverters besides a reset switch. Variant fabrication process and asymmetrical doping generate two unequal threshold voltages for the inverters. While two output nodes (O_1 and O_2) are shorted by the reset switch, their voltage is equal to a value between two threshold voltages. Following the reset phase, each inverter amplifies the difference between its relevant threshold voltage and this value; due to the regenerative nature of this structure, O_1 and O_2 reach the logic levels.

Applying the input signal, the outputs have to be forced to be separated in desired direction. Because of the positive feedback nature of the system, one must reset the structure to clear the previous data, then evaluate the correct direction according to the inputs and finally ignite the regenerative latch.

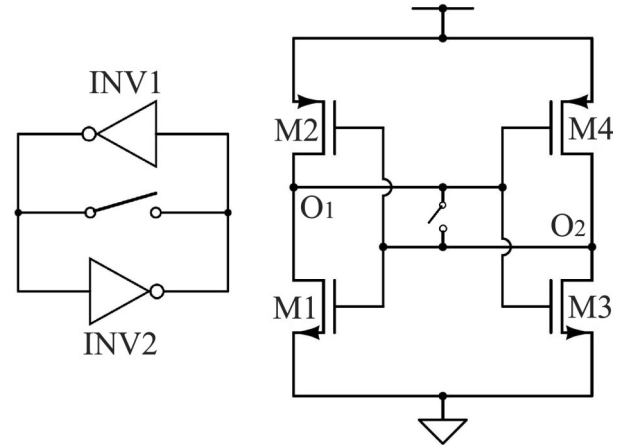


Figure 2: Block Diagram and Circuitry of Two Back-to-Back CMOS Inverters Forming an Intense Positive Feedback Structure.

3 Proposed High-Speed Comparator

Based on the described behavior of the latch block, a rail-to-rail folded cascode amplifier is modified using a positive feedback structure of two back-to-back inverters. Also an NMOS device is utilized as reset switch for removing the previously latched data from the output nodes. The structure is scheduled for performing the consecutive sequences of the comparison process (reset, evaluation and latch). The bias circuit is also an active block which alters the relevant biasing currents of the folded cascode in different operation modes. The proposed comparator structure besides its timing diagram is presented in Fig. 3. Four differential pairs ($M_5 - M_{12}$) are in connection with the cascode nodes of the amplifier. The analog input signals are applied to these differential pairs. The mentioned back-to-back inverter structure is formed by ($M_1 - M_4$). Two bias circuits are also observed in Fig. 3. The first section of the bias circuit ($M_{21} - M_{23}$) prepares the appropriate bias voltages for the current sources of the differential pairs. The next circuit is the active section of the bias block which provides the cascode devices ($M_{13} - M_{16}$) with variable bias voltage, proportional to the running operation mode.

Considering the timing diagram of Fig. 3, by rising edge of ϕ_1 , two output nodes are shorted through S_r . By the same time the infirm PMOS device M_{25} , enfeebles the positive feedback force of ($M_1 - M_4$) which facilitates the data removal process. Unlike most of the latched comparators, in the proposed structure of Fig. 3 the reset and evaluation sequences are merged and can be performed simultaneously in separate nodes. While the reset phase is running at the regenerative outputs, the primary evaluation of the input signals is going on at the cascode nodes.

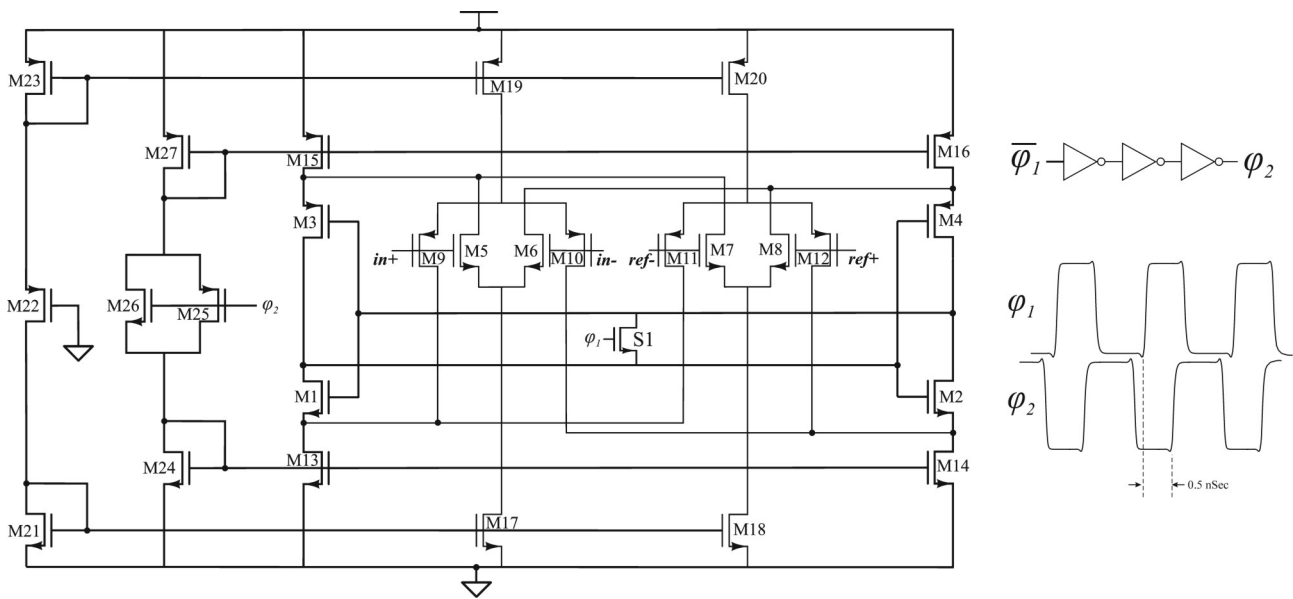


Figure 3: Improved High-Speed Comparator and its Timing Diagram.

After the evaluation, when the voltage difference reaches the detectable range of the positive feedback latch, M_{25} is replaced by M_{26} at the rising edge of ϕ_2 . So, the strength of the positive feedback is intensified again and the output voltages are separated up to the digital values. From another site of view, the evaluation phase has a separate timing schedule from reset and latch, making it possible to achieve both high speed and accuracy.

Kickback noise is a limiting factor for comparators accuracy [1, 4]. This kind of noise is mainly originated by the regenerative outputs of the positive feedback block. In the proposed comparator of Fig. 3 the current of the positive feedback inverters is limited by the cascode current sources ($M_{13} - M_{16}$), so rapid variations at the output nodes are avoided and hence the main source of kickback noise is limited.

4 Proposed Low Kickback Noise Comparator

The next proposed comparator is illustrated in Fig. 4. Similar to the comparator of the previous section, this structure also consists of two back-to-back inverters forming an intense positive feedback. What makes the proposed circuit distinguished is its novel data reception style. The input signals are applied to the bulks of the transistors via two differential pairs.

It is necessitous to reverse bias the drain-bulk diode of the transistors to insure their proper work, this affair can be realized in different ways. As it is done in mostly all conventional circuits one can ignore the bulks of the

transistors and connect them to VDD and GND respectively for PMOS and NMOS devices. All NMOS transistors on a single die have one common bulk terminal which is the substrate of the chip, it must be connected to the lowest voltage of the circuit (usually GND) to avoid the drain-bulk diode from turning on, so their bulk nodes are not applicable in almost all cases, but in case of PMOS transistors it is not the same. Each PMOS device can be constructed in an individual n-well region so its bulk terminal is also an individual node and can be connected to desirable voltages.

In this paper with aid of the capacitors ($C_1 - C_2$) and their relevant charging devices ($M_9 - M_{10}$), voltage level at the bulks of PMOS devices, M_2 and M_4 , is kept near VDD insuring the reverse bias of their drain-bulk diodes; also a floating state is established at these bulk nodes which are evaluation nodes of the circuit. The utilized capacitors, C_1 and C_2 , are selected as 100fF.

The maximum error arisen for capacitors of this size is about 5% ($\pm 2.5\%$), if their layout pattern is implemented accurately. With such an error, one of the inputs will have a higher influence, which introduces new offset source to the system; hence, the difference of the capacitors appears as offset voltage at the inputs of the comparator.

Applying the differential inputs alters the voltage level of the mentioned bulks against each other. According to (4), variations in the source-bulk voltage of a transistor directly affects its threshold voltage and consequently the corresponding inverters threshold. Thus the comparison is done by steering the threshold voltages in opposite directions.

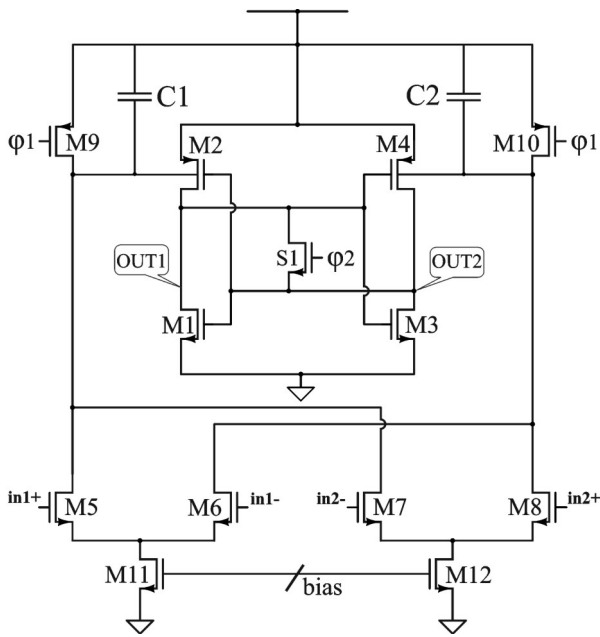


Figure 4: Proposed Low Kickback Noise Comparator.

$$V_{th} = V_{th0} + \gamma \left(\sqrt{V_{SB} + V_{\phi}} - \sqrt{V_{\phi}} \right) \quad (4)$$

Reset, evaluation and latch are three required phases which are performed consecutively in sequential one-stage comparators. This obligation affords delay to the process and limits the speed extremely. In the proposed structure, reset and evaluation sequences are performed simultaneously in separate nodes.

The digital controlling signals are illustrated in the timing diagram of Fig. 5. Reset phase starts at the rising edge of ϕ_2 , concurrently as ϕ_1 goes low, the capacitors C1 and C2 are approximately charged up to the VDD level; at the rising edge of ϕ_1 , evaluation occurs in the bulk terminals of M_2 and M_4 . In pursuit of the output reset, the evaluated data affects the regenerative latch; up to the next rising edge of ϕ_2 , the positive feedback has the opportunity for separating the output voltages. In other words, independence of the evaluation phase from reset and latch phases makes it possible to achieve both high speed and accuracy.

5 Readout Circuit

A simple readout circuit is utilized to hold the latched data. In absence of this circuit, the outputs of the comparator are set to a common mode voltage level after each reset phase and it lasts to reach the desired level once more. Implementing the readout circuit preserves the latched data of the regenerative nodes for one full clock cycle; in fact, it increases the validity period of

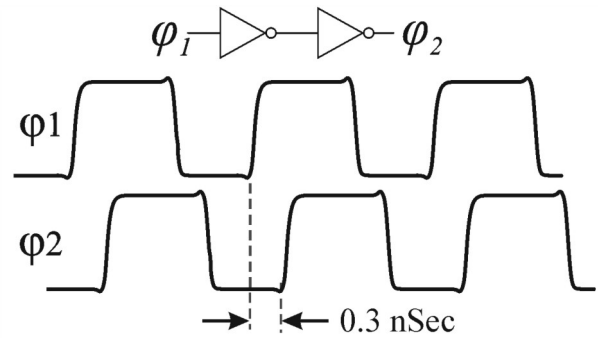


Figure 5: Timing Diagram for the Comparator of Fig.4.

the output signals. The discussed circuit is pictured in Fig. 6. It is made up of a data latch and a pair of NMOS devices. The outputs of the proposed comparators are applied to the gates of the NMOS devices; bit+ and bit- are the outputs of the readout circuit.

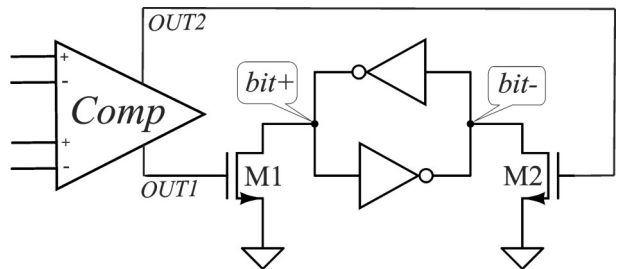


Figure 6: Conventional Readout Circuit.

Cascading the proposed comparator of Section 4 with the readout circuit of Fig. 6 introduces additional capacitance to the output nodes of the comparator hampering the comparison process. As a solution two inverters are implemented as interface between the comparator and the readout circuit. Aiming to reduce the input capacitance of interface circuit, the first inverter of each side has a different structure from the well-known static inverters. The NMOS devices of the first inverters at both sides of the interface circuit are connected to the comparator outputs but their PMOS side is driven by a delayed version of the RESET signal named W. The idea is pictured in Fig. 7.

Reviewing the function of this interface circuit for one side, at falling edge of W, the PMOS device M4 is turned ON for a short time period charging the node K+ and then goes OFF (pre-charge). If the output of the comparator is LOW, the NMOS device M3 will stay in cut-off region and cannot discharge the node K+ so it remains HIGH, but if the comparator output is HIGH, it makes the NMOS transistor to turn ON and discharge K+ (evaluation), hence the comparators output is inverted. K+ is inverted once more by a normal inverter producing the signal D+, this signal is then applied to the pro-

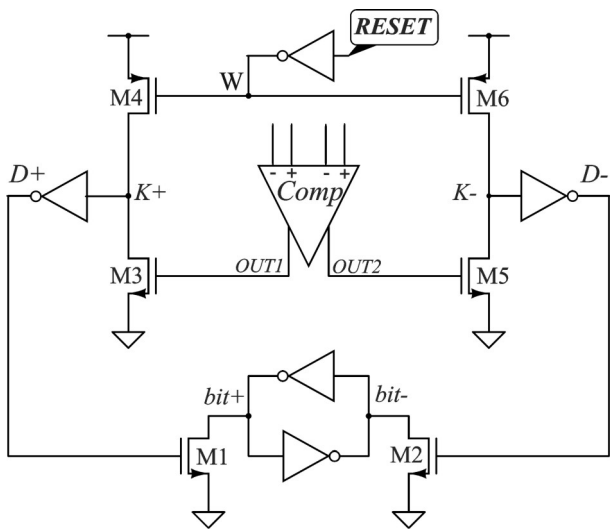


Figure 7: Proposed Readout Circuit.

posed readout circuit. Same story goes on for the next output of the comparator.

By this mean, only a minimum size NMOS device is connected to out1 and out2, so the additional capacitance is dramatically reduced insuring the correct comparison process.

6 Simulation Results

The main cores of the presented comparators beside the readout circuit of Fig. 7 are implemented in 0.35 μ m CMOS process. As illustrated in Fig. 8, an active area of 715 μ m² and 360 μ m² is occupied by the proposed comparators of Sections 3 and 4. In order to confirm the performance accuracy of the circuits in various terms, multiple simulations are performed in all process corners, using HSPICE (level49) with a standard 0.35 μ m CMOS process and the power supply of 3.3V. Aiming to generate a none-ideal power supply, some sinusoidal voltage sources are utilized in series with the VDD which leads to a noisy power supply. The simulation results indicate a 300mV p-p noise which is mounted on the VDD source.

In order to examine the capability of erasing the previously latched data, a challenging simulation known as worst case comparison is performed in which the input voltage alters from a large amplitude to a small value in the opposite direction and viceversa.

Precession of the operation is confirmed for both of the proposed structures. As illustrated in Fig. 9, the comparator of the Section 3 has the sufficiency of recognizing a 2mV differential input with 800MHz update rate. On the other hand, Fig. 10 confirms that a 1mV differen-

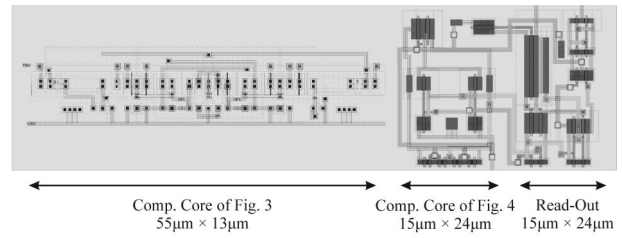


Figure 8: Layout of the Presented Comparators and Readout Circuit.

tial input at as high a clock frequency as 1GHz is simply sensible for the proposed comparator of Section 4. The measured power consumption of these two structures is 2.6mW and 1.6mW respectively.

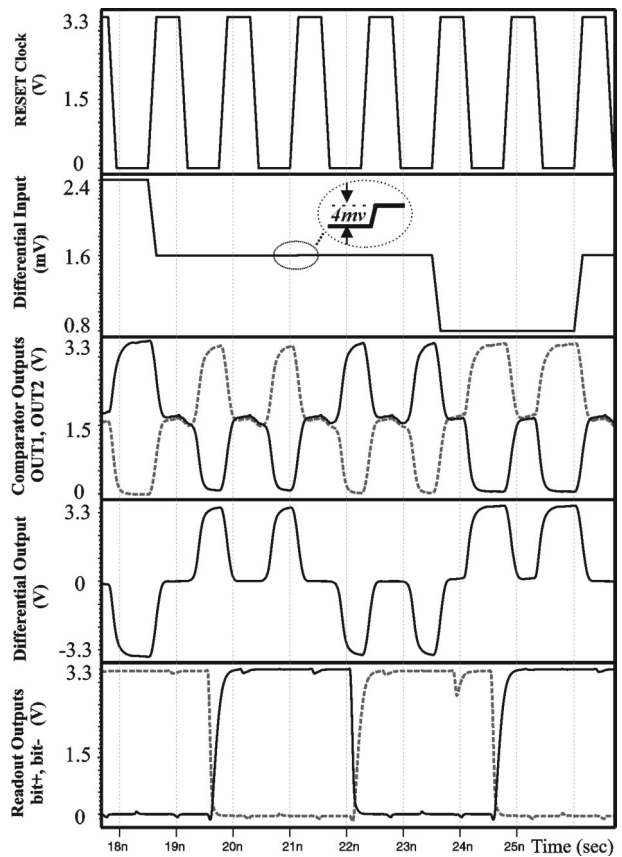


Figure 9: Simulation Results for Comparator of Fig. 3 Consisting the Reset Clock @ 800 MHz, Differential Input, Comparator Outputs, Differential Output and Outputs of the Readout Circuit.

In order to simulate the comparator of Fig. 4 with imbalance capacitors, C_1 and C_2 are selected as 97.5fF and 102.5fF (with $\pm 2.5\%$ tolerance). A variable ramp source is applied to the comparator as offset voltage source. As depicted in Fig. 11, once the offset cancellation source (ramp voltage source) reaches around the 1.9mVolts, the tolerance of the capacitors is compensated and the improper operation of the comparator is corrected. The issue confirms that any mismatch in the

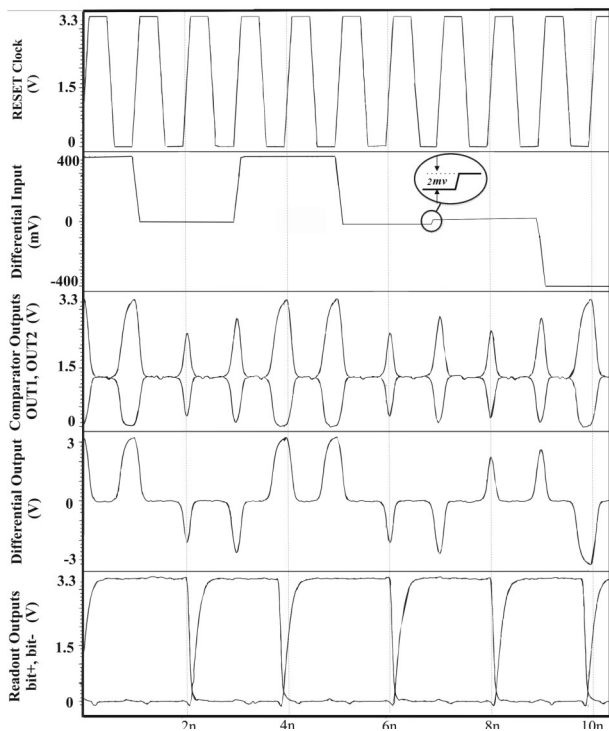


Figure 10: Simulation Results for Comparator of Fig. 4 Consisting the Reset Clock @ 1 GHz, Differential Input, Comparator Outputs, Differential Output and Outputs of the Readout Circuit.

capacitor values, appears as offset voltage at the inputs of the comparator, as well.

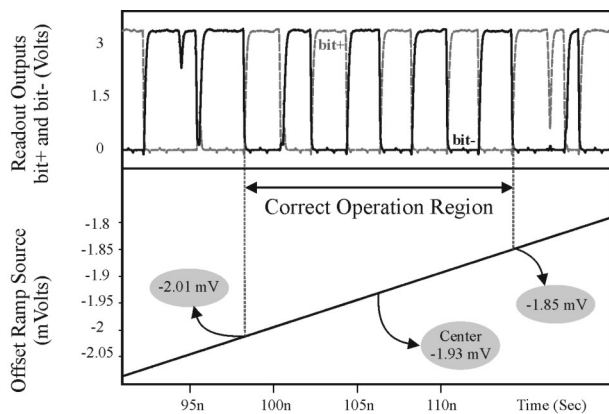


Figure 11: Correcting the Operation of the Comparator of Fig. 4 via a Variable Ramp Source Applied as Offset Voltage Source when C_1 and C_2 are Utilized with $\pm 2.5\%$ Tolerance.

The originated voltage spikes of the regenerative latch are not able to impress the ideal input voltage source; hence, a resistor string of 10K Ω is used at each end which makes it possible to measure the kickback noise level. According to Fig. 12 and Fig. 13, the maximum amplitude observed is about 1mV and 0.6mV respectively for the comparators presented in Sections 3 and 4.

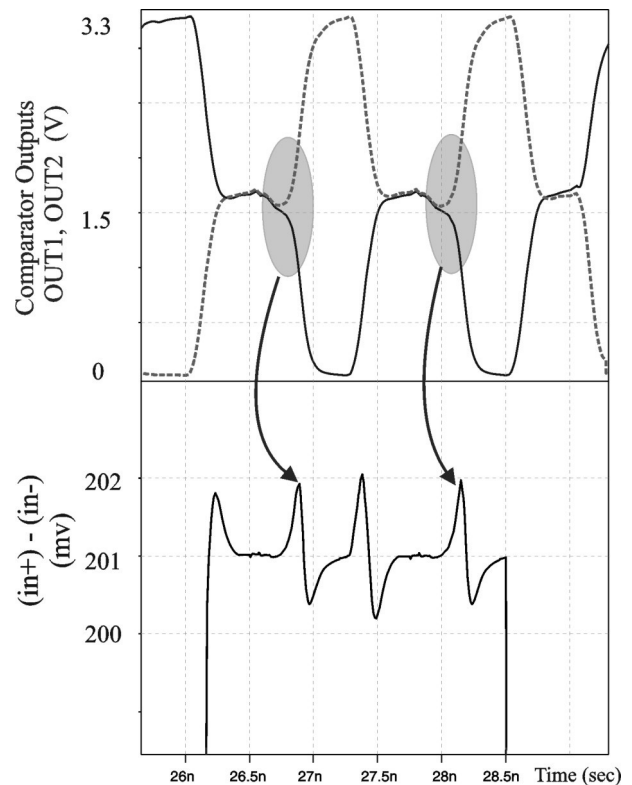


Figure 12: Kickback Noise Simulation for Comparator of Fig. 3.

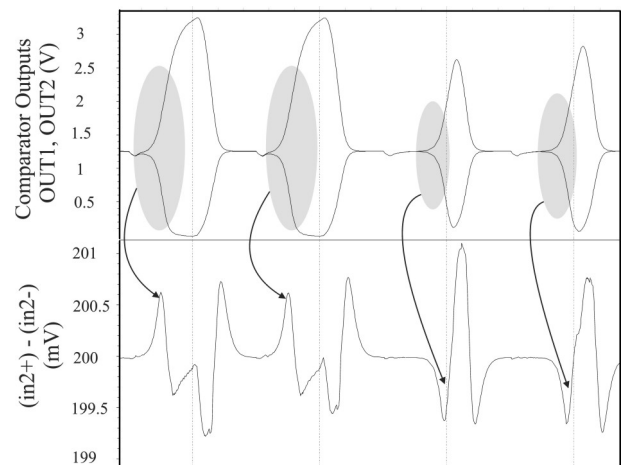


Figure 13: Kickback Noise Simulation for Comparator of Fig. 4.

7 Conclusion

A high performance comparator based on the preamplifier-latch topology was provided by improving the rail-to-rail folded cascode amplifier. Also a novel data reception style was utilized to engender a low-noise structure. Sufficiency of the comparators for high-speed, high-accuracy and low-power applications is confirmed by various simulation results. Table 1 sum-

marizes the performance of the proposed structures and Table 2 compares the proposed circuits with earlier presented similar works.

Table 1: Performance Summary

Process	Standard 0.35µm CMOS Process	
Supply Voltage	3.3Volts	
Power Supply Noise	300mVolts p-p	
Number of Stages	Single Stage	
	Improved High-Speed Comparator	Proposed Low Kickback Noise Comparator
Comparison Rate	800MHz	1GHz
Resolution	2mVolts	1mVolts
Kickback Noise Disturbance	1mVolts	0.6mVolts
Power Consumption	2.6mW	1.6mW
Area	55µm × 13µm	24µm × 15µm

Table 2: Comparison Table

	[1] (2011)	[4] (2010)	[10] (2012)	[11] (2014)	[12] (2011)	[13] (2013)	Proposed Comp. of Fig. 3	Proposed Comp. of Fig. 4
Process	0.35 µm	0.35 µm	45 nm	0.18 µm	0.18 µm	0.18 µm	0.35 µm	0.35 µm
No. Stages	1	1	3	1	1	2	1	1
Comparison Rate (GS/s)	1	0.5	20	2.4	0.5	1.25	0.8	1
Resolution (mV)	10	5	-	-	1	-	2	1
Power Consumption (mW)	1	0.6	0.561	329	0.6uW	0.274uW	2.6	1.6
Area (µm ²)	250	300	-	392	-	-	715	360
Kickback Disturbance (mV)	0.4	11.5	-	43 - 13	-	-	1	0.6

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