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Voltage Differencing Transconductance Amplifier based Ultra-Low Power, Universal Filters and Oscillators using 32 nm Carbon Nanotube Field Effect Transistor Technology

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Abstract: Carbon nanotube field-effect transistor (CNTFET) is a strong candidate to replace existing silicon-based transistors. The ballistic transport of electrons in the CNTFET channel leads to ultra-low-power and high-frequency devices. Although a lot of digital applications of CNTTFET were presented, less work was done in analog applications of CNTFETs. This paper presents analog applications of CNTFET and its implementation of voltage differencing transconductance amplifier (VDTA). The CNTFET VDTA based filters and oscillators were proposed. The VDTA circuits are resistorless and can be tuned electronically only by changing transconductance. The proposed CNTFET VDTA shows power consumption of 4000 times less than compared to silicon CMOS technology and a significant reduction in chip area. All simulations were performed using SPICE and MATLAB simulation tools.

Keywords: Carbon Nanotube (CNT); Carbon Nanotube Field Effect Transistors(CNTFET); Voltage differencing Transconductance Amplifiers (VDTA); MOSFETS

Univerzalni filtri in oscilatorji na osnovi napetostnega transkonduktančnega ojačevalnika v tehnologiji 32 nm poljskega tranzistorja z ogljikovimi nanocevkami

Izvleček: Poljski transistor z ogljikovimi nanocevkami (CNTFET) je močen kandidat za zamenjavo obstoječih silicijevih tranzistorjev. Balističen prenos elektronov v CNTFET kanalu omogoča nizko porabo moči in visoke frekvence. Kljub številnim digitalnim aplikacijam CNTFETov, je na analognem področju zelo malo objav. Članek opisuje uporabo CNTFET v analognem vezju napetostno diferencialnega transkonduktančnega ojačevalnika (VDTA). Vezja so brez uporov in elektronsko nastavljiva s spreminjanjem transkonduktance. Predlagano vezje ima 4000 krat nižjo porabo moči kot ekvivalentna izvedba v silicijevi CMOS tehnologiji. Simulacije so izvedenev SPICE in MATLAB okolju.

Ključne besede: Ogljikove nanocevke (CNT); poljski transistor z ogljikovimi nanocevkami (CNTFET); napetostno diferencalni transkonduktančni ojačevalnik (VDTA); MOSFET

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1 Introduction

Silicon-based MOSFETs have already reached their limits in scaling. CNTFET, with its ultra-long mean free path (MFP), looks to overcome the limitations of conventional silicon-based MOSFETs due to its unique electronic and mechanical properties. These properties come from their strong atom-to-atom bonds, ballistic or near ballistic transport, and quasi 1D features

of the CNT channel. Besides, by changing the chirality of the CNT its material properties can be changed from semiconducting to metallic. Many attempts at building CNTFET models have been reported in the literature [1-9].

Two major geometries are available for CNTFET design, which are planar and gate-all-around. Sanchez et al. have compared all available architectures and their performances [1]. Dokania et al. have proposed gate-all-around (GAA) or also known as wrap gate, analytical SPICE model [2]. The gate capacitance and drain current in the channel should be accurately designed to predict the precise performance of CNTFETs. Ahmed et al. proposed a model of the gate capacitance in which CNTs are arranged arbitrarily, unlike other models in which CNTs are placed at a fixed distance [3]. The authors of [3] have reported a 3% error with numerical simulations. Ballistic or near ballistic transport models for the drain current are proposed in [4-9]. These models are SPICE compatible, which means that the model can be easily compiled and integrated with any other circuit. The model used in this paper is from the articles [8-9].

Nizamuddin et. al proposed CNTFET and CMOS-based three-stage, hybrid operational transconductance amplifiers (OTA) [7]. Marani et al. reported improvement in DC gain by 17%, 40% less power consumption, and a decrease in output resistance by 90% in comparison to CMOS OTA [7]. Low power mixed-mode active filter using 12 CNT and 2 capacitors was presented by Zanjani et al. [14]. Jooq et al. designed CNTFET based ring oscillators suitable for the internet of things (IoT) applications [17]. Low power CNTFET based RF oscillator is reported in [18]. Digital applications of CNTFET, such as adders and multipliers can be found in papers [19-21].

Most of the CNTFET studies are limited to simulations only since commercially CNTFETs are not available. Mindy et al. have proposed a method for the production of CNTFETS in commercial silicon manufacturing facilities and reported experimental measurements of CNTFETs fabricated in two different manufacturing facilities [22]. Besides, the authors have improved the speed of the fabrication process 1100 times, by decreasing the deposition of CNT on the wafer from 48 hours to 150 seconds. Rebecca et al. have reported the first experimental data for CNTFET CMOS analog circuitry [23]. They have successfully fabricated 2 stages CTNFET CMOS op-amp with the channel length of 3 µm, which achieves the gain > 700. Thus, the basics of CNTFET technology is CMOS too. Even so, when we write CMOS, we refer to silicon-based CMOS in this paper.

The first Voltage differencing transconductance amplifier (VDTA) was introduced by D. Biolek as an active element for analog signal processing[10]. However, any author did not perform the circuit implementation and application until the authors of proposed the realization of CMOS filters using VDTA [11]. The miniaturizations of electronic gadgets are becoming mainstream in today's technology. It will get harder and harder to integrate passive inductors into nano level circuits. VDTAs can be used to simulate inductors in signal processing circuits.

This work is organized as follows: Section 2 and 3 present the fundamentals of CNTFETSs and VDTAs respectively. The simulations' results and discussion of CNTFET VDTA including its comparison with CMOS VDTA are presented in section 4. In section 5,the application example of VDTA is presented. The universal filter realization is presented in section 5.1. The simulation results of CNTFET VDTA based oscillators are presented in section 5.2. Finally, in section 6 the conclusion of this paper is presented.

2 Carbon nanotube field-effect transistors fundamentals

Carbon nanotubes can be classified as single-walled and multi-walled. CNTFETs presented in this paper are made from single-walled CNTS as shown in Fig. 1. The chirality of CNT is the key parameter that determines whether a material is metal or semiconducting. There are two parameters of chirality, n and m (in some books or papers also referred to as n1 and n2). The values of these chirality parameters vary according to the rolling up method of CNT. The CNT is metallic if the difference of n and m is a multiple of 3. Otherwise, if the difference of n and m is not a multiple of 3 then the CNT is semiconducting [12-13]. The CNTFET presented in this paper is designed with semiconducting CNT.

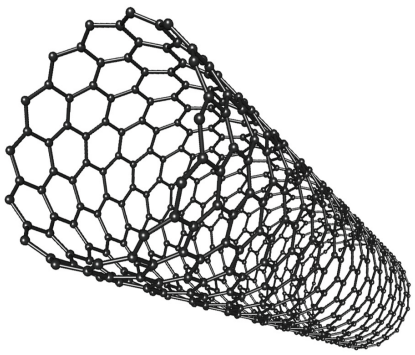


Figure 1: Rolled up Graphene sheet (Carbon Nanotube).

The bandgap is another key parameter which can be calculated from [12]:

$$E_G = \frac{2a_{cc}|t|}{2d} \approx \frac{0.8eV}{d} \quad (1)$$

Where, tight binging energy t is 3.0eV (also referred to as C-C bonding energy) and C-C bonding distance a_{cc} of the nearest neighbor is 1.42A°. Whereas, equations for CNT diameter CNTFET threshold are given as [13]-[14]:

$$D_{CNT} = \frac{\sqrt{n^2 + m^2 + mn}}{\pi} a \quad (2)$$

$$V_T \approx \frac{aV_\pi}{\sqrt{3}eD_{CNT}} \quad (3)$$

Here, *a* (C-C unit vector length) is 0.246 nm. From equations, it is obvious that both bandgap and threshold voltages are dependent on the diameter of CNT. The width of CNTFET can be calculated from the parameters like the number of tubes, the distance between tubes, and the diameter of CNT.

$$W = (N-1)S + D_{CNT} \quad (4)$$

Numerical simulations of equations (1) and (3) were performed via MATLAB tool and the results are shown in Fig. 2 and Fig. 3. The exponential proportional dependency of CNT diameter for both bandgap and threshold voltage was observed. Both, threshold and band gap values increase as the CNT diameter value decreases.

The CNTFET model used in this research is shown in Fig. 4 [8-9;14]. The CNTs are placed under the gate separated by high-k (high dielectric constant) material. The CNT extension regions between S/D and gate are heavily doped. Default parameter values provided by authors of the model [8-9;24] are shown in Table 1.

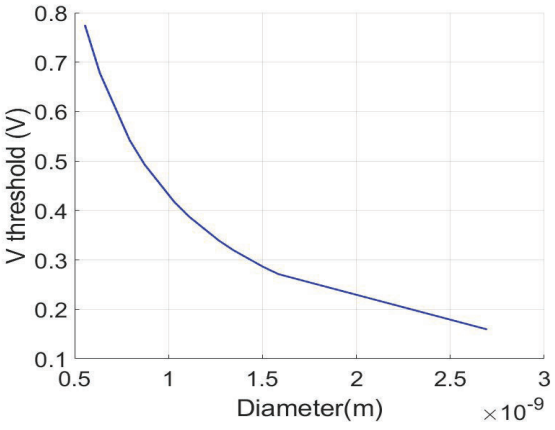


Figure 2: CNT Diameter vs V threshold.

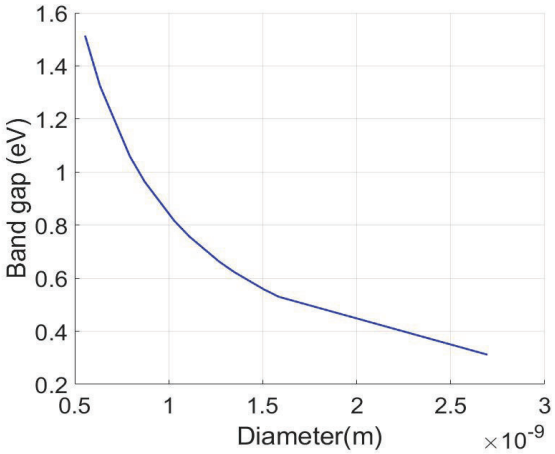
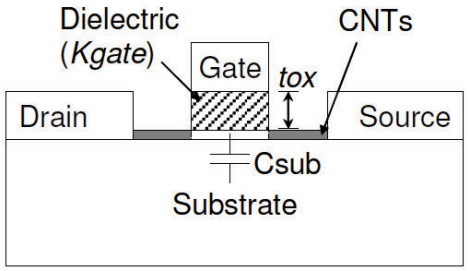


Figure 3: CNT Diameter vs bandgap.

(a)



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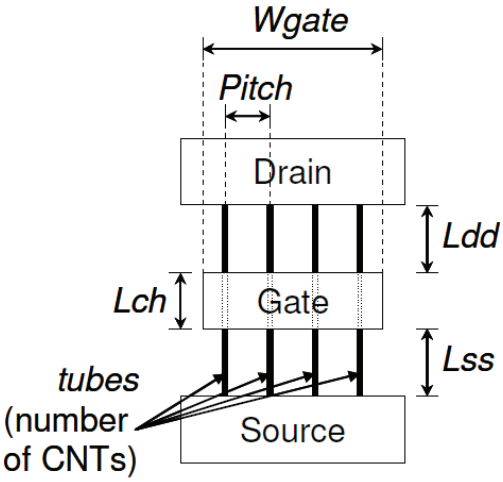

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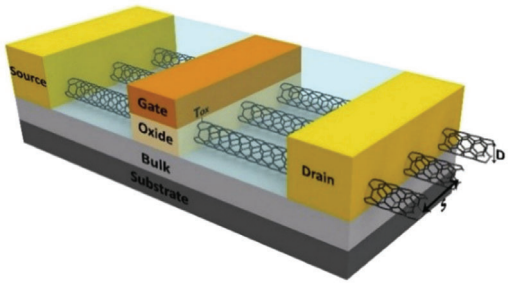

Figure 4: MSOFET-like CNTFET, a)1-D side view b) top view, c) 3-D view of typical TG CNTFET [8-9].

3 VDTA

The proposed VDTA's circuit symbol and its circuit architecture at CNTFET level are shown in Fig. 5 and Fig. 6 respectively. The VDTA is an active element with high impedance input terminals V_P, V_N, and high impedance output terminals Z, X+, and X-. The relationship between I/O terminals of an ideal VDTA can be expressed as follow [11]:

$$\begin{bmatrix} I_Z \\ I_{x+} \\ I_{x-} \end{bmatrix} = \begin{bmatrix} g_{m1} & -g_{m1} & 0 \\ 0 & 0 & g_{m2} \\ 0 & 0 & -g_{m2} \end{bmatrix} \begin{bmatrix} V_{VP} \\ V_{VN} \\ V_{VZ} \end{bmatrix} \quad (5)$$

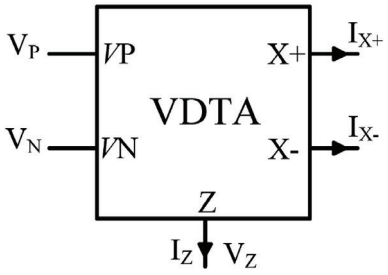

Figure 5: The Circuit Symbol of VDTA.

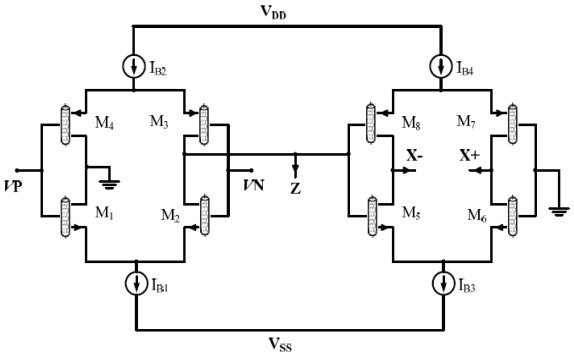

Figure 6: CNTFET implementation of VDTA.

Where g_{m1} is the transconductance of the first stage and g_{m2} is the transconductance of the second stage. The voltage difference at the input terminals P and N transforms into output currents at terminal Z by g_{m1}. Then the voltage at the terminal Z is converted to output currents by g_{m2} at the output terminals x+ and x- [15]. VDTA can be tuned electronically by adjusting the values of g_m of the first stage or second stage.

4 Simulations, results, and Discussions

All simulations were performed using HSPICE software. The parameters of CNT transistors used to get DC and AC characteristics of CNTFET VDTA are shown in Table 2. Supply voltages are fixed to $V_{DD} = -V_{SS} = 0.3V$ and biasing currents are –considered as $I_{B1} = I_{B2} = I_{B3} = 1\mu A$. DC varying between –0.3V and 0.3V was applied first to the P and N terminals to measure the output current and to the Z terminal. Then DC changing between –0.3V and 0.3V was applied Z terminal of VDTA to measure output currents at terminals +X and -X. The results of DC transfer characteristics for ideal current sources are shown in Fig. 7 and Fig. 8 in two steps. As expected, the output current increases as the CNT diameter increases. Because the I_{on} of CNTFET increases as diameter increases due to an increase in carrier mobility and velocity [25]. For instance, in Fig. 7, the output current of CNTFET VDTA for 0.1V with CNT (7,0) is around 0,85μA, CNT (13,0) is around 0,89μA, CNT (19,0) and CNT (34,0) is 0,90 μA.

Table 1: Design parameters and definitions [24].

Parameter	Definition	Value
Lch	Length of channel	32nm
Lss, Ldd	The length of the doped CNT source/drain extension region.	32nm
Pitch	The distance between the centers of two adjacent CNTs within the same device	20nm
Dcnt	The diameter of Carbon Nanotubes	1.5nm
Tox	The thickness of the high-k top gate dielectric material	4nm
Parameter	Definition	Value
Kox	The dielectric constant of a high-k gate oxide material.	16
Tubes	The number of tubes in the device.	3
(n1, n2)	The chirality of tube	(19, 0)

Table 2: Transistor dimension of Proposed CNFET VDTA FCS.

Transistors	W(nm)	L(nm)	Chirality	D_{CNT}(nm)	Tubes
M1,M2,M5,M6	41.5	32	19,0	1.5	3
M3,M4,M7,M8	221.5	32	19,0	1.5	12

The AC response of CNTFET VDTA for different CNT parameters is shown in Fig. 9 and Fig. 10. The same supply voltage and bias currents as in the previous section were used. Similar to DC simulations, two-step simulation and measurement was done to get the AC response of VDTA. In the first step, the input AC voltage of 1V was applied at one of the input terminals P or N, and the gain at the output terminal Z was measured. In the second step, both input terminals were grounded and the input AC voltage of 1V was applied to the Z

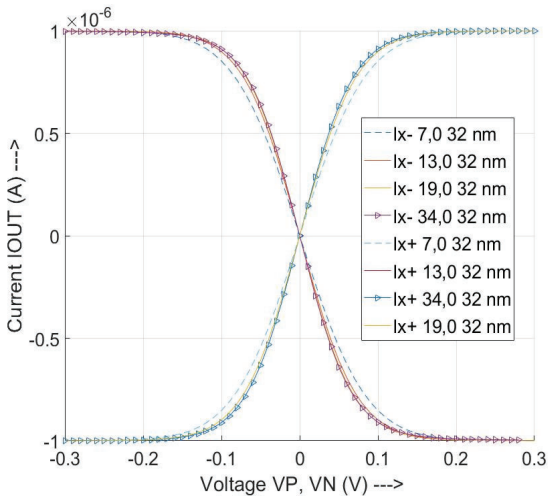

Figure 7: DC Characteristcs of CNTFET VDTA. Step 1 $V_{in} = V_P$ and V_N vs I_z.

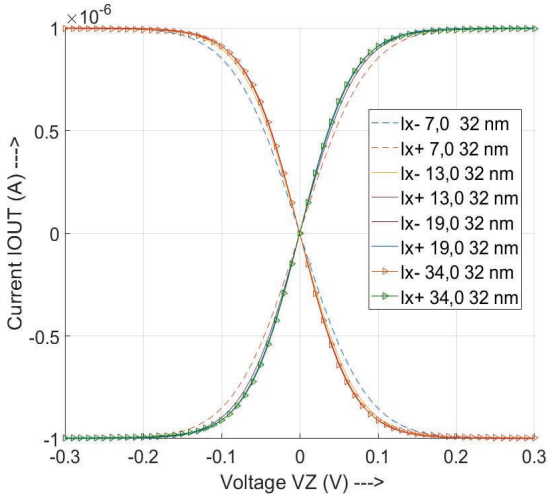

Figure 8: DC Characteristics of CNTFET VDTA. Step 2 $V_{in} = V_z$ vs I_{x+} and I_{x-}.

terminal. The output gain was measured from the X+ terminal. Both steps of DC/AC simulations show the same results which prove that CNTFET VDTA is operating properly.

Table 3: Comparison of CNFET and CMOS technologies.

VDTA Structure	Supply voltage	Biasing current	Power consumption	Transistor dimension N-type (channel WxL)	Transistor dimension P-type (channel WxL)
CMOS 18µm	±0.3	1mA	12mW	1.296 µm²	5.99904 µm²
CMOS 32nm	±0.3	400 µA	4.8mW	0,00132 µm²	0,00708 µm²
CNTFET 32nm	±0.3	1µA	1.2 µW	0,00132 µm²	0,00708 µm²

Comparison of CMOS 0.18um, CMOS 32nm node technology VDTA, and CNFET 32 nm technology VDTA is shown in Table 3. All three architecture is designed to meet the same frequency response ($f_c \approx 3.5$ GHz). For the case of CMOS 32 nm VDTA, the DC characteristics degrade a little bit, the maximum output current does not reach the supplied ideal current source. Where CMOS 0.18 µm maximum current reaches and CNTFET VDTA maximum current reaches. Besides, even if the same dimensions (channel WxL) as for CNTFET VDTA are used for CMOS 32nm VDTA, the biasing current of 400µA is needed for CMOS 32nm technology to meet the same frequency response of CNTFET.

As we can see from graphs in DC simulations (Fig. 7-8) there is no much difference between CNT (7,0), (13,0), (19,0), and (34,0). However, the V_{th} of (7,0) is much higher compared to (34,0).In AC simulations of VDTA (Fig. 9-10), we can observe a significant increase in gain with the change of CNT chirality from (7,0) to (19,0). Between (19,0) and (34,0) there is no much difference in gain but the diameter changes from 1.5 nm to 2.6 nm which will drastically increase the transistor dimension as well. Hence, we have selected CNT (19,0) for our further simulations. Another reason for selecting CNT (19,0) is to compare our simulation results with other references. Because all other works also used (19,0) CNT, including the authors of the original model from [24].

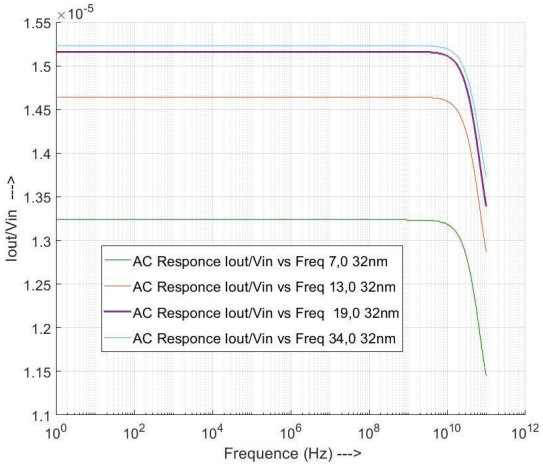

Figure 9: AC Characteristics of CNTFET VDTA. Step1 $V_{in} = V_P$ vs I_z/V_P.

5 Application example

VDTA has a wide range of applications in the analog signal processing field. One of them is a spectrum analyzer shown in Fig. 11. This spectrum analyzer uses low pass filters, bandpass filters, local oscillators, and mixers to get the final intermediate frequency (IF).

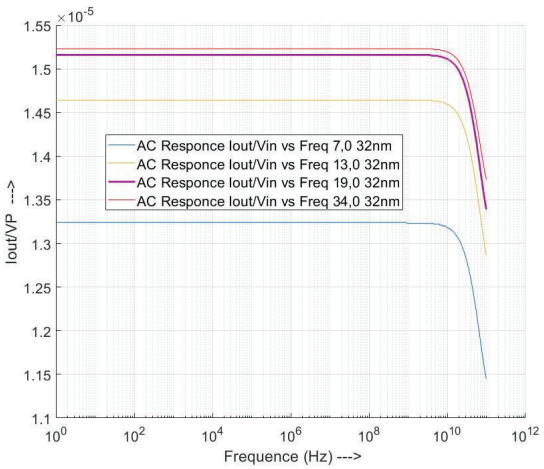

Figure 10: AC Characteristics of CNTFET VDTA. Step2 $V_{in} = V_z$ vs I_{x+}/V_z.

As an application example, this paper presents four filters and three local oscillators used in the spectrum analyzer.

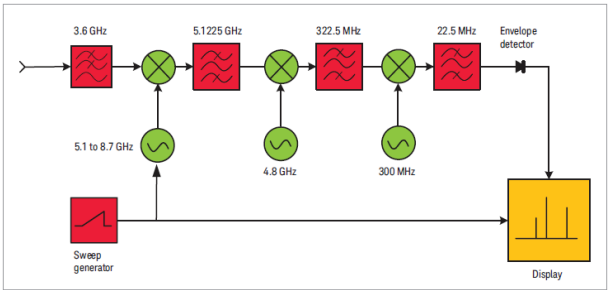

Figure 11: Spectrum analyzers [16].

5.1 Filters

VDTA can be categorized as voltage mode and current mode. This paper presents voltage mode CNTFET VDTA. The realization of CNTFET voltage mode VDTA derived from ref [11] is shown in Fig. 6. Further, the universal filter topology of CNTFET VDTA is proposed as shown in Fig. 12. The presented CNTFET VDTA filter can operate as LP and BP filter.

The transfer function of the filter is as follow:
If $V_1 = V_{IN}$ then

$$BP \rightarrow \frac{V_{O1}}{V_{IN}} = \frac{sC_1 g_{m1}}{s^2 C_1 C_2 + sC_1 g_{m2} + g_{m1} g_{m2}} \tag{6}$$

$$LP \rightarrow \frac{V_{O2}}{V_{IN}} = \frac{g_{m1} g_{m2}}{s^2 C_1 C_2 + sC_1 g_{m2} + g_{m1} g_{m2}} \tag{7}$$

And the expressions for Quality factor and natural frequency are given below:

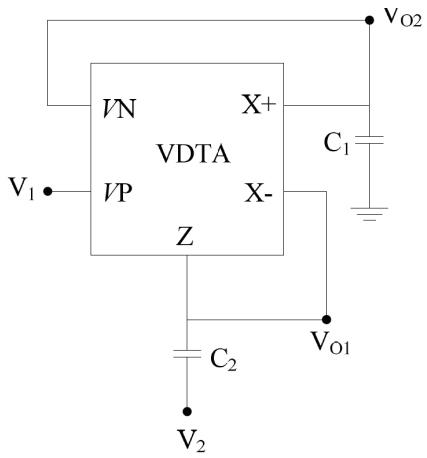

Figure 12: Application of proposed CNTFET VDTA filter.

$$w = \sqrt{\frac{g_{m1} g_{m2}}{C_1 C_2}} \tag{8}$$

$$Q = \sqrt{\frac{C_2 g_{m1}}{C_1 g_{m2}}} \tag{9}$$

The filter blocks from Fig. 11 have been realized using proposed CNTFET VDTA from Fig.12 and the results are plotted in Fig. 13. The parameters of CNT transistors used for filter applications are shown in Table 2. The values of capacitors used for the filter application of CNTFET VDTA are shown in Table 4. The same supply voltage and bias currents as in the previous section were used. CNT (19,0) was selected for further applications of VDTA. There is no much difference between (7,0) and (19,0) CNT when the biasing current is set to 1µA. As biasing current increases, the center frequency of filters also increases due to an increase in transconductance.

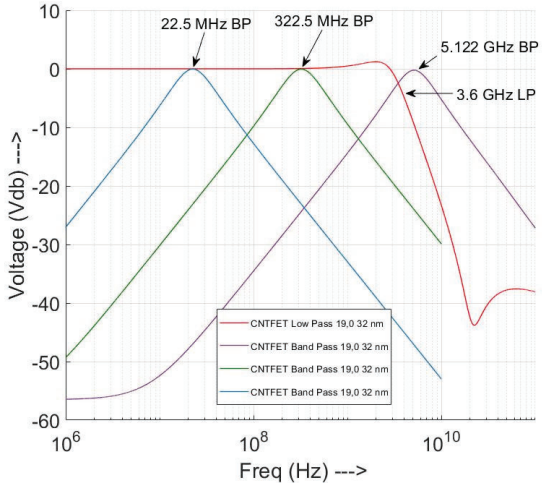

Figure 13: 3.6GHz LP, 5.122GHz BP, 22.5MHz BP and 322.5MHz BP filters.

Table 4: Capacitor values selected CNFET VDTA filters.

Filters	C1	C2	Chirality n,m
3.6 GHz LP	80.5fF	80.5fF	19,0
5.122 GHz BP	0.4334fF	0.4334fF	19,0
322.5 MHz BP 22.5 MHz BP	74.5pF 10.72pF	74.5pF 10.72pF	19,0 19,0

5.2 Oscillator

The oscillator is a DC to AC converter, which converts DC input signals to AC output signals such as sinusoidal waves. Local oscillators are used to change the frequency of the signal as in a spectrum analyzer from Fig. 11 and along with mixers, they improve the performance of receivers in electronic circuits. The circuit symbol of the CNTFET VDTA oscillator is shown in Fig. 14. The oscillator blocks from Fig. 11 have been realized using the proposed oscillator structure.

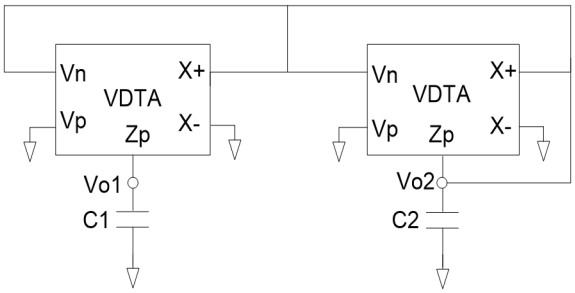

Figure 14: Application of proposed CNTFET VDTA quadrature oscillator.

The circuit analysis of the second-order characteristical equation can be represented as:

$$s^2C_1C_2 + sC_2(g_{m3} - g_{m4}) + g_{m1}g_{m2} = 0 \quad (10)$$

$$g_{m3} = g_{m4} \quad (11)$$

$$\omega_0 = \sqrt{\frac{g_{m1}g_{m2}}{C_1C_2}} \quad (12)$$

Where $g_{m3} = g_{m4}$ is the condition for oscillation and ωo is oscillation frequency. The parameters of CNT transistors used for oscillators applications are shown in Table 5. Supply voltages are fixed to $V_{DD} = -V_{SS} = 0.3V$ and biasing currents are considered as $I_{B1} = I_{B2} = I_{B3} =$ 1μA. The simulation results are plotted through Fig. 15-Fig. 17.

Table 5: Transistor dimension of proposed CNFET VDTA oscillator.

Transistors	W(nm)	L(nm)	Chirality	D_{CNT}(nm)	Tubes
M1,M2,M5,M6	221.5	32	19,0	1.5	12
M3,M4,M7,M8	1121.5	32	19,0	1.5	57

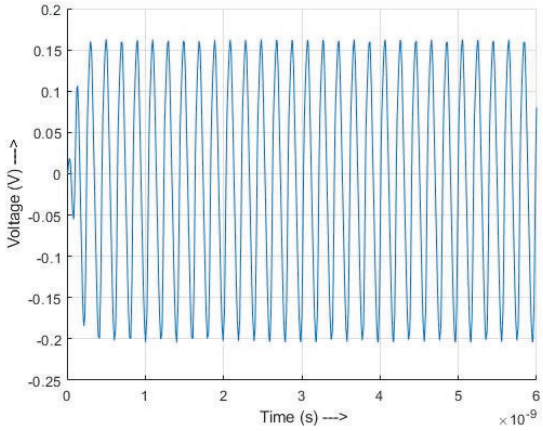

Figure 15: 5.1 GHz VDTA Based Oscillator C1=C2 =0.068fF.

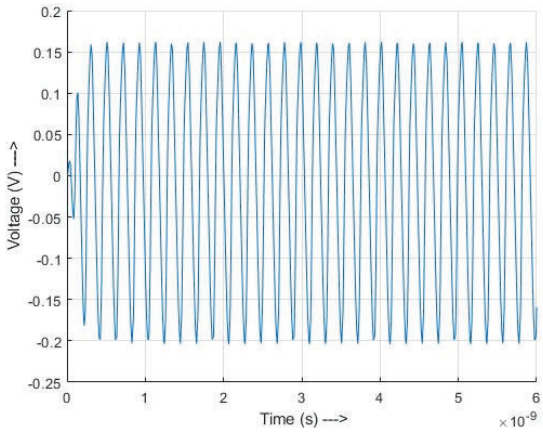

Figure 16: 4.8 GHz VDTA Based Oscillator C1=C2 =0.08fF.

6 Conclusion

Ultra-low-power CNTFET based VDTA filters and oscillators were presented. As shown in Table 3. CNTFET 32 nm based VDTAs consume the power of 4000 times less than CMOS 32nm based VDTAs. Also, n-type CNTFETS occupy approximately 989 times less than space in the chip area (only considering effective channel WxL) compared to n-type MOSFET transistors while p-type CNTFETS occupy approximately 848 times less space(only considering effective channel WxL)

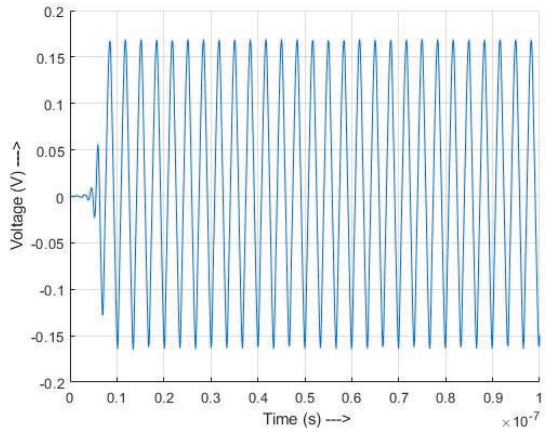

Figure 17: 300 MHz VDTA Based Oscillator C1=C2 =3.9fF.

compared to p-type 0.18µm technology node MOSFETS used in typical VDTAs. Higher biasing current or capacitors may be adjusted to change the center frequency of CNTFET filters. CNTFET VDTA based filters and first-ever CNTFET VDTA based oscillators for spectrum analyzer are presented as an application example.

7 Conflict of interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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