Professional paper

Informacije MIDEM
Journal of Microelectronics,
Electronic Components and Materials
Vol. 45, No. 1 (2015), 87 – 97

Contour Graph Approach of Micropower Clock Generator Design for Energy Harvesting Charge Pump Circuits

R. Aloulou[1,2], J. Armand[2], P-O Lucas de Peslouan[2], F. Alicalapa[2], H. Mnif[1], J. D. Lan Sun Luk[2] and M. Loulou[1]

[1]LETI Lab, University of Sfax, Tunisia
[2]LE2P Lab, University of La Reunion Saint Denis, Reunion, France

Abstract: This paper presents a novel design methodology of micropower noncritical clock generator for charge pump circuits. Embedded clock generator circuit requires careful attention in terms many issues: topology choices, component sizes, power dissipation and signal voltage values. This paper also presents comparisons and performance optimization of microwatt clock generators using SPICE simulator. Additionally a contour graph approach is developed to find relevant parameters value in order to minimize the power consumption and the chip area. The circuit design was implemented on standard 0.35 µm Si CMOS process. The active area dimensions are 42 µm*25 µm. Consistent results were obtained between experimental results and transient simulations. In comparison to previous papers, under low-voltage constraints, interesting measured circuit consumption was observed: 1.15 µW from 1 V.

Keywords: Contour curve; clock generator; micropower clock; power consumption; optimization; low power; charge pump; energy harvesting

Metoda grafa obrisa za urni generator majhnih moči pri črpanju energije z okolja

Izvleček: Članek predstavlja novo metodologijo načrtovanja urnih generatorjev za črpanje energije z okolja. Vgrajeno vezje urnega generatorja zahteva posebno pozornost pri: topologiji, velikosti komponent, porabi energije in napetosti signala. Predstavljena je optimizacija in primerjava urnih generatorjev v SPICE okolju. Za zmanjšanje porabe energije je uprabljena metoda grafa obrisa. Vezje je bilo implementirano v 0.35 µm Si CMOS tehnologiji z aktivno površino 42 µm * 25 µm. V primerjavi s prejšnjimi rešitvami je bila dosežena nizka poraba energije: 1.15 µW pri napetosti 1 V.

Ključne besede: Graf obrisa; generator ure; poraba energije; energija iz okolice

** Corresponding Author's e-mail: aloulourahma@yahoo.fr*

1 Introduction

Energy harvesting is becoming a practical solution to improve battery lifetime in micro-scale electronic systems for wireless sensor applications. Many research papers have been proposed to design an energy harvesting system based on a charge pump circuit [1]. Charge pumps (CPs) are circuits that generate voltages greater than the supply voltage from which they operate. Some of these circuits are based on two anti-phase pumping clocks [2]. For this charge pump circuit operation, low frequency clock generator is actually needed. Clock generator circuits are thus widely-used in CPs and are an important subpart of these systems [3,4]. In the literature, some papers have been published on their performance, where oscillators are aimed to be used as clock generators [3, 5, and 6]. In the context of energy scavenging, power consumption is a crucial issue [7]. The energetic constraint is also applied to clock generators despite the fact that it is sometimes underplayed or un-optimized. This trend is confirmed by the publications on subthreshold mode circuits [8], in which power consumption is dominated by leakage current Ioff [9, 10] and supply voltages lower than 1 V [7]. Furthermore to keep the cost low, attention should

also be given to the chip size by introducing effective design methods.

This work compares power consumption and performance analysis of different square-wave clock generator topologies. Topologies comparison aim at selecting an appropriate low frequency clock generator topology, under low power constraint, in the energy scavenging context. This comparison is performed under some specific conditions: the energy criterion is more important than noise performance. The operating frequency is in the range of hundreds of megahertz (in accordance with charge pump circuit design concepts for energy harvesting applications [11], from 1 Hz to 100 MHz). Furthermore, the clock signal generator is designed to drive CP switches [4]. In this scheme, its output square signal amplitude should be high enough to have an appropriate voltage gate control of the CP switches. In this work, the minimum voltage level is set to V_t = 0.7 V, as the CP CMOS switches are not operating in subthreshold mode. About the supply voltage, as the clock generator will be associated with a bandgap and a charge pump circuit, the typical value that will be considered is 0.8 V. And finally in this context, the studied topologies are intended for application in highly integrated systems (consuming a reasonable silicon area), using a low-cost 0.35 µm Si CMOS process.

Many candidates are well-known in the literature: LC circuits, CMOS oscillators and crystal oscillators. Some of them are not suitable for low-cost process integration (crystal oscillators) or rather interesting for high frequency low noise applications. Some others use additional external components. Alternative topologies are interesting for the purpose of this work: the Schmitt trigger circuit, the ring oscillator and the voltage controlled ring oscillator. Some drawbacks are known, but under certain aspects of ring oscillators, they can be exploited. All, these points will be respectively presented in section 2, 3 and 4. Attention will be paid to low power consumption and frequency range in order to select one of these circuits. Section 5, will present the contour graph methodology which was used to optimize the circuit under the constraints (power, frequency, chip area). Then a power consumption comparison is performed for the different clock generator topologies at selected low frequencies. Measurement results are provided in section 6, along with the parasitics effect on power consumption offset and comparison with some publications. Section 7, finally presents the conclusions of this paper.

2 Schmitt trigger clock generator STCG

The circuit depicted in Fig. 1 is known as a multivibrator circuit, astable type. The circuit is configured around an inverting Schmitt trigger gate and a delay structure (composed of the surrounding components, R and C).

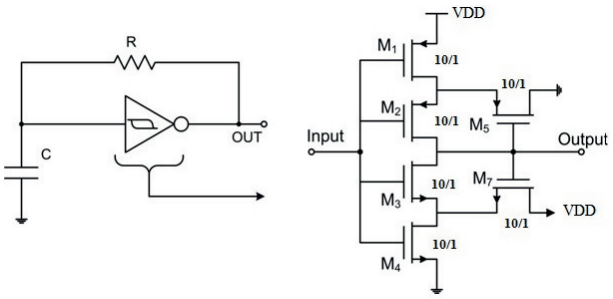

Figure 1: Schmitt Trigger Clock Generator circuit

The oscillation frequency f_o is mainly determined by the delay structure as:

$$f_o = \frac{1}{RCIn\dfrac{V_{high}\left(V_{low}-V_{DD}\right)}{V_{low}\left(V_{high}-V_{DD}\right)}} \quad (1)$$

Where, V_{DD} is the power supply voltage. Considering the upper (V_{high}) and lower (V_{low}) switching voltages (usually associated with transistors transconductance ratios), which define the hysteresis of the gate in the transfer curve: the Schmitt trigger's output is a well defined voltage, which is really suitable for noisy signal or signal cleaning functions [12].

Dynamic behavior simulations of STCG circuit have been performed using SPICE simulator and 0.35 µm Si CMOS process parameters.

The operating frequency range was simulated for different values of the delay structure (τ = R.C, Fig. 2).

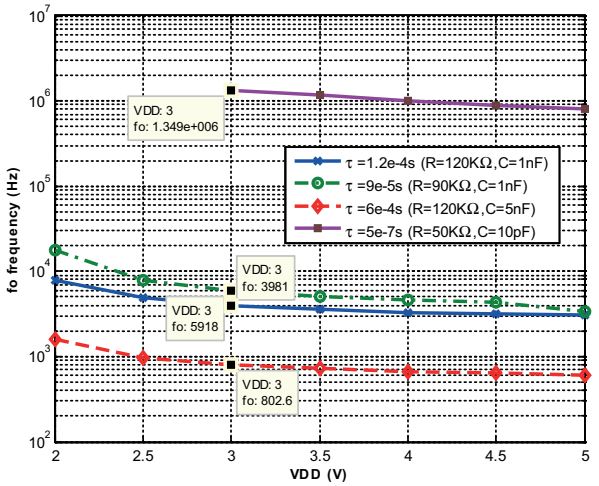

Figure 2: Simulated output frequency fo versus supply voltage (VDD) - STCG circuit

Over the frequency range of 10 Hz to hundreds of megahertz, f_o is inversely proportional to τ = R.C. The oscillation frequency range is obviously governed by the RC time-constant.

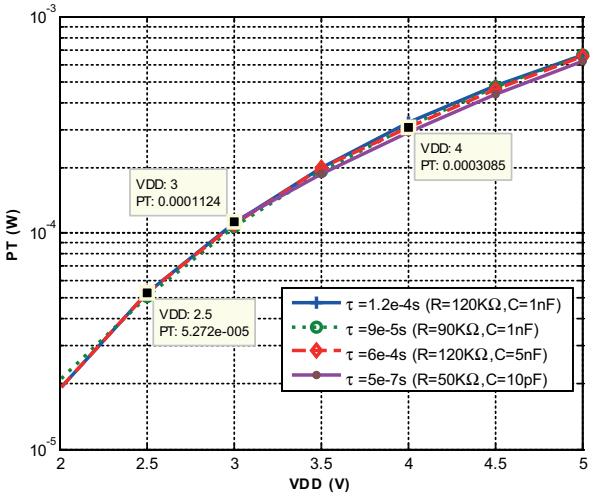

Figure 3: Spice simulated power consumption as a function of the supply voltage VDD - STCG circuit

From the power dissipation point of view, Fig. 3 displays power simulation results as a function of the supply voltage V_{DD}. From this graph, it can be seen that a fall of the supply voltage, lowers the power consumption. Also, it can be deduced that the variation of the power consumption has a small fluctuation as function of the delay structure τ.

Transient results and the theory reveal that the circuit does not work properly for a supply voltage less than 2 V. In fact, the gate hysteresis tends to disappear at this voltage level. At this lowest 2 V voltage, the total power consumption is 20 µW.

Consequently, and especially in the context of our purpose where a low power and frequency clock generator is required, this drawback (lowest supply voltage=2 V) can represent a major limitation for the use of this topology. In the next section a different topology (inverter based clock generator) is presented.

3 Ring oscillator RO

A ring oscillator (RO) (Fig. 4) consists of an odd number of inverters in a unity gain feedback loop [13]. To achieve oscillation, the circuit must satisfy the Barkhausen's criterion which means that the total phase shift and the gain of the feedback loop must be 2π and one respectively [14].

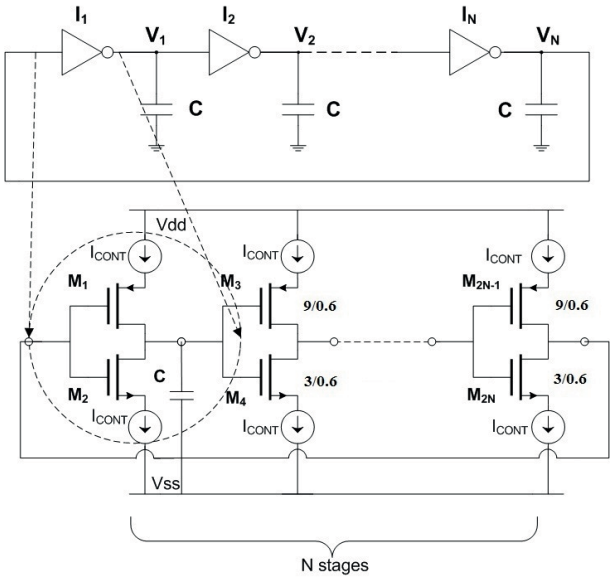

Figure 4: Ring Oscillator circuit and additional C capacitors

To design oscillators whose output frequency ranges from 1 Hz to 100 MHz, a ring structure of three stages is chosen. C capacitors have also been included to lower the output signal frequency to meet the custom specifications of charge pump circuits.
Instead of C addition, we could have chosen a greater number of stages. In terms of output frequency value and power consumption, this is not compatible with our application (supply voltage value of 0.8 V and low power circuit) as depicted in Table 1.

Table 1: RO clock generator frequency as a function of V_{DD} and the inverter stage number without capacitors

V_{DD} (V)	3 stages	5 stages	7 stages
0.8	18.45 MHz	10.54 MHz	7.65 MHz
1	115.5 MHz	63.1 MHz	44.55 MHz
1.5	257 MHz	191 MHz	114.5 MHz

Theoretically, the frequency of the oscillation can be found as:

$$f_o = \frac{1}{2N\tau_{inv}} \quad (2)$$

Where *N* is an odd number and τ_{inv} is the propagation delay of one inverter stage. The delay of each inverter stage will be given by:

$$\tau_{inv} = \frac{V_o C_{in}}{I_{CONT}} \; avec \; V_o = \int \frac{I_{CONT}}{C_{in}} dt \quad (3)$$

Where, V_o is the voltage signal amplitude, I_{CONT} is a DC control current source (Fig. 4) and C_{in} the equivalent input capacitor of the following inverter (intentional ad-

dition (C) and MOS transistors parasitics). The expression of the frequency becomes [15]:

$$f_o = \frac{I_{CONT}}{2NV_oC_{in}} \quad (4)$$

It is known that the delay of each stage is governed by the supply voltage V_{DD} and the capacitors value, C. This dependence can be verified by simulations of the frequency performance and power consumption (Fig. 5 and Fig. 6). These parametric simulations (sweep on C) are performed as a function of V_{DD}.

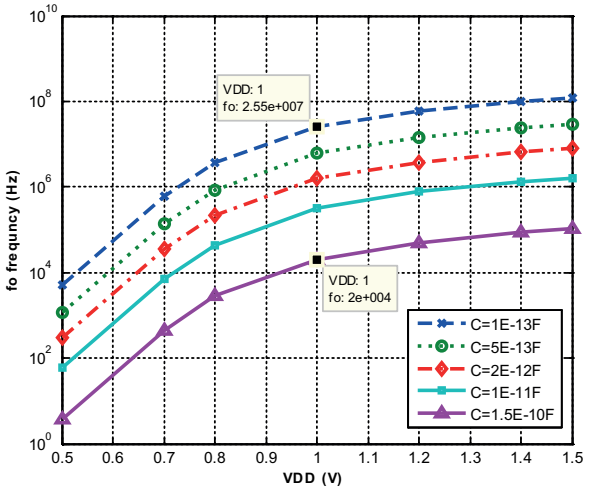

Figure 5: Simulated output signal frequency (fo) as a function of the supply voltage V_{DD} and C capacitor value, RO circuit

In Fig. 5, considering the V_{DD} range between 0.5 V and 1.5 V, the output frequency ranges from 10 Hz to 1 GHz. But referring to section 1, the lowest supply is limited to 0.7 V in order to ensure the charge pump correct operation. In the same context, considering the lowest voltage limit, the real performances range from 500 HZ to 1 GHz. Furthermore, taking into account additional circuits which should be included in the global charge pump circuit (bandgap and charge pump circuit), the supply voltage must be greater than 0.8 V and below 1.5 V. In this voltage range, referring to Fig. 5, we can see that suitable capacitor values to generate a 20 kHz signal (at 1V as supply voltage) are in the order of 1.5×10^{-10} F. This can be a drawback for the chip size.

About of power consumption, Fig. 6 reports power simulations as a function of the supply voltage V_{DD} and capacitor C. Power consumption decreases naturally with the reduction of the supply voltage. In contrast, the simulations reveal that the capacitors value C, is not explicitly related to power in this circuit. For purpose of comparison, when the supply voltage value is 1 V and for an output signal of 20 kHz, this circuit has a consumption power of 9 µW. At the end of this section, it has been remarked that to obtain the required operating frequency range, additional capacity must be included or greater number of stages must be designed. These points are disadvantages for the chip area. Therefore, the next paragraph will discuss a third topology of clock generators.

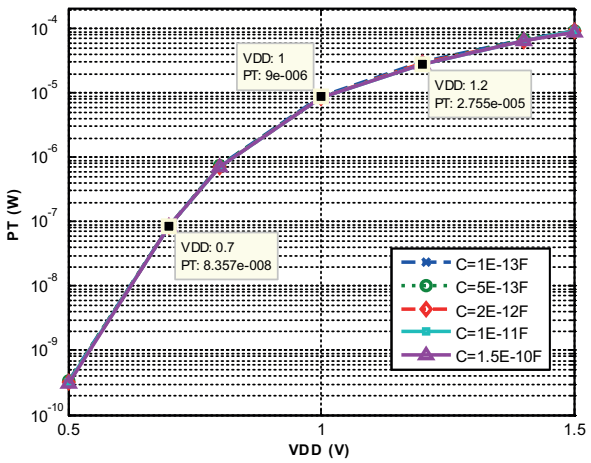

Figure 6: Simulated power-V_{DD} curves over a range of capacitor value, RO circuit

4 Voltage controlled ring oscillator VCRO

Since the limitations and drawbacks of the previous topologies the voltage-controlled ring oscillator (VCRO) will be opted to meet the custom performances (frequency, power and area) of the charge pump design. Different schemes can be used for controlling the circuit. Compared to the RO circuit, a voltage-controlled ring oscillator (VCRO) commonly uses variable voltage source to control its oscillation frequency (the possibility to adjust the clock frequency is obviously a strong point). Tunability of the VCRO is implemented via a variable resistance in the circuit. Theses resistances are designed using a transmission gate (Nmos-Pmos transistors), where the MOS transistors are controlled by their gate voltage. This topology (Fig. 7) was firstly proposed by Retdian [15] in order to improve the output voltage swing. Compared to Fig. 4, this circuit is also composed of three stages to satisfy some criteria. Among these criteria: the output frequency and the power consumption. Each stage includes one inverter (namely INV_i in Fig. 7, consisting of MP_{INVi} and MN_{INVi} transistors) and one transmission gate (namely TG_i, made up of MP_{TGi} and MN_{TGi}). The voltage V_{CONT} applied on transmission gates enables the resistance tuning. The result being as expected, a control of the output frequency, which can be given as:

$$f_o = \frac{1}{2NC_{in}\left(R_{in} + R_{TG}\right)} \quad (5)$$

Where: R_{IN} is the inverter equivalent resistance, and R_{TG}, the transmission gate equivalent resistance. C_{in} is the equivalent input capacitor of the following inverter (the sum of the MOS transistors parasitic capacitors).

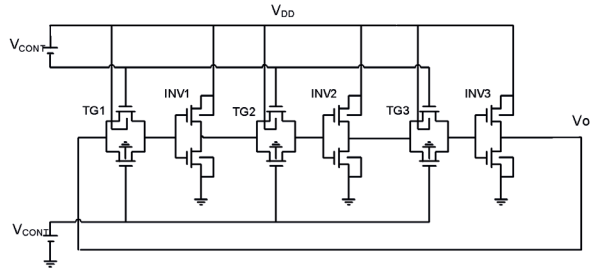

Figure 7: Voltage Controlled Ring Oscillator circuit, VCRO

5 VCRO performance optimization using contour graph approach : power, frequency and area

5.1 Contour graph approach

The contour graph approach is a good graphical tool for representing spatial relations between two variables. In addition, a contour line or isoline (often, is just called a « contour ») is a curve that joins points of equal values. Plotting these contours forms a map called a contour map.

Hence, considering the VCRO candidate, electrical and geometrical characteristics can be optimized, to find a minimum power dissipation point [16] using this contour graph approach.

In order to apply this approach and evaluate the the power dissipation and frequency behaviors, simulations are performed as a function of V_{DD}, V_{CONT} and W/L transistor ratios.

To go further, once V_{DD} and V_{CONT} have been fixed to their typical value (0.8 V), concerning the transmission gates and the inverters of VCRO: the W/L transistor ratio (which is assumed to be identical for each electronic sub-function), have an impact on the optimal operation point. Fig. 8, 9, 10 and 11 show their influence on isopower dissipation and isofrequency graphs.

First focusing on MP_TG and MN_TG transistors, frequency performance and power dissipation are studied for a set of values of W/L ratio. Contours of Fig.8 and 9 demonstrate that frequency performance and power dissipation are mainly dependent on MP_TG transistors.

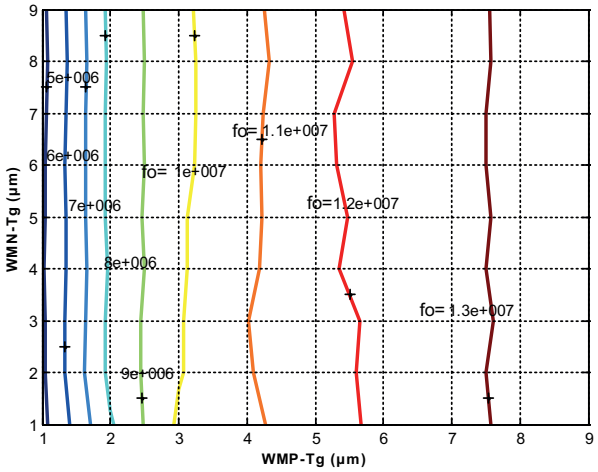

Figure 8: Isofrequency curves versus TG transistors width (MP_TG, MN_TG), VCRO circuit

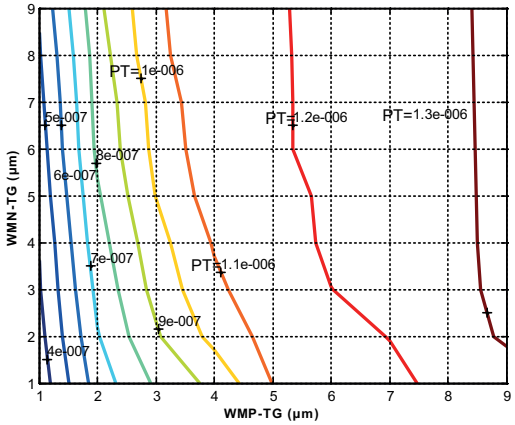

Figure 9: Isopower consumption (PT) versus TG transistors width (MP_TG,MN_TG), VCRO circuit

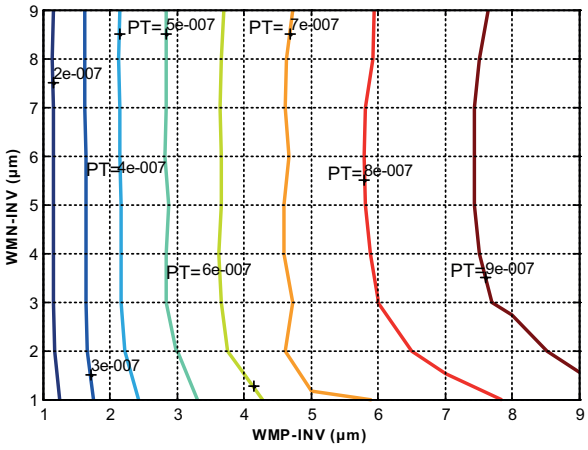

Figure 10: Isopower consumption curves versus IN transistors width (MP_INV, MN_INV) - VCRO circuit

Now, regarding the inverters and the effect of W/L transistor ratio: power dissipation and frequency performance are given respectively in Fig. 10 and Fig. 11 for MP_INV and MN_INV transistors.

It appears that the variation of power dissipation has a rather small fluctuation compared to MP_TG and MN_TG impact on the power dissipation (Fig. 10). About Fig. 11, MP_INV and MN_INV transistors have roughly the same impact on frequency performance.

Previously, we saw that C capacitors in ring oscillators didn't change power dissipation (Fig. 6). Consequently, it can suggest that inverter transistor dimensions (MP_INV, MN_INV) mainly contribute to the overall equivalent capacitance.

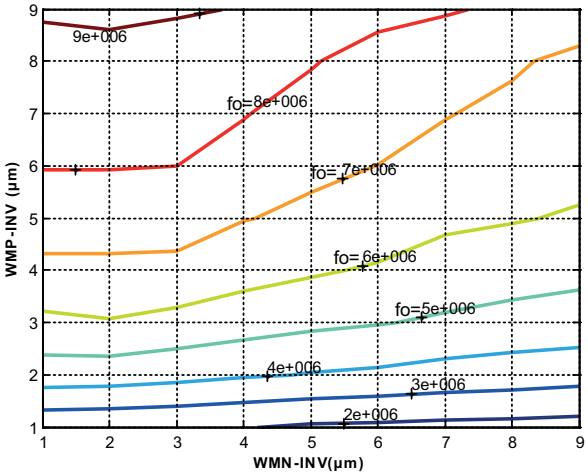

Figure 11: Frequency performance versus IN transistors width (MP_INV, MN_INV) - VCRO circuit

About the conclusions of this approach: these curves indicate that power dissipation is dominated by MP_TG transistors (as depicted by the vertical parts). A power optimization method can firstly consist of sizing of MP_TG transistors, based on energy resources. And secondly the desired frequency performance can be adjusted using the W/L ratios of MP_INV and MN_INV transistors. This methodology can save time for low power and low frequency oscillator with small size devices. In the purpose of our work, the operating frequency of the charge pump is in the range of tens of megahertz. By using this contour graph method (Fig 8, 9, 10, 11), the following sizes were selected to generate the required frequency.

Table 2: Selected CMOS transistors sizes - VCRO (V_{DD} = V_{CONT} = 0.8 V)

Transistors	W/L (µm)
MP_INV	9/0.6
MN_INV	4.5/1.2
MP_TG	3/0.6
MN_TG	1.5/1.2

For the given parameters of transistors, in order, to study the evolution of the power dissipation and frequency characteristics as a function of V_{DD}, V_{CONT} Fig. 12 and 13 show contour graphs representing lines of equal frequency and power (isofrequency and isopower graphs). In these simulations, the points that are located under the line defined by $V_{DD} = V_{CONT}$, should not be considered, as this means that $V_{DD} < V_{CONT}$. In this case, additional circuits are needed to generate negative voltages for the TG transistors. That's the reason why we will consider $V_{DD} > V_{CONT}$.

Concerning the frequency performance (Fig. 12), the output frequency (f_o), doesn't depend strongly on V_{DD} as denoted by the vertical parts. Reading the isolines of Fig. 13, power dissipation varies between 0.1 nW and 10 µW. For a given value of V_{DD} while V_{CONT} is increasing, we note that the power dissipation increases too.

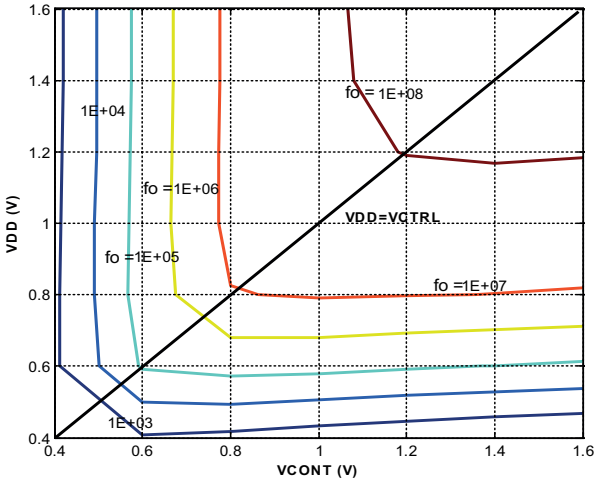

Figure 12: Simulated isofrequency contour graphs (fo) as a function of V_{DD} and V_{CONT}, VCRO circuit

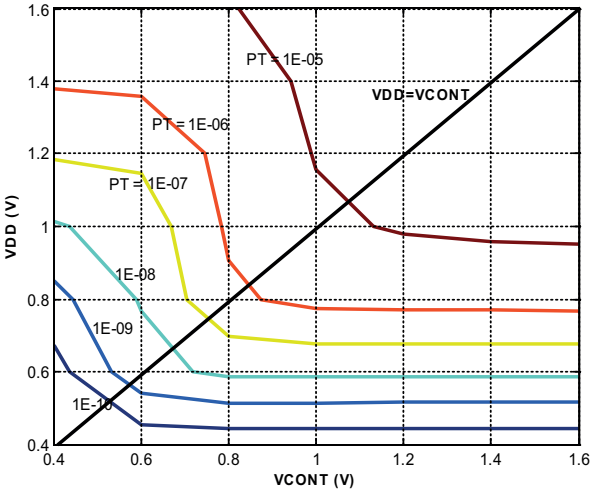

Figure 13: Constant power dissipation contour graphs simulations (PT) as a function of VDD and VCONT, VCRO circuit.

In order to operate to a specific frequency f_o (which depends on the CP topology) and at the minimum power dissipation, V_{DD} and V_{CONT} should be the lowest with respect to the application requirements. The optimal operating point can be extracted from these curves, which are useful for circuit design. The optimal operating point is the voltages (V_{DD} and V_{CONT}), which give the minimum power dissipation for a desired output frequency.

V_{DD} and V_{CONT} can be chosen independently. But Fig. 14 pictures the impact of the difference between the two voltages: power dissipation as a function of V_{DD} –V_{CONT} for different output frequencies. These results clearly show that the optimal point is achieved when V_{DD} = V_{CONT}.

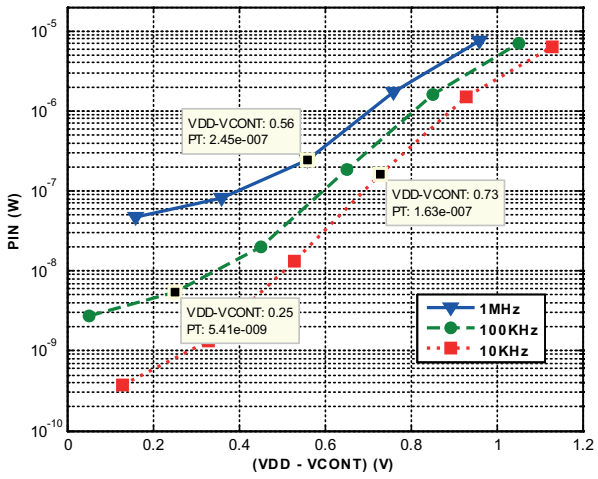

Figure 14: Power dissipation (P_T) as a function of V_{DD} - V_{CONT} for three frequencies, VCRO circuit

5.2 Validation of the approach and comparisons results

In order to evaluate the VCRO performance and the design approach, and for the purpose of comparison with previous clock generators (STCG, RO), the frequency and power performances (Fig 15 and16) have been investigated.

On Fig. 15, the output frequency is plotted as a function of V_{CONT} at a supply voltage of 1 V. For control voltage (V_{CONT}) between 0.1 V and 1 V, this topology achieves a tuning frequency range from 20 Hz to 36.6 MHz. This frequency range is reached using a reasonable silicon area as no additional capacitors are needed

Concerning the power dissipation (Fig. 16) the total power dissipation in CMOS circuits comes from two parts [17]: static and dynamic power.

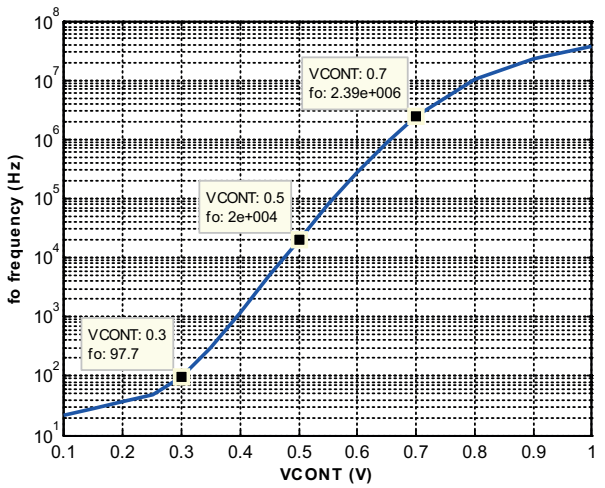

Figure 15: Output frequency simulation as a function of V_{CONT}, V_{DD} = 1 V, VCRO circuit

$$P_T = \underbrace{I_S V_{DD}}_{Statics} + \underbrace{aC_{out} V_{DD}^{\ 2} f_o}_{Dynamic} \quad (6)$$

Where, ***Is*** the total current leakage, ***a*** is the activity factor, C_{out} is the total output switching capacitance and f_o the clock frequency. Dynamic dissipation has theoretically been far greater than static power. This issue is also true for this circuit as proved in Fig. 16

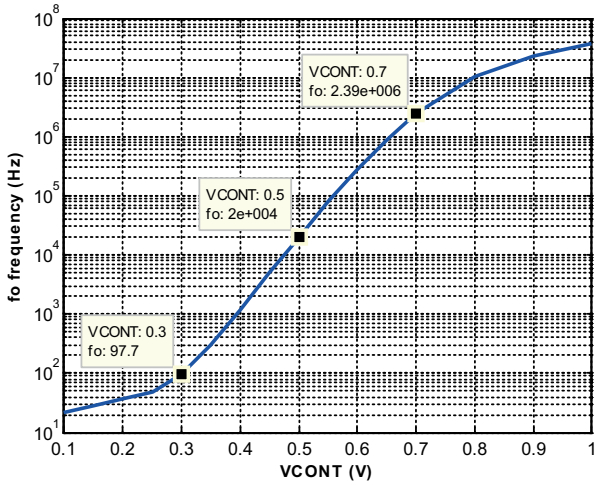

Figure 16: Simulated frequency dependence of power consumption (P_T), VCRO

In the same manner (in view of eq6), on Fig. 17, the total simulated power consumption, P_T, is reported as a function of V_{CONT} at V_{DD} = 1 V. Dynamic power dissipation increases with high V_{CONT} values. And as in some way Fig. 15 and 17 have shown that V_{CONT} and the output frequency has identical trend, it should be noticed that low V_{CONT} values cannot be used in the frequency range of interest. Thus in the useful range of V_{CONT} (V_{CONT} <0.35 V), dynamic dissipation dominates the total power consumption.

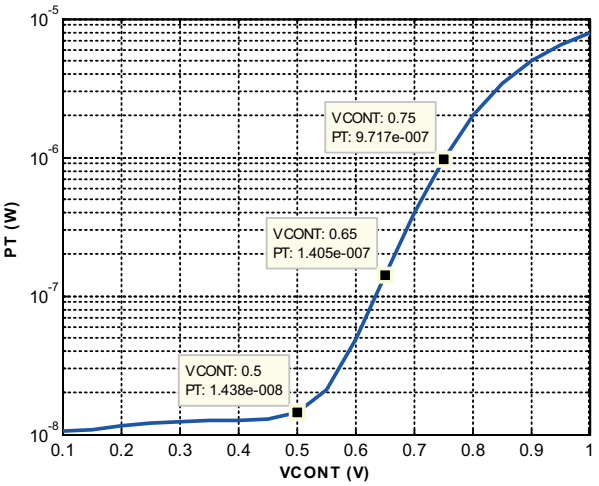

Figure 17: Simulated power dissipation (P_T) as a function of V_{CONT}, V_{DD} = 1 V, VCRO circuit

For the purpose of comparison, this circuit has a power consumption of 14.38 nW (Fig. 17) at V_{DD} = 1 V and V_{CONT} = 0.5 V. In this case the output frequency is 20 kHz.

These data (summarized in Table 3) tend to indicate that the VCRO reaches the lowest power dissipation for the operating ranges under consideration (frequencies, voltages). Indeed, the latter exhibits a typical 14.38 nW power dissipation, one decade below the others.

Table 3: Typical simulated power dissipations of the CMOS clock generators @ 20 kHz

VCRO	RO	STCG
P_T = 14.38 nW	P_T = 9 µW	P_T = 20 µW

6 Experimental results and discussions

In order to verify and validate the system operation for low frequency and low power power clock applications, a three stages voltage controlled ring oscillator was implemented using AMS 0.35 µm Si CMOS technology. Fig. 18 shows the microphotograph of the circuit. The VCRO occupies a small effective area of 1050 µm^2, where its dimensions are 42 µm x 25 µm.

This section also describes the measured results for the power dissipation and output frequency of the VCRO. Fig. 19 compares the simulated and measured power dissipation as a function of V_{CONT} at a supply voltage of 1 V. As seen the measured power dissipation increases with the voltage control as mentioned earlier. The trends are nearly the same. We note, however, an offset between the simulated and measured power consumption. Our analysis of the mismatch, of the circuit and the layout, took us to an assumption:

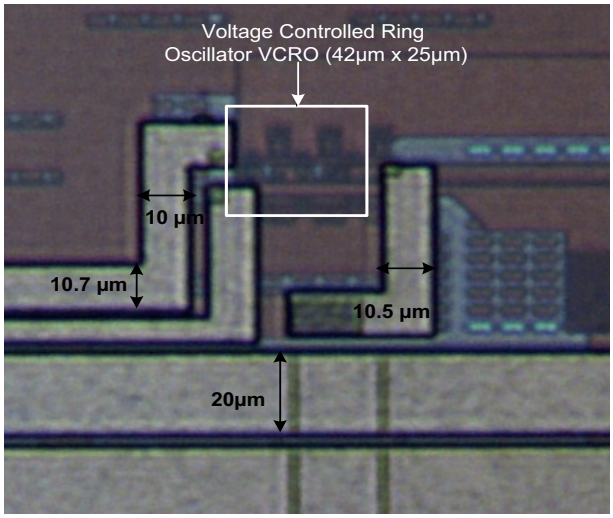

Figure 18: Die photo of the VCRO circuit using AMS 0.35 µm Si CMOS technology - active area: 42 µm x 25 µm

the effect of parasitics (resistances and capacitances) associated with metal wires, bonding pad and bonding wires. Indeed, in the context of the charge pump circuit, VCRO is not intended to be connected to any lead frame in an individual package. Among the possible parasitics, as we have two output bonding pads, we decided to include two capacitances to the circuit (Fig. 20), as it could change the output frequency and consequently the power consumption. Furthermore, about the interconnecting metal wires: their resistance can be neglected considering their short lengths and actual widths (Fig. 20).

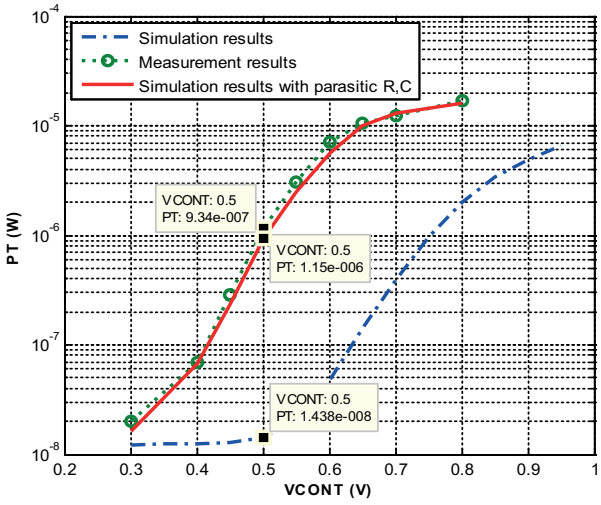

Figure 19: Measured and simulated power consumption as a function of V_{CONT} @VDD = 1 V.

Thus, new simulations were computed with the addition of C capacitors and their series resistors. As pictured in Fig. 19, a good match can be observed be-

tween the corrected measurements and prediction given in the previous section.

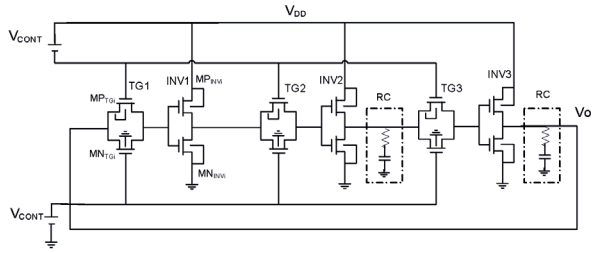

Figure 20: VCRO and the effect of selected parasitics

The second experiment (Fig. 21) aims at comparing the simulated and measured output frequency as a function of V_{CONT} and the supply voltage. These curves were obtained for V_{DD} ranging from 1 V to 2 V and V_{CONT} from 0.4 V to 0.65 V. Through these curves, we see that the frequency increases with the voltage control and also increases as the supply voltage increases too. Good agreement are observed.

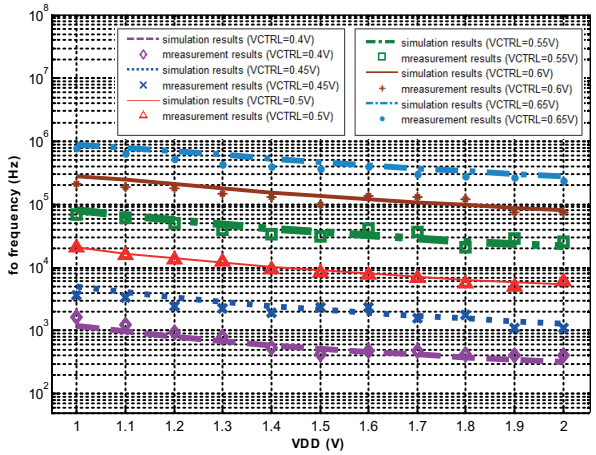

Figure 21: Measured and simulated output frequency as a function of V_{DD} and V_{CONT}

A summary of the performances of this circuit is presented in table 4.

To demonstrate the advantages of the proposed design, Table 5 reports performance comparisons between the VCRO circuit and others comparable designs which have been already reported in the literature.

Table 4: Simulated performances of the VCRO

Parameters	Values
Supply voltage	0.4 V-1.6 V
Control voltage range	0.4 V-1.6 V
Frequency range	400 Hz-190 Mhz
Power consumption range	25.23 pW-79.5 µW
Area of layout	1050 µm^2
Technology	AMS 0.35 µm CMOS

As observed the VCRO has very low power consumption with the lowest silicon area. A further advantage is that the VCRO circuit can be fully integrated, as it does not require any external components, compared to other circuits presented in Table 5.

Referring to section 5 and table 2, the frequency of oscillation of the VCRO while V_{DD} = 1 V and V_{CONT} = 0.5 V is around 20 kHz. Thus, Fig. 22 shows the transient simulation response for this frequency. In this typical condition, Fig. 23 illustrates the measurement output waveform of the VCRO oscillating at 18.62 kHz and exhibits the good agreement between simulation and experimental waveforms. Voltage level is also suitable for the charge pump CMOS switches control.

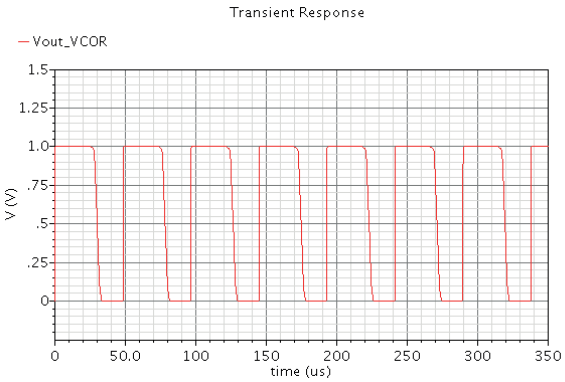

Figure 22: Simulated transient voltage of the VCRO, V_{DD} = 1 V, V_{CONT} = 0.5 V (F_{osc} = 20 kHz)

Table 5: Measured performances comparison with other designs

	[3]	[5]	[6]	[13]	[18]	This work
Supply voltage (V)	0.8	2.5	1.25	1.25	1	1
Power consumption (µW)	0.62	5.9	1120	810	52	1.15
Frequency (Hz)	50E3	34.6E3	6E6	200E3	100E3	20E3
External components	no	yes	yes	no	yes	no
Area (mm^2)	0.24	0.1	0.14	0.032	0.09	0.01050
Technology(µm, CMOS)	0.35	3	0.18	0.35	0.35	0.35

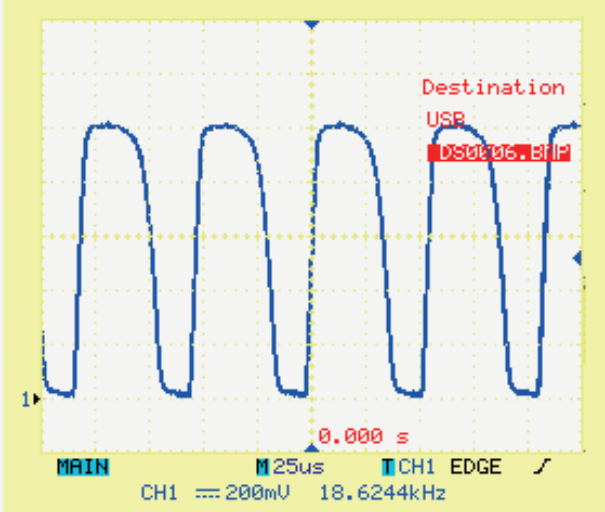

Figure 23: Measured VCRO output waveform V_{DD} = 1V, V_{CONT} = 0.5 V (18.62 kHz)

7 Conclusions

Through the preceding realizations and analysis, this work has examined power dissipation for three CMOS clock generator circuits. It has shown that the voltage controlled ring oscillator achieves the lowest power consumption for moderate frequency. Its silicon area on the chip is really interesting (1050 µm^2), which is significantly smaller than comparable clock generators. In comparison with others, another strong point was also studied: for the power consumption estimation, nanowatt values are observed. It can be less than 15 nW.

The simulation results also show that the VCRO exhibits a wide frequency tuning range, with good transient characteristics, both at high and low frequencies. This is usually difficult to obtain from the conventional generators.

Complementary simulations have shown the effect of input voltages (V_{DD}, V_{CONT}) and transistors sizes scaling (W/L ratios), on power and frequency performances. The optimal point is guaranteed when the V_{DD} = V_{CONT} relation is verified. Another important point is that, MP_TG transistors of VCRO, dominate the power dissipation and the frequency performance. From the same complementary simulations, contour graphs were drawn in order to find the optimal voltages and dimensions. These results are valuable information for the design of low power VCRO clock generator circuits.

Finally, to validate this approach, the VCRO circuit has been fabricated using AMS 0.35 µm Si CMOS technology. Output signal path parasitics has been considered for the power consumption measurements. A close agreement between simulation and experimental data is obtained, which testify the performances of the VCRO circuit for lower power systems and energy harvesting applications.

Acknowledgment: We gratefully acknowledge the financial support of the structural funds of the European Community, and the Regional Council Reunion Island (Region Reunion), for providing research grants (grant FEDER PRESAGE32933, CARERC project n°33933).

8. References

1. R.J.M. Vullers , R. van Schaijk, I. Doms, C. Van Hoof,R. Mertens "Micropower energy harvesting" Solid-State Electronics 53 684–693,(2009)
2. Inge Doms, Patrick Merken, Chris Van Hoof, and Robert P. Mertens, "Capacitive Power Management Circuit for Micropower Thermoelectric Generators With a 1.4 µA Controller" IEEE journal of solid-state circuits, vol. 44, no. 10, october 2009
3. F. Marraccini, G. D. Vita, S. D. Pascoli, G. Iannaccone, "Low-voltage nanopower clock generator for RFID applications", Microelectronics Journal 39 (12) (2008) 1736 – 1739.
4. Feng Pan, Tapan Samaddar « Charge Pump Circuit Design », 2006, 978-0071470452
5. P. Kakela, T. Rahkonen, J. Kostamovaara, "A micropower RC oscillator for consumer ASIC applications", Electrotechnical Conference, May 1991, Ljubljana, Slovenia, pp. 278–281.
6. F. Bala, T. Nandy, "Programmable high frequency RC oscillator", the 18th International Conference on VLSI Design, January 2005, Kolkata, India, pp. 511–515.
7. N. Weste, D. Harris, Principles of CMOS VLSI Design: "A Systems Perspective (3rd Edition)", Addison-Wesley, (2005).
8. Ming-Hung Chang, Chung-Ying Hsieh, Mei-Wei Chen, and Wei Hwang"Near-/Sub-threshold DLL-based Clock Generator with PVT-aware Locking Range Compensation" Low Power Electronics and Design (ISLPED) 2011 International Symposium on Aug. 2011,pp 15 - 20
9. Y. Teh, F. Mohd-Yasin, F. Choong, M. Reaz, "Design of adaptive supply voltage for sub-threshold logic based on sub-1 v bandgap reference circuit", Microelectronics Journal 39 (1) (2008) 24 – 29.
10. L. H. Ferreira, T. C. Pimenta, R. L. Moreno, "A cmos threshold voltage reference source for very-low-voltage applications", Microelectronics Journal 39 (12) (2008) 1867 – 1873.

11. Sun, X. Wu, "Subthreshold voltage startup module for setup dc-dc converter", Electronics Letters 46 (5) (2010) 373–374.
12. H. L. R.J. Baker, D. Boyce," CMOS (Circuit Design, Layout, and Simulation)", Wiley-IEEE Press, (1997).
13. Jamel Nebhen, and all «Temperature compensated CMOS ring VCO for MEMS gas sensor », 2013 Analog Integr Circ Sig Process (2013) 76:225–232
14. H. M.-N. P. M. Farahabadi, A. Ebrahimzadeh, "A new solution to analysis of cmos ring oscillators", Iranian Journal of Electrical and Electronic Engineering 5 (1).Vol 5, No.1, March 2009. (P32-p41)
15. N. Retdian, S. Takagi, N. Fujii, "Voltage controlled ring oscillator with wide tuning range and fast voltage swing, in: ASIC", 2002. Proceedings. 2002 IEEE Asia-Pacific Conference on, 2002, pp. 201 – 204.
16. A. Wang, A. Chandrakasan, S. Kosonocky, "Optimal supply and threshold scaling for subthreshold cmos circuits, in: VLSI", 2002. Proceedings. IEEE Computer Society Annual Symposium on, 2002, pp. 5 –9.
17. R. Gu, M. Elmasry, "Power dissipation analysis and optimization of deep submicron cmos digital circuits", Solid-State Circuits, IEEE Journal of 31 (5) (1996) 707 –713.
18. K. Lasanen, E.R. Ruotsalainen, J. Kostamovaara, "A 1-V, self adjusting, 5-MHz CMOS RC-oscillator", ISCAS 2002, May 2002, vol. IV, pp. 377–380.

Arrived: 16. 09 .2014
Accepted: 10. 11. 2014