Professional paper

Informacije MIDEM
Journal of Microelectronics,
Electronic Components and Materials
Vol. 45, No. 1 (2015), 73 – 79

Comparative Assesment of Ground Plane and Strained based FDSOI MOSFET

Avtar Singh[1],Sarosij Adak[2], Hemant Pardeshi[2], Arghyadeep Sarkar[3], Chandan Kumar Sarkar[2]

[1]Department of Electronics and Communication, Invertis University, Barielly, India
[2]Electronics and Telecommunication Engineering Department, Jadavpur University, Kolkata, India
[3]Department of Material Science & Engineering, National Chiao Tung University, Hsinchu, Taiwan

Abstract: In the present work, we have investigated the performance of ground plane and strained silicon on FDSOI MOSFETs. The 2D ATLAS simulations are done and the simulation model is validated with previously published experimental results. The transfer characteristics, DIBL, Vt, Ion and Ioff of all the structures are analyzed for 25 nm and 32 nm gate length. The effect of body thickness on device performance is also evaluated. Strained device offer higher drive current, but increases the leakage current. We have applied the ground plane to reduce the leakage current. The DIBL is higher for the strained device. DIBL in GPS and GPB structures (strained and unstrained) is almost same, and is lower than conventional FDSOI structure. The FDSOI devices have the lowest threshold voltage as compared to the GP and GPB devices, with GPB offering the highest Vt. The drain current is observed to increases almost linearly with body thickness. The deployment of ground plane and strained silicon on FDSOI MOSFET shows promise to substitute conventional MOSFET for high speed and low power applications.

Keywords: FDSOI; Strained FDSOI; Ground Plane in BOX; Ground Plane in substrate; DIBL

Primerjalna ocena FDSOI MOSFET-ov z masnim slojem in na osnovi napetega silicija

Izvleček: V članku predstavljamo rezultate raziskav lastnosti masnega sloja in napetega silicija na FDSOI MOSFET. Simulacije so opravljene z 2D ATLAS simulatorjem in preverjene z rezultati prejšnjih raziskav. Analizirane so prenosne karakteristike, DIBL, Vt, Ion in Ioff za dolžine vrat 25 nm in 32 nm. Prav tako je obravnavan vpliv debeline elementa na njegove lastnosti. Elementi z napetim silicijem omogočajo višje krmilne tokove, a imajo hkrati tudi večji uhajalni tok. Za zmanjševanje uhajalnega toka je dodan masni sloj. DIBL je višji ob uporabi napetega silicija. DIBL pri GPS in GPB elementih je enaka in nižja kot pri klasičnih FDSOI strukturah. FDSOI strukture imajo najnižjo pragovno napetost v primerjavi z GP in GPB elementi. Ponorni tok se linearno povečuje z debelino substrata. Uvedba masnega sloja pri FDSOI MOSFET nakazuje možnost njihove uporabe pir hitrih aplikacijah z nizko porabo.

Ključne besede: FDSOI; napet silicij; masni sloj; DIBL

** Corresponding Author's e-mail: avtar.ju@gmail.com*

1 Introduction

The performance of conventional MOS transistor is degraded by short channel effects in the sub-100 nm regime. In such a scenario, the Silicon-on-Insulator (SOI) technology come forward to become the next driver to continue the Moore's Law. SOI has proved capable of providing increased transistor speed, reduced power consumption and enhanced device scalability as demanded by the today's era and beyond technology generations. Today, however, the ever increasing demand for small size, high speed and low power consumption overshadows the inherent advantages of SOI. The fully depleted (FD) SOI transistor came into manufacturing mainstream by 2008 [1]. According to France-based Soitec, almost all semiconductor companies have either switched to SOI or are considering it for current and future devices. While IBM, AMD, Sony Group and Toshiba have adopted SOI for the cell processor, Philips semiconductors has been using SOI for high voltage ICs. Freescale and ST Microelectronics have also begun to use SOI wafers. Several device based on SOI varying from single gate to multiple gate

© MIDEM Society

structures have evolved and are in the stage of being researched [2].

Although SOI technology is widely used by the chip-makers, at smaller gate length (below 50 nm), its performance is degraded by short channel effects (SCE). For short gate lengths devices operates under very high traverse electric fields, which continue increases with scaling. The increase in the vertical electric field severely degrades silicon channel mobility [3]. Many device level techniques has been adopted to reduce the SCE's like- Thin body FD SOI with raised source and drain, graded Channel FDSOI, Metal gate FDSOI, Buried insulator Engineering, Ground plane FDSOI MOSFET, multiple gate FDSOI MOSFET , etc.

For the mobility enhancement, innovations in device design are required to keep up the device performance. In this regard, silicon has attractive feature, which boosts the device performance. Most of the semiconductor companies like Intel and Texas Instruments have switched to strained silicon based devices for mobility enhancement [4]. In fact, now, Silicon on Insulator (SOI) and Strained Silicon are the two key drivers of CMOS scaling.

In this paper, we have studied the effect of ground plane and strained silicon on FDSOI MOSFET. Ground plane is the highly doped P-type semiconductor in NMOS case and highly doped N-type semiconductor in PMOS. Ground plane is used for grounding the electric field lines originating from drain due to high drain bias. Ground plane act as a collector of the drain electric field lines, thereby reduces DIBL. Two types of insertion techniques viz. GPS (Ground plane in substrate) and GPB (ground plane in BOX) are possible. The GPB structure is more effective when the distance between the GP and the drain is small as compared to the channel length. In GPS structure, the BOX thickness should be kept as small as possible to reduce leakage current. To minimize the leakage current, GPB structure is preferred [5].

Strain in silicon channel can be introduced either during processing known as process-induced strain or from the bottom by growing silicon on top of a crystalline template typically silicon with 20 % or more germanium content, known as substrate-induced strain. In this work, we use the substrate-induced strain. The most effective way to introduce high tensile strain to the channel is to epitaxial grow strained silicon on a relaxed silicon germanium (Si-Ge) layer [6]. There is no doubt that Strained silicon helps in increasing the ON current, but it also significantly increases the leakage current (OFF current), which degrades the device performance. To decrease the leakage further we implied the concept of Ground plane in strained devices to optimize the device for low power and high-speed applications.

In this work, we have compared and analyzed the device performance of FDSOI, FDSOI-GP, FDSOI-GPB, Strain-FDSOI, Strain-FDSOI-GP and Strain-FDSOI-GPB MOSFETs. We have proposed new device, in which strained channel and ground plane, both device level techniques are incorporated in the same structure. This structure is the optimized structure of strained silicon and ground plane. The transfer characteristics, DIBL, V_t, I_{on} and I_{off} of all the six structures are analyzed for 25 nm and 32 nm gate length. The effect of body thickness on device performance is also evaluated. In Section 2, the device structure of all devices is discussed. In Section 3 the simulation framework and model calibration is discussed. Section 4 presents the result and discussion. Finally, section 5 concludes the paper.

2 Device Description

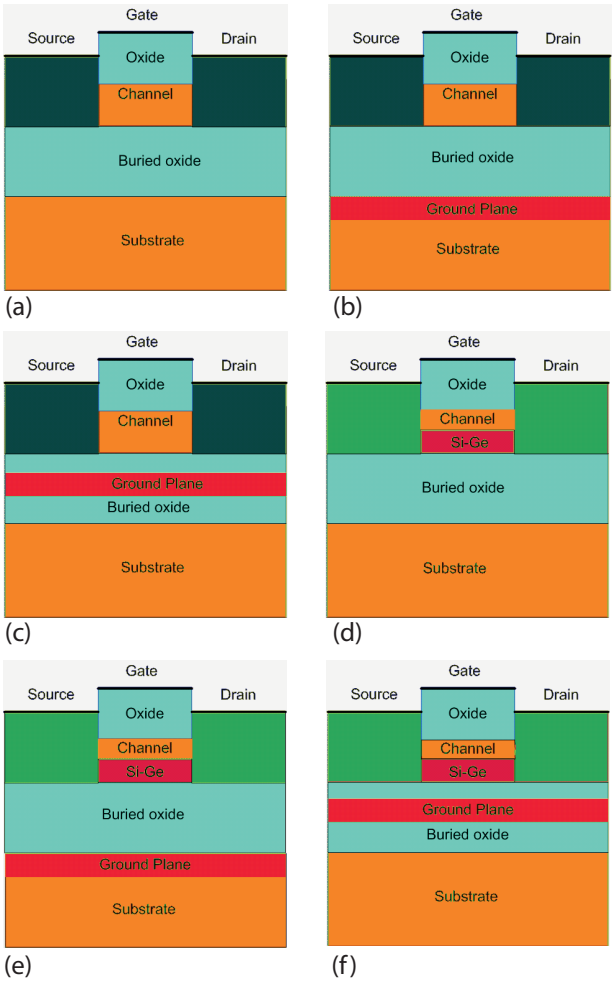


Figure 1: Physical structure of FDSOI devices (a) conventional FDSOI, (b) FDSOI-GP, (c) FDSOI- GPB, (d) Strained FDSOI, (e) Strained FDSOI-GP, (f) Strained FDSOI-GPB

Fig 1 shows the six different FDSOI device structure i.e. Conventional FDSOI (FDSOI), FDSOI with ground plane in substrate (FDSOI-GP), FDSOI with ground plane in BOX (FDSOI-GPB), strained FDSOI (Strain FDSOI), strained FDSOI with ground plane in substrate (Strain FDSOI-GP), Strained FDSOI with ground plane in BOX (Strain FDSOI-GPB). All the devices are analyzed at 25 nm and 32 nm gate length. Gate oxide thickness of 2 nm has been used. The source and drain regions are doped with the concentration of 10^{16} cm^{-3}, have an abrupt doping profile at source and drain ends. For conventional FDSOI BOX thickness of 50 nm and substrate thickness of 70 nm is used. Substrate has been taken intrinsic and channel has lightly doped with P-type semiconductor to adjust the threshold voltage. Ground plane is made by the P++ type doping in NMOS for the two structures of ground plane are discussed in this work, Ground plane thickness is taken as 5 nm in both the cases.

The strained SOI structure is designed using the substrate induced strain i.e. biaxial strain. Strain induced by placing the Silicon Germanium layer under the device silicon layer. The proportion of germanium in (Si-Ge) alloy and the thickness of the (Si-Ge) layer are the main factors that control the strain in the channel. We have used 20 % of germanium and 80 % of silicon and thickness of silicon germanium layer is 22 nm.

3 Simulation model calibration and experimental comparison

The 2D simulation were carried out by using ATLAS device simulator incorporating the concentration dependent mobility model and electric field dependent carrier mobility model with velocity saturation. Shockley–Read–Hall recombination/ generation with doping-dependent carrier lifetime, and Auger recombination were included in the simulation to account for leakage currents. For numerical iteration Gummel numerical solution procedures is used along with the Fermi Dirac carrier statistics to obtain an improved initial guess for Newton solution scheme. The Gummel iteration method is generally used for the SOI. Watt mobility model is also used with suitable modification in the saturation velocity of the electrons for considering best mobility approximation In the presence of heavy doping, greater than 10^{18} cm^{-3}, experimental work has shown that the pn product in silicon becomes doping dependent. As the doping level increases, a decrease in the bandgap separation occurs, where the conduction band is lowered by approximately the same amount as the valence band is raised. To deploy the strain in the simulation we used the strained silicon low field mobility model [7].

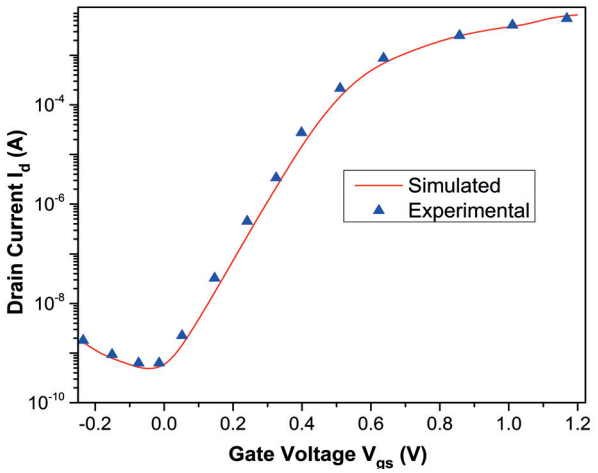


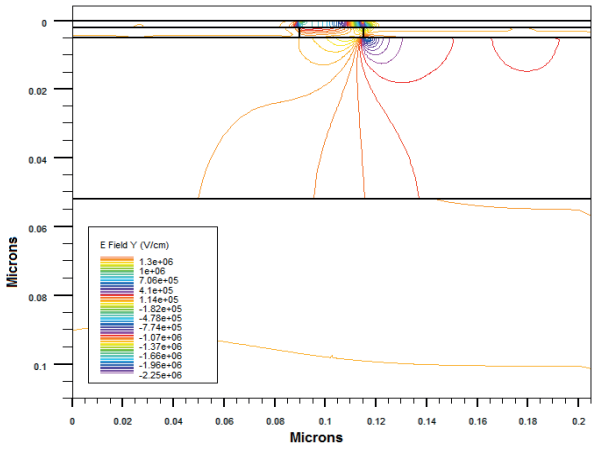
Figure 2: Experimental [8] (symbols) and simulated (solid lines) transfer characteristics for FDSOI-GP at V_{ds} = 1 V.

In this section, we have simulated the fabricated Ground Plane FDSOI structure of ref [8] and calibrated our simulation model by comparing the simulation with the experimental transfer characteristic. Fig 2 shows a very good agreement between the experimental [8] and simulated transfer characteristics of FDSOI-GP device, validating our simulation model. Post validation extensive simulation of the FDSOI, FDSOI-GP, FDSOI-GPB, Strain FDSOI, Strain FDSOI-GP, and Strain FDSOI-GPB is done to analyze the effect of gate length and body thickness on the device performance.

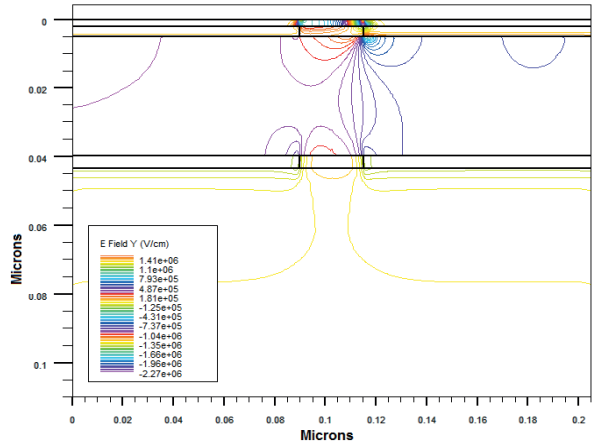
4 Results and Discussion

Fig. 3 shows the electric field contour of the FDSOI, FDSOI-GP, and FDSOI-GPB structures. In Fig 3(a), conventional FDSOI have large number of electric field lines passing through the channel body, hence the drain to substrate leakage is high in this structure. Whereas, in FDSOI-GP and FDSOI-GPB (fig 3(b) and 3 (c)) comparatively less electric field lines pass through the channel, thereby reducing the leakage due to the addition of ground plane in conventional FDSOI structure. The GPB structure has the lowest leakage in all the above mentioned structures due to the reduced distance between the channel and the ground plane [5].

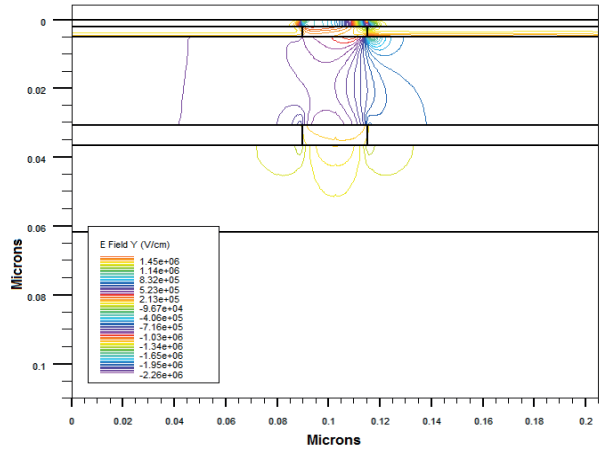
Fig 4 shows the transfer characteristics for a 25 nm (Fig 4a) and 32 nm (Fig 4b) length device. On reducing gate length from 32 nm to 25 nm the drain current is obseved to increases for all devices. The fact that the drain current is able to sustain its increase is thanks to the increasing drain velocity at the drain side of the device. On-state current, I_{on}, defined as the current at V_{dd} = 0.8 V when the gate length is 25 nm and V_{dd} = 25 nm



(a)



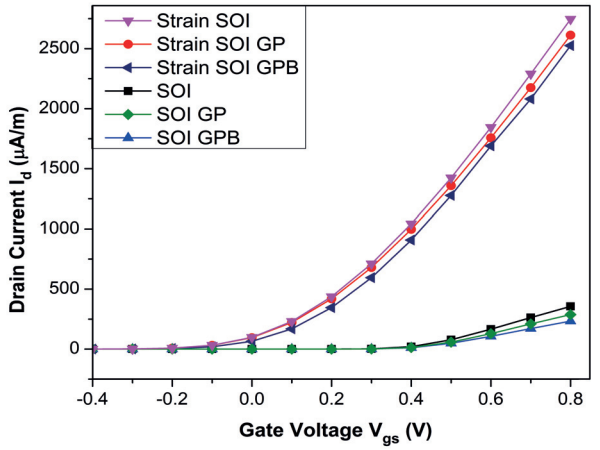
(b)



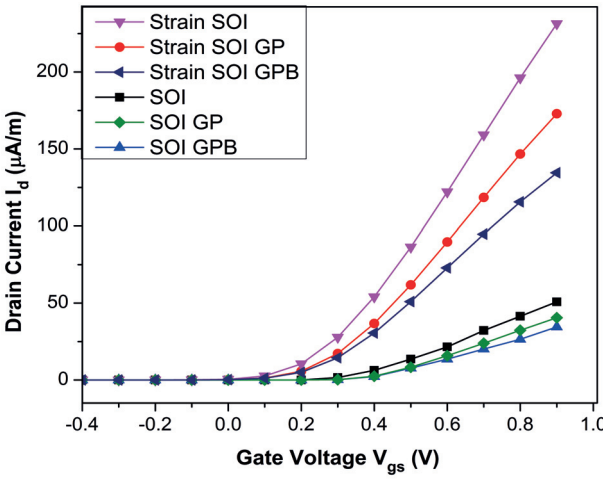
(c)

Figure 3: Electric Field Contour for FDSOI Devices extracted from ATLAS device simulator at $V_{gs} = V_{ds} = 1$ V. (a).Conventional FDSOI, (b). FDSOI-GP, (c). FDSOI-GPB

for 32 nm gate length, it is greater in strained channel devices then devices without strain in channel because application of biaxial strain to the channel increases the mobility of the charge carriers and increased mobility directly enhances the drive current.[9] The I_{on} is inversely proportional to gate length and it increases as gate length decreases.



(a)

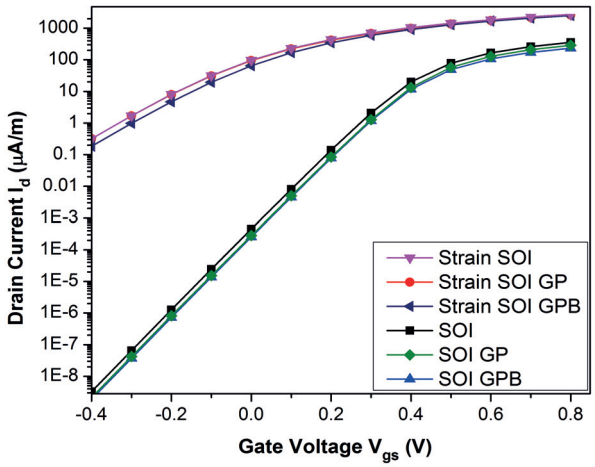


(b)

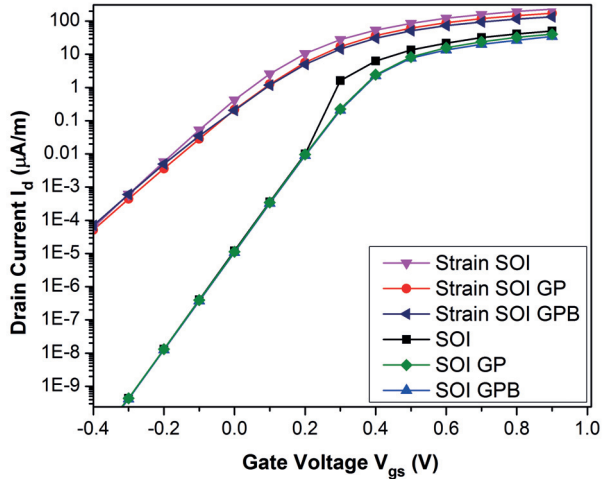
Figure 4: Transfer Characteristics of the FDSOI, FDSOI-GP, FDSOI-GPB, Strain-FDSOI, Strain-FDSOI-GP and Strain-FDSOI-GPB devices. (a) For gate lengths of 25 nm, (b) For gate length 32 nm. The drain voltage $V_{ds} = 1$ V.

The benefit of adding strain is visible at both the gate lengths. The I_{on} is highest for FDSOI devices followed by GP and GPB for both stained and unstrained devices. In GPB structures, the current drive capability of the transistor is less as the active region is much closer to the ground plane.

From figure 5, it can be seen that the off state leakage current (I_{off}) defined as the drain current at zero bias. This leakage current is less in GP structures because the highly conducting surface (ground plane) acts as a barrier for electric field and shields the fringing electric field lines from drain to channel. The leakage cur-



(a)



(b)

Figure 5: Subthreshold Characteristics of the FDSOI, FDSOI-GP, FDSOI-GPB, Strain-FDSOI, Strain-FDSOI-GP and Strain-FDSOI-GPB devices. (a) For gate lengths of 25 nm, (b) For gate length 32 nm. The drain voltage V_{ds} = 1 V.

rent is lowest in case of GPB structures because in this structure the active region of the device comes closer to ground plane region[5], reducing the drain induced electric field [5]. The leakage current is significantly larger for the device with channel under strain. To reduce the leakage current in strained FDSOI further we apply the ground plane, and it reduce the leakage current upto some extent.

In short gate length (L_g) devices the threshold voltage (V_t) is a function of drain to source voltage (V_{ds}) leading to Drain Induced Barrier Lowering (DIBL). As L_g reduces, the drain depletion region comes closer to the source depletion region and finally the field is penetrated. The lowered potential barrier at the source increases the injection of electrons by the source over the reduced channel barrier, due to which V_t is shifted. To find the DIBL, we have to first calculate the threshold voltage as the gate voltage at which the drain current I_d= 6 (*W*/*L*) nA, where width, *W* of the device is taken as 1 μm. DIBL short channel effect is calculated by the

$$DIBL = \frac{\Delta V_{th}}{\Delta V_{ds}} = \left[\frac{(V_{th1} - V_{th2})}{(V_{ds1} - V_{ds2})}\right] \quad (1)$$

where, V_{th1} is threshold voltages extracted at drain bias of V_{ds1} = 0.1 V and V_{th2} is threshold voltages extracted at drain bias of V_{ds2}=1.0 V

Fig 6 shows the DIBL of all the devices under consideration having gate length of 25 nm and 32 nm. It is observed that DIBL increases with decreasing in L_g. The degradation in DIBL with L_g is due to the interaction of drain and source side depletion regions with each other near the channel surface to lower the source potential barrier. When a high V_{ds} is applied to a short gate length device, it lowers the barrier height, resulting in further decrease of the V_t. It is known that DIBL in ground plane devices is dependent on the distance between the channel and the ground plane [10]. If this distance is reduced DIBL will also reduce due to the effect of grounding the electric field lines originating from channel at high drain voltage. DIBL of GPS and GPB structure is almost same (Fig 6) because the distance of the ground plane from the channel is same in both the structures.

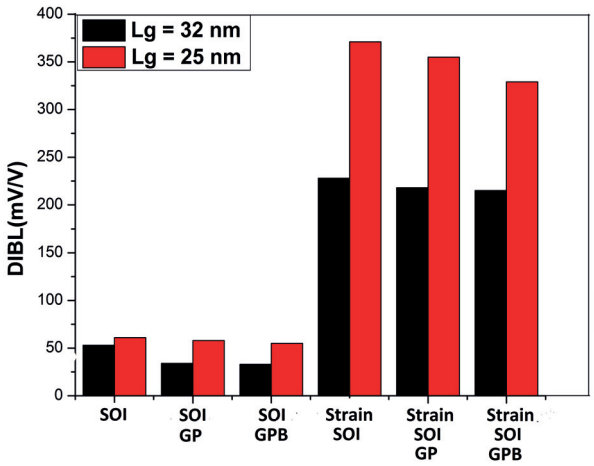
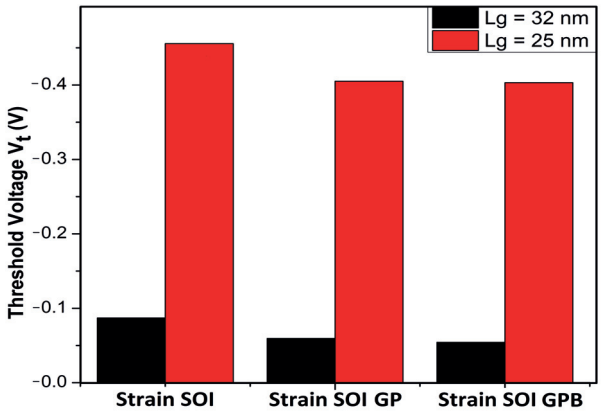


Figure 6: Comparison of DIBL for the FDSOI, FDSOI-GP, FDSOI-GPB, Strain-FDSOI, Strain-FDSOI-GP and Strain-FDSOI-GPB devices at gate lengths of 25 nm and 32 nm.

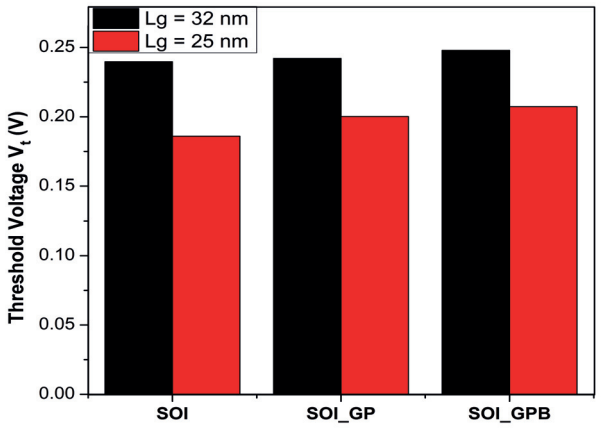
The strain causes the band gap (E_g) reduction that decreases the silicon work function (Fermi level decreases due to the increase of the intrinsic carrier concentration), which consequently affects the depletion region at the drain/channel junction, increasing the DIBL [11]. The DIBL for all the strained device is observed to be higher than unstrained devices. The DIBL for GPS and

GPB structures (stained and unstrained) is almost same, and is lower than conventional FDSOI structure.

The variation in threshold voltage for all devices for 25 nm and 32 nm gate lengths are shown in Fig 7. The V_t reduces with decrease gate length because of V_t roll-off effect. The FDSOI devices have the lowest V_t as compared to the GP and GPB devices. The V_t of GP and GPB devices is almost same, with GPB having slightly higher V_t as compared with GP device. The ground-plane keeps the electric field lines from propagating into the channel region, which helps to improve the SCE. The blocked field leads to increases in the threshold voltage. The application of strain reduces the threshold voltage [9].



(a)

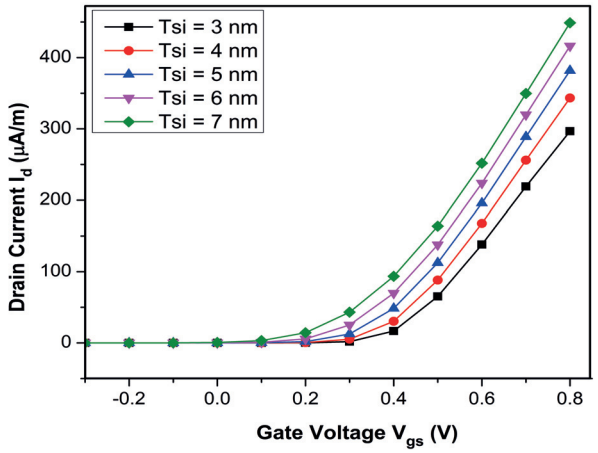


(b)

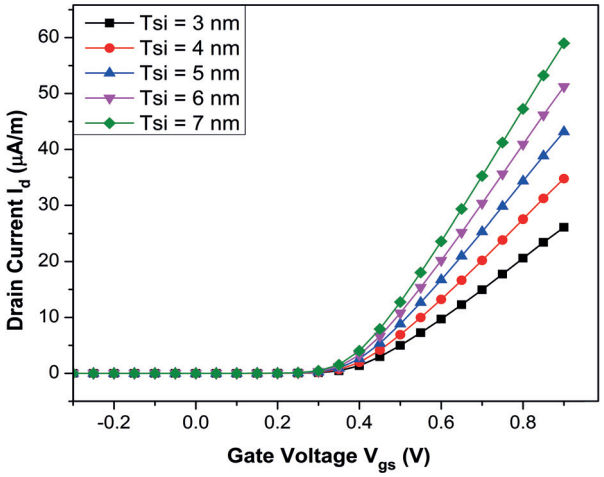
Figure 7: Comparison of Threshold Voltage for the FD-SOI devices at gate lengths of 25 nm and 32 nm. (a). Unstrained FDSOI, FDSOI-GP, FDSOI-GPB (b). Strain-FDSOI, Strain-FDSOI-GP and Strain-FDSOI-GPB

The strained Si/SiGe devices have negative threshold voltage. Negative threshold voltage is due to the lower conduction band edge in the strained Si than that in SiGe. The band gap narrowing is larger for biaxial strain as the valence band edge is shifted more. The threshold voltage decreases with increase in Ge content because of decrease in flatband voltage, decrease in source-body/drain-body build in potential [12].

The transfer characteristics of the conventional FDSOI devices as a function of body thickness are shown in Fig. 8a (for L_g=25 nm) and Fig.8b (for L_g=32 nm). It is observed that the drain current increases almost linearly with T_{si}. For body thickness less than 3nm, the quantum mechanical effect start to dominate and degrades the device performance. The threshold voltage (V_t) decreases as T_{si} increases and short channel effects comes into existence. The scaling of the T_{si} region increases the distance between conduction band (E_C) and ground state eigen energy due to which carriers goes into the higher energy subband, fermi level is also moves towards



(a)



(b)

Figure 8: Transfer Characteristics of the FD SOI devices as a function of body thickness. (a) L_g = 25 nm, (b) L_g = 32 nm. The drain voltage V_{ds} = 1 V.

ground state eigen energy, due to which V_t increases. The peak values of drain current for the 25 nm device is 448 µA (Fig 8a.) and for 32 nm device is 58.9 µA (Fig 8b). These values are also shown in the table (Table 1).

Table 1: I_{on} and I_{off} of the FDSOI, FDSOI-GP, FDSOI-GPB, Strain-FDSOI, Strain-FDSOI-GP and Strain-FDSOI-GPB devices at gate lengths of 25 nm and 32 nm.

	L_g = 25 nm		L_g = 32 nm	
Device	I_{on} (µA)	I_{off} (nA)	I_{on} (µA)	I_{off} (pA)
FDSOI	356	45.2	50.7	12.1
FDSOI-GP	287	28.1	40.5	11.3
FDSOI-GPB	233	25.1	34.5	10.8
FDSOI	2750	97.9	231	0.418
FDSOI-GP	2610	94.7	172	0.216
FDSOI-GPB	2530	64.2	134	0.205

5 Conclusion

Effect of ground plane and strained silicon on FD SOI MOSFET (fully depleted Silicon on insulator MOSFET) has been studied. I_{off} reduced using FDSOI-GPS structure as compared to conventional FD SOI MOSFET and it is further reduced in case of FDSOI-GPB structure at two gate lengths 25nm and 32nm. The leakage current is less in GPB because in this structure the device region comes closer to ground plane region. Hence, the drain induced electric field reduced. In these structures, the current drive capability of the transistor also reduces. To increase the I_{on} concept of strained silicon has been deployed. The peak drain current in strained FD SOI structure is 2.750 mA as compared to 0.356 mA of conventional FD SOI MOSFET for 25 nm gate length device. To decrease leakage current, the concept of ground plane in strained SOI structure has been introduced. The simulated result shows that there is a reduction of leakage current by using strained GPS FD SOI up to some extent. The DIBL for all the strained device is observed to be higher than unstrained devices. The DIBL for GPS and GPB structures (strained and unstrained) is almost same, and is lower than conventional FDSOI structure. The FDSOI devices have the lowest V_t as compared to the GP and GPB devices, with GPB offering the highest V_t.). The drain current is observed to increases almost linearly with T_{si}.

6 Acknowledgement

The authors would like to thank Department of Science and Technology, Govt. of India, AICTE, and Invertis University, Barielly for their valuable support in carrying out this research work.

7 References

1. T. Numata, K. Uchida, J. Koga, and S. Takagi, "Device design for subthreshold slope and threshold-voltage control in sub-100 nm fully-depleted MOSFETs", *IEEE Trans. Electron Devices*, vol. 51, pp. 2161-2167, Dec. 2004
2. A.Vandooren, D. Jovanovic, S. Egley, M. Sadd, B.-Y. Nguyen, B. White, M. Orlowski, and J. Mogab, "Scaling assessment of fully-depleted SOI technology at the 30 nm gate length generation", in *Proc. IEEE Int. SOI Conf.*, Oct. 2002, pp. 25–26.
3. L. Ge, J. G. Fossum, and B. Liu, "Physical compact modeling and analyses of velocity overshoot in extremely scaled CMOS devices and circuits", *IEEE Trans. Electron Devices*, vol. 48, pp. 2074–2080, Sept. 2001
4. Moroz et al., "The Impact of Layout on Stress-Enhanced Transistor Performance", Int. Conf. SISPAD, 2005, pp. 143-146
5. M. J. Kumar and M. Siva, "The Ground Plane in Buried Oxide for Controlling Short-Channel effects in Nanoscale SOI MOSFETs", *IEEE Transactions on Electron Devices*, vol. 55, no. 6, pp. 1554 – 1557, June2008.
6. K. K. Rim, J. L. Hoyt, and J. F. Gibbons, Fabrication and analysis of deep submicron strained-Si N-MOSFETs, *IEEE Transactions on Electron Devices*, vol. 47, pp. 1406-1415, 2000.
7. ATLAS user's manual' (Silvaco Int, 2010).
8. M. K. Md Arshad, S. Makovejev, S. Olsen, F. Andrieu, J.-P. Raskin, D. Flandre, and V. Kilchytska, "UTBB SOI MOSFETs analog figures of merit: Effects of ground plane and asymmetric double-gate regime", *Solid. State. Electron.*, vol. 90, pp. 56–64, Dec. 2013.
9. S.-T. Chang, "Nanoscale Strained Si/SiGe Heterojunction Trigate Field Effect Transistors", *Jpn. J. Appl. Phys.*, vol. 44, no. 7A, pp. 5304–5308, Jul. 2005.
10. M. Saremi, B. Ebrahimi, A. A. Kusha, M. Saremi, K. Abad, and K. Abad, "Process Variation Study of Ground Plane SOI MOSFET" *2nd Asia Symposium on Quality Electronic Design,* 2010.
11. S. Dereste, J. A. Martino, E. Simoen, and C. Claeys, "Impact of Selective Epitaxial Growth and Uniaxial / Biaxial Strain on DIBL Effect Using Triple Gate FinFETs", *Journal Integrated Circuits and Systems,* vol. 5, no. 2, pp. 154–159, 2010.
12. M. J. Kumar, S. Member, V. Venkataraman, S. Member, and S. Nawal, "Impact of Strain or Ge Content on the Threshold Voltage of Nanoscale Strained-Si / SiGe Bulk MOSFETs", *IEEE Transactions on Device and Materials reliability*, vol. 7, no. 1, pp. 181–187, 2007.

Arrived: 21. 07. 2014
Accepted: 23. 09. 2014